SURVEY OF FPGA BASED MEMORY DESIGN

[1]Brinda Rathod, [2] Tarun Agrawal, [3] Mrs. Shivi Shukla
[1]Master Student, [2]Master Student, [3]Project Engineer
[1]VLSI & Embedded System Design, Electronics & Communication Engineering
[1]GTU PG School,Gandhinagar,Gujarat,India,[2]GLA University, Mathura, India,[3] CDAC,Pune,India

Abstract : ***This survey paper provides comparative analysis of IO standards. This comparison is based on different parameters i.e. different operating frequency, various temperature and various kind of Nanometer(nm) FPGA devices. Basically IO standards used for impedance matching between IO ports and Logic Blocks of FPGA. Also IO standards used in many applications like high speed data transmission, low power memory design , low power multipliers and many more. For proper voltage signals and impedance matching between IO ports and logic blocks of FPGA, selection of proper IO standard is must. This analysis is helpful to select proper IO standard for designing of memory like SRAM on FPGA.***

IndexTerms – Low Power, SRAM, FPGA, IO Standard

I. INTRODUCTION

From the past decades , researchers worked on memory designing to make it power efficient , area efficient , cheaper and faster. Efficient memory design has to provide less delay for faster operation. There is always trade-off between these parameters[1]. Means if we want higher speed then we have to compromise with power. According to Moore's law number of transistors are doubled after each 18 months. This is because of technology is getting shrinking to Nanometer scale. If technology is scaled down then number of transistors are more, if transistors are more then number of logic cells are more and so density of FPGAs increases. Therefore, new FPGAs are fabricated on 16nm node[1]. Now, as far as memory concerns , its design has to be efficient, and if we want to design such kind of memory on FPGA then selection of IO standards is better approach for this work. SRAM is static memory , provides random read-write operation and also provides faster performance compared to DRAM. Therefore, It has to be power efficient up to some extent. Off course there is trade off between power and speed but still if we select proper IO standard then it is possible to design efficient memory[7].

SRAM is the nearest memory to the processor which provides faster operation than any other memory. Its basic Architecture has 6 Transistor cell [8] as shown in Fig. 1. Back to back inverter is connected to retain the data in the cell. To access this bit of data, access transistors are used which are connected to bit lines. Its read and write operation requires pre-charging of bit lines, then according to internal data, discharging of bit lines will be performed. Sizing of cell for efficient read and write operation is must. Therefore, transistor sizing of SRAM cell is essential part of SRAM Design[8]. Fig.1 shows the basic structure of static memory cell, which consist of two PMOS pull up transistor(PM0,PM1) and two NMOS pull down transistor(NM0,NM1). Access transistors (NM2,NM3) are used to transfer the internal bit of data to bit lines(bl,bl_bar). Gate of Access transistors, is connected to word line(wrt). If wrt line is asserted then and then only read or write operation of cell can be happened.

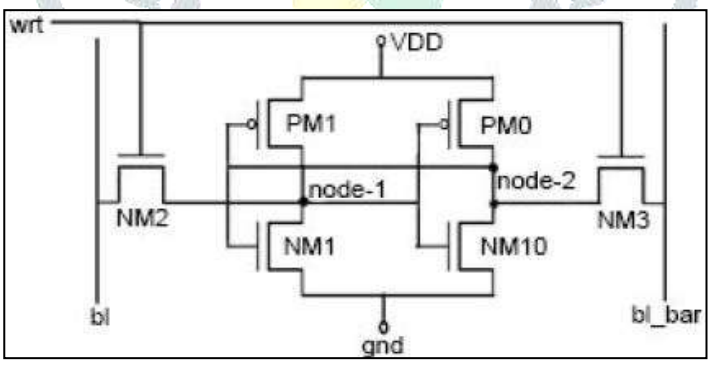

Fig. 1 SRAM 6 Transistor Cell [8]

FPGA is Field Programmable Gate Array, contains thousands of logic cells, Flip flops and many other digital blocks. All these modules present in CLB(Configuration Logic Block). CLB is one of the main block of FPGA. For communication between CLBs to IO pads or vice versa, programmable interconnects are there. Internal Architecture of FPGA contains CLBs, IO pads and Programmable interconnects as shown in fig.2[6]. From the past three decades, it is observed that process technology of FPGA is grown up[1]. Due to this, Ultra-scale FPGAs are fabricated on 16 nm technology node. Security of FPGA in terms of its storage data gains more attraction now a days. SRAM based FPGAs were build to provide better security[11]. The basic feature of SRAM that is its volatility is used for security purpose in SRAM based FPGAs.

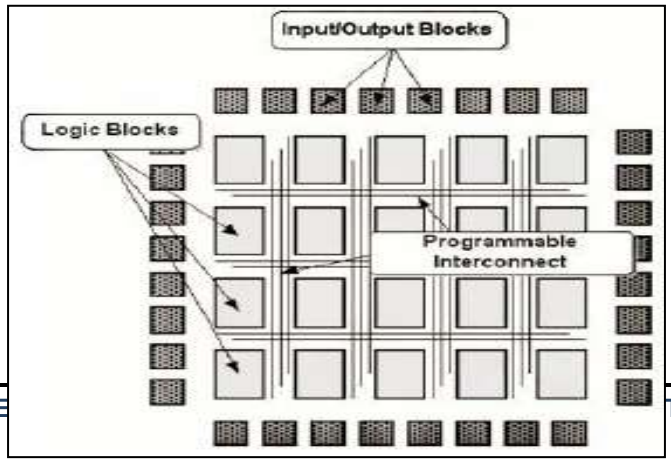

Fig.2 Internal Architecture of FPGA[6]

If power is cut off from the memory then its data does not present in it and no one can steal this bit streams(FPGA data) of FPGA. This kind of security feature is present in 7 series of Xilinx's FPGAs and Altera's Stratix FPGA. Basically military, industrial and space applications uses these FPGAs. Section II is about different IO standards provided by FPGA, Section III is about IO standard related results. At last, Section IV is about conclusion and future work.

II. DIFFERENT IO STANDARDS PROVIDED BY FPGA

WhereverTimesisspecified,TimesRomanorTimesNewRomanmaybeused.Ifneitherisavailableonyourwordprocessor,pleaseusethefontclosestinappearancetoTimes.Avoidusingbit-mappedfonts.TrueType1orOpenTypefontsare required.Pleaseembed all fonts, in particular symbolfonts,aswell,formath,etc. IO standards used as buffer, provides different configuration i.e. internal supply voltage, output driver supply voltage, reference voltage etc. These buffers resides between IO blocks or IO pads and Logic blocks of FPGA. When any signal transmitted from port to logic block or vice versa , there is a chance of noise added into this signal and signal gets disrupted. This phenomena of disrupting signal is called transmission line effects , due to which actual data will not sent/receive at desired location. To reduce these kind of effects, buffers in terms of IO standards are used. Different IO standards provided by FPGA are High speed trans-receiver logic(HSTL)[2], Stub Series Terminated logic(SSTL)[7],[10], Low voltage Digitally control Impedance with Half Impedance (LVDCI_DV2)[7],Low voltage Transistor Transistor logic(LVTTL)[6], Low voltage CMOS(LVCMOS) [7],[4]and Mobile DDR(Double Data Rate)[6]. These IO Standards have different Families, which are operated on different supply voltages. Some of these family is mentioned here.

A. HSTL IO Family:

HSTL mainly classified into output buffer supply voltage like HSTL_II_18 has 1.8V VCCO. HSTL_II_12 has 1.2V VCCO.Fig.3 shows the various family members of HSTL family. HSTL is technology independent IO standard. Used for mainly durability of hardware.

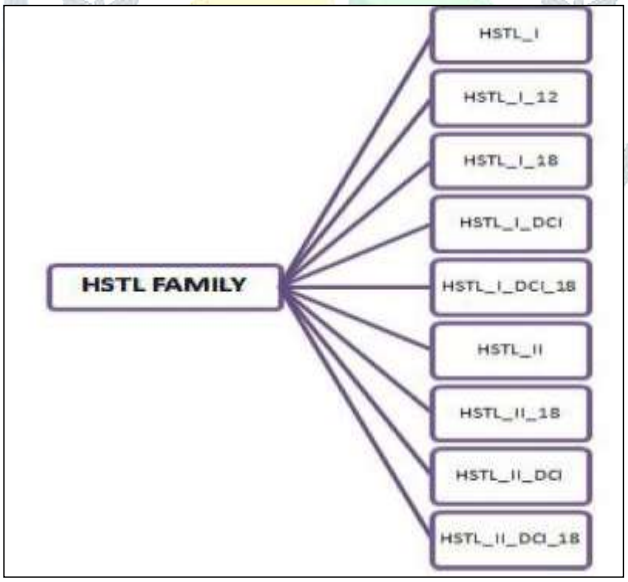

Fig.3 Family of HSTL Standard[2]

B. LVCMOS IO Family

Low Voltage CMOS is generally used for Low Power Application like 3.3V, 2.5V, 1.8V, 1.5V and 1.2V application. It also has various Family types as shown in Fig.4. LVCMOS is upgraded version of LVTTL.

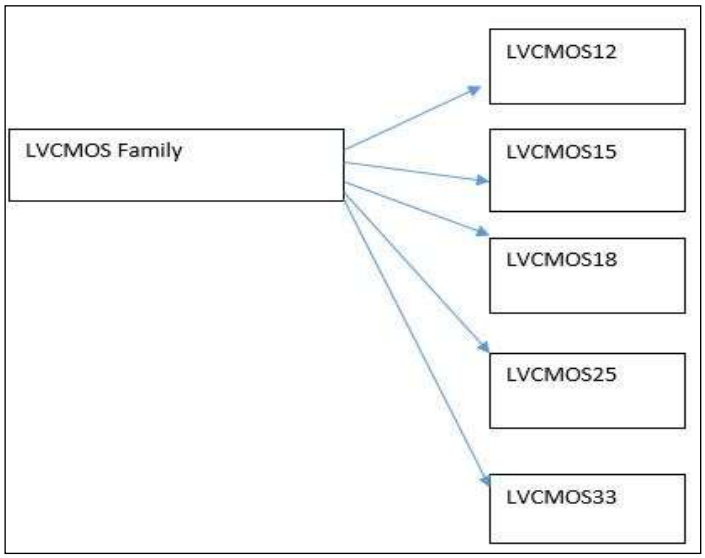

Fig.4 Family of LVCMOS[2]

C. IO Buffer Schematic

IO buffer schematic helps to understand the buffer design of IO standard. This schematic provides information about its configuration parameters i.e.VTT(termination voltage), Vref(reference voltage), Vccint(internal core supply voltage), VCCO(output buffer supply voltage) etc. Below figures gives schematic of HSTL and LVCMOS IO standards.

Fig.5 shows HSTL class I buffer. Its specification is provide by JEDEC. Here, 50ohm impedance is used to match the impedance between output buffer and input buffer. VTT is termination voltage used for termination of this line. Rp is parallel resistance, connected to the transmission line of buffers. This termination resistor is used to minimize reflections of signals in transmission line.

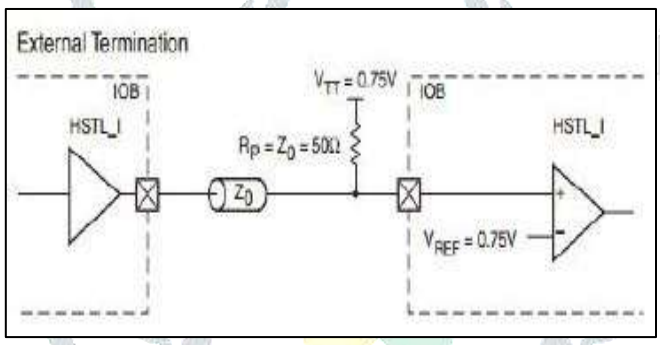

Fig.5 HSTL class I Buffer Schematic[7]

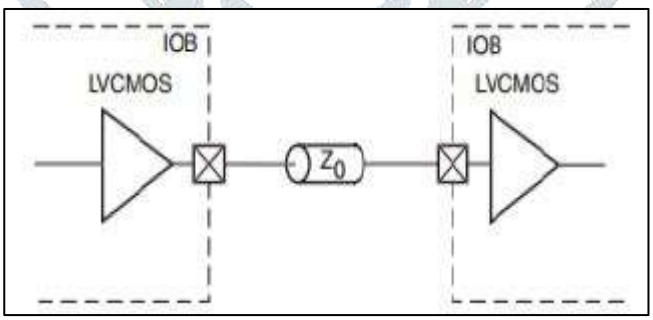

Fig.6 LVCMOS Buffer Schematic[7]

Fig.6 shows basic LVCMOS buffer schematic, in which only impedance is present. Different kind of termination topology is used for LVCMOS Standard, like unidirectional and Bi-directional termination topology. This figure shows unidirectional topology of termination[7].

III. IO STANDARD RELATED RESULTS

Beforeyoubegintoformatyourpaper,firstwriteandsavethecontentasaseparatetextfile.Keepyourtextandgraphicfilesseparateuntilafterthetexthas beenformattedandstyled.Donotusehardtabs,andlimituseofhardreturnstoonlyonereturnattheendofaparagraph.Donotaddanykindofpaginationanyw hereinthepaper.Donotnumbertextheads—thetemplatewilldothatforyou. This Section gives information about IO Standard related work done for memory designing. Different standards are used for the analysis of power consumption of memory on FPGA.

A. HSTL Standard:

HSTL class I IO standard is most power efficient at 1GHz frequency, among all other families of HSTL IO standard , for memory design on 28nm FPGA[2].At 1THz frequency, HSTL_II DCI is most power efficient , provides 59.03% power saving in comparison with HSTL_I_18. At 100GHz, HSTL_I_12 is the most power efficient , provide 56.93% power saving in comparison with HSTL_I_18. At 10GHz,

HSTL_I_12 is the most power efficient , provide 76.32% power saving in comparison with HSTL_II_DCI_18. At 1GHZ, HSTL_I is the most power efficient, provide 87.44% power saving in comparison with HSTL_II_DCI_18.

TABLE 1: Power Efficient HSTL Standard at Different Frequency[2]

Frequency Range	Most Power Efficient IO Standard	Power reduction in(%)	In comparison with	
1THz	HSTL_II_DCI	50.03	HSTL_I_18	
100THz	HSTL_I_12	56.93	HSTL_I_18	
10GHz	HSTL_I_12	76.32	HSTL_II_DCI_18	
1GHz	HSTL_I	87.44	HSTL_II_DCI_18	

B. LVCMOS12 and LVCMOS25:

RAM is implemented on Spartan 3E -90 nm FPGA[4]. They uses LVCMOS12V and LVCMOS25V IO family, with different frequency. Below table shows Power Consumption for LVCMOS25 IO Standard.

TABLE 2 : Power Consumption at LVCMOS25 [4]

Frequency	Clock Power	Leakage Power	Dynamic Power	Total Power
1THz	16.276	0.125	19.491	19.616
100GHz	1.628	0.118	1.949	2.067
10GHz	0.163	0.084	0.195	0.278
1GHz	0.016	0.081	0.019	0.101
100MHz	0.002	0.081	0.002	0.082
10MHz	0.000	0.081	0.000	0.081

When operating frequency is higher than 1GHz, we observed that power consumption is more with LVCMOS12 IO standard in comparison to LVCMOS25 IO Standard as shown in Fig.7. Therefore ,for higher frequency(GHz) one can use LVCMOS25 IO standard for memory design instead of LVCMOS12.

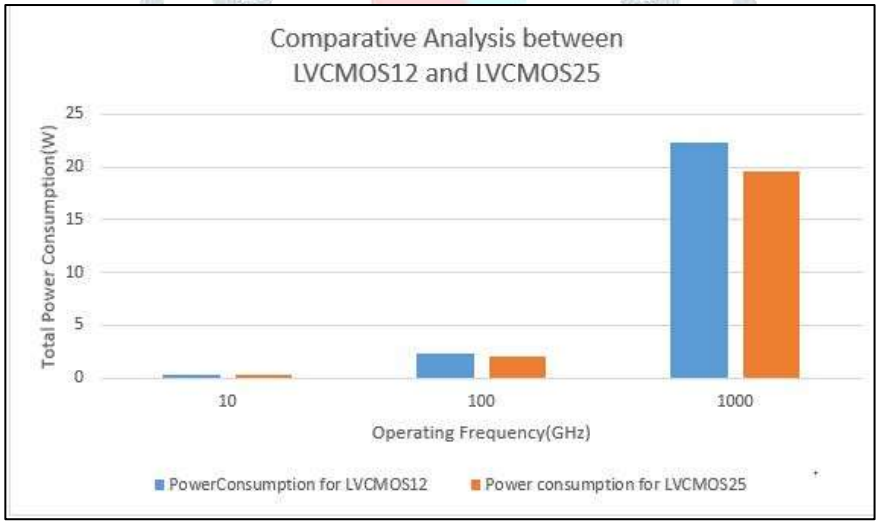

Fig7. Comparative Analysis between LVCMOS IO Standards at Higher Frequency[4]

Below table shows power consumption of LVCMOS12 IO standard at different operating frequency. It is observed that at lower frequency(MHz) total power consumption is less. At 1THz total power consumption is 22.370 W while at 10MHz total power consumption is 0.081 W.

TABLE 3 : Power consumption at LVCMOS12 [4]

Frequency	Clock Power	Leakage Power	Dynamic Power	Total Power
1THz	16.276	0.122	22.247	22.370
100GHz	1.628	0.122	2.226	2.349
10GHz	0.163	0.081	0.224	0.305
1GHz	0.016	0.078	0.004	0.082
100MHz	0.002	0.078	0.004	0.082
10MHz	0.000	0.078	0.002	0.081

From the below figure we can observed that, if ferequncy is in the range of several MHz like 100MHz then LVCMOS12 standard consumes less power then LVCMOS25 Standard. Therefore, if operating frequency is in the range of MHz then one should use LVCMOS12 IO Standard instead of LVCMOS25 for memory design.

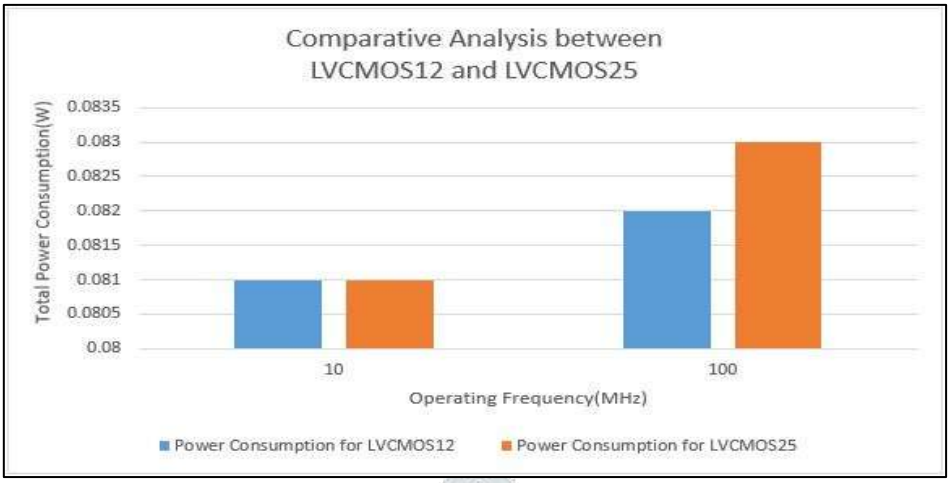

Fig.8 Comparative Analysis between LVCMOS IO Standards at Lower Frequency[4]

C. LVDCI and LVCMOS IO Standard in Comparison with other Standards:

RAM is designed on 40nm Virtex FPGA[7]. Different IO standards like LVCMOS, HSLVDCI, HSTL, LVDCI_DV2 and SSTL are used. Among these standards, LVCMOS and LVDCI_DV2 standard is more power efficient. Using LVCMOS , there is 94.28% power reduction in comparison with SSTL, 94.26% power reduction in comparison with HSTL and 32% power reduction in comparison with HSLVDCI[7]. Also using LVDCI_DV2 , there is 95.29% power reduction in comparison to SSTL, 27% power reduction in comparison to HSTL , 44% power reduction in comparison to HSLVDCI and 17.65% power reduction in comparison to LVCMOS. Therefore, By using LVCMOS or LVDCI_DV2 IO standard , power efficient RAM is designed on FPGA[7].

TABLE 4: Comparison of Power Consumption for LVCMOS and LVDCI_DV2 Standard with other Standards[7]

LVCMOS	**HSLVDCI**	**HSTL**	**LVDCI_DV2**	**SSTL**
17mW	25mW	296mW	14mW	297mW

As shown in above table, 17mW power is consumed if LVCMOS IO Standard is used while 14mW power is consumed if LVDCI_DV2 IO Standard is used, for memory design.

D. Power consumption of verious modules and parameters at different temperature:

Thermal ability and power efficiency of RAM is checked, by taking different temperature and different frequencies. First approach is, take a particular temperature value and take different frequency and measure the power dissipation for different modules like Clocks, Logic, IOs, BRAMs and parameters like signals and leakage, for your particular design[5]. Second approach is, take particular frequency and take different temperature values and observe the power consumption of above mentioned modules and parameters for your design. Below table shows the results of second approach.

TABLE 5: Power Consumption at Different Temperature[5]

Modules	12C	20C	35C	52C	75C
Clock	0.057	0.057	0.057	0.057	0.057
Logic	0	0	0	0	0
Signals	0.065	0.065	0.065	0.065	0.065
IOs	0.018	0.018	0.018	0.018	0.018
BRAMs	2.927	2.927	2.927	2.927	2.927
Leakage	0.52	0.566	0.807	1.029	1.029
Total	3.588	3.634	3.875	4.098	4.098

From this table we can conclude that if temperature is scaled down from 75C to 12C then leakage power consumption reduces from 1.029 W to 0.53W [5]. Therefore, Ultimately total power consumption reduces from 4.098 W to 3.588 W [5]. But there is no change in Clock, Logic, Signals, IOs and BRAMs.

E. Comparison between Mobile-DDR and LVTTL:

RAM is designed on 28nm Artix-7 FPGA by using different IO standards. To make it power efficient , firstly comparative analysis is done based on LVTTL and Mobile-DDR IO standard. Then we conclude that Mobile DDR is more power efficient IO standard then LVTTL. Result analysis shows that when we use Mobile DDR in place of LVTTL then 43% power is saved at 1GHz, 56% power is saved at 2GHz, 60% power is saved at 3GHz and 64% power is saved at 4GHz for IO block/port [6]. For total power consumption analysis, it is observed

that 28% to 47% power saving achieved when frequency increases from 1GHz to 4GHz, if LVTTL is replaced by Mobile DDR standard. Table 6 and 7 shows the power consumption at different frequency for both the above mentioned standards.

TABLE 6: IO Power Consumption with LVTTL Standard:[6]

Standard	1GHz	2GHz	3GHz	4GHz
LVTTL(W)	0.349	0.698	1.047	1.395

As shown in the above table, as frequency is scaled down from 4GHz to 1GHz then significant amount of power is saved. Therefore, it is better to use LVTTL at lower frequency when your application work with 3.3 voltage. LVTTL is used for 3.3 voltage applications.

TABLE 7 : IO Power Consumption with Mobile-DDR Standard:[6]

Standard	1GHz	2GHz	3GHz	4GHz
Mobile-DDR(W)	0.198	0.304	0.410	0.516

Above table shows that, if you scaled down the frequency from 4GHz to 1GHz then power consumption is less. Therefore, it is better to use Mobile-DDR IO standard if your application is work with 1.8 voltage. Mobile-DDR is used for 1.8 voltage applications.
Now, for the selection of better IO standard from LVTTL and Mobile-DDR , comparative analysis is done as shown in Fig.9. From this analysis we can conclude that at higher frequency(up to 4GHz) Mobile-DDR consumes less power then LVTTL.

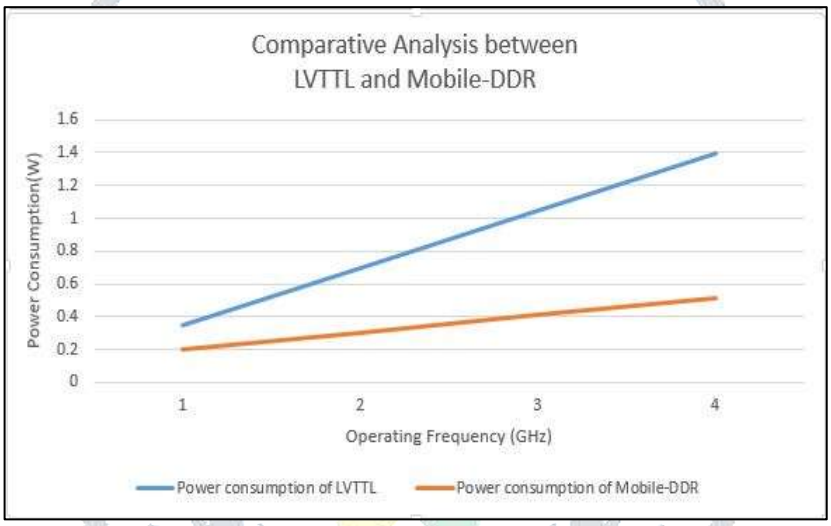

Fig.9 Comparative Analysis between LVTTL and Mobile-DDR IO Standard at Higher Frequency

IV. CONCLUSION AND FUTURE SCOPE

After this survey of IO standard technology, it is observed that various IO standards are power efficient for various FPGA devices. Also Power can be saved for memory design, if operating temperature decreases. Because if temperature decreases then power consumption also decreases. One can use any IO standard according to his/her design requirements(like low power design or high speed)with desired operating frequency. If power is concerned for designing then LVCMOS is better. Also Mobile DDR is better in terms of power in comparison with LVTTL. If speed is concern then HSTL family and Mobile-DDR is better.There is a scope to enhance this analysis for better performance of SRAM on FPGA. Comparative analysis will be done for HSTL family and Mobile-DDR for future work. This analysis will be done ,at desired operating frequency to identify which one is better for power efficient SRAM design or which one is better for speed efficient SRAM design.

ACKNOWLEDGMENT

I would like to thank my project mentor Mr. Tarun Agrawal for his technical support. Also I would like thank my college internal guide Mrs. Shivi Shukla for her motivation and encouragement for this survey.

REFERENCES

[1] M. Stephen,"Three Ages of FPGAs: A Retrospective on the First Thirty Years of FPGA Technology ", Proceedings of the IEEE, USA, vol. 103, No.3, March 2015.

[2] Sweety, B. Pandey, T. Kumar and T. Das, "Design of Power Optimized Memory Circuit Using High Speed Transreceiver Logic IO Standard on 28nm Field Programmable Gate Array ", IEEE International Conference on Reliability, Optimization and Information Technology-ICROIT,India, February 2014.

[3] J. Moore and M. Stephen, "FPGAs Security: Motivations, Features and Applications," Proceedings of the IEEE, vol. 102, No.8 August 2014.

[4] D. Singh, B. Pandey and M. Pattanaik ,"IO standard based Low Power design of RAM and Implementation on FPGA," Journal of Automation and Control Engineering, vol.1, No.4, December 2013.

[5] G. Verma, M. Aditi, B. Pandey, "Thermal and Power Aware Internet of things enable RAM design on FPGA," IEEE 2nd International Conference on Computing for Suitable Global Development, New Delhi, INDIA, March 2015.

[6] A. Kumar, G. Sharma, T. Agrawal and D. Agrawal, "A Designing of Random Access memory using Different IO standard Technology," ICCCNT,TX,USA, July 2016

[7] R. Kaur, J. Kumar and S. Nagah, "IO standard based Low Power Memory Design and Implementation on FPGA," IEEE 2nd International Conference on Computing for Suitable Global Development, New Delhi, INDIA, March 2015.

[8] A. Pathak, D. sachan, "A modified SRAM based Low Power Memory Design", 29th IEEE International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID),4-8 January, 2016

[9] M. Bansal, R. Saini and N. Bansal, "HSTL I/O Standard Based Environment Friendly Energy Efficient ROM Design on FPGA", IEEE 2nd International Conference on Computing for Sustainable Global Development (INDIACom), New Delhi,INDIA,March,2015

[10] M. Bansal, R. Saini, B. Pandey and Hussain "SSTL I/O Standard Based Environment Freiendly Energy Efficient ROM Design on FPGA", Proceedings of the 3rd Intrnational Symposium on Environment-Friendly Energies and Applications, Paris, France, 2014

[11] M. Stephen,"FPGA Secutiry: Motivations, Features and Applications", Proceedings of the IEEE, USA, vol. 102, No.8, March 2015.