FPGA BASED RISC PROCESSOR WITH INBUILT AUTO TUNED PID CONTROLLER FOR DRUM BOILER FEED WATER CONTROL

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Abstract:- In the field of real-time signal processing, like most of automatic control systems nowadays present at the industry and focused on PID (Proportional-Integral-Derivative) controllers, it is common to find software-oriented solutions based on powerful 32-bit DSP, RISC or CISC processors. This work deals with the hardware/software co-design of a PID coprocessor, all embedded on a system-on-chip device. The performances reached by a platform composed of an 8-bit MCU and a dynamically reconfigurable FPGA allow scheduling the PID algorithm as a set of tasks executed by both devices concurrently. Moreover, thanks to the flexible hardware characteristics, some modules synthesized into the FPGA are reconfigured at run-time while the rest keeps on active. This cost-effective approach, encouraged by its parallelism, is an alternative to commercial –both general-purpose and specific-purpose–processors in whatever made-to-measure engineering application. This paper deals with implementation of RISC processor having inbuilt auto tuned PID controller for Drum Boiler Feed Water Control.

Keywords: - RISC Processor, Auto tuned PID Controller, Feed Water Control, Simulink

I INTRODUCTION

FPGA- Field Programmable Gate Array; it is an integrated circuit designed and configured by a customer or designer after manufacturing hence called "Field Programmable". The specification of configuration is normally done by using Hardware Description Language (HDL). It contains Logic Components which are programmable called Logic box and it has the ability to interconnect that cell or blocks to be wired together. It contains over 10000 logic cells. The individual cells are interconnecting by a matrix of wires and programmable switches

RISC stands for Reduced Instructions Set Computer (RISC). It is a processor which uses only simple instructions, which performs low level operation in a single clock cycle. It has a very high performance capacity and capable of executing those instructions in a single microprocessor cycle. It has advantage of having pipelining therefore multiple instructions can execute in a single clock cycle. This results in high speed instruction execution. It also has Load/Store architecture where memory is accessed through particular instructions. It also has a simple Arithmetic Logic Unit (ALU) for basic operations with simple and uniform instruction set. This work presents the design of reconfigurable 8 bit RISC processor. The fig. No. 1 and 2 shows Block diagram of 8 bit RISC processor and RTL view of 8 bit RISC processor. The basic modules of this processor are programmed by using Verilog Hardware Description Language (VHDL), it is then verified the simulation result using XILLINX ISE 14.2 tool.[1]

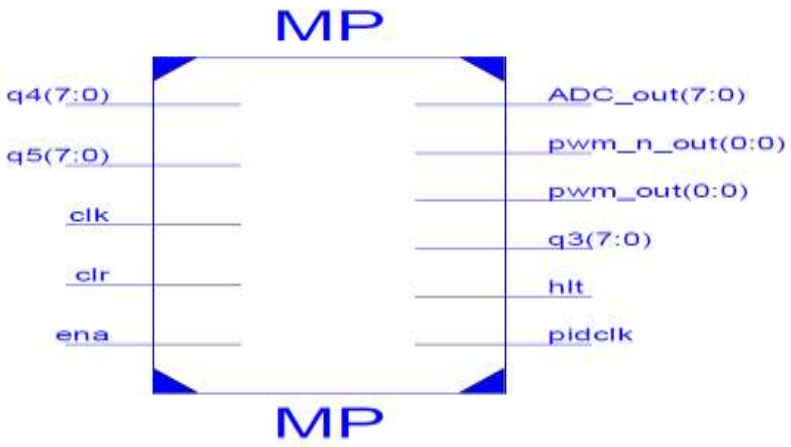

Fig 1:- Block diagram of RISC processor

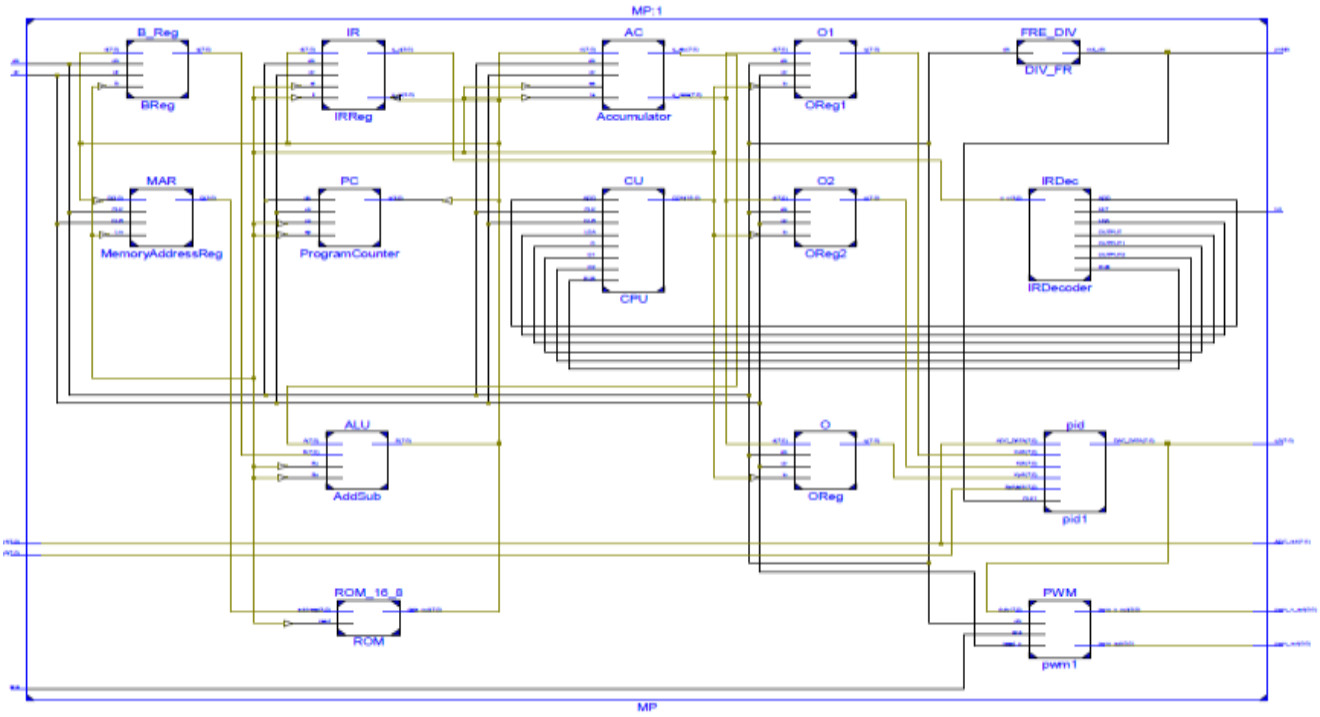

Fig 2:- RTL schematic of implemented RISC processor.

The fig. no. 2 shows the RTL view 8 bit RISC processor. It contains Central Processing Unit (CPU), Read Only Memory (ROM), Arithmetic and Logical Unit (ALU), Accumulator (A Register), B Register, Instruction Register (IR), Instruction Register (IR) Decoder, Memory Address Register (MAR), OUT Register, Frequency Divider and Supporting Peripherals for RISC processor like Proportional-Integral-Derivative (PID) controller, Counter, Pulse Width Modulation (PWM), and Universal Asynchronous Transfer Receiver (UART) [2].

II Drum boiler feed water control

The primary function of feed water control is to maintain drum water level at the desired set point. In this simplest form one can visualize the process of defining drum level as a simple integration of water flow in to the boiler, less than steam flow out of the drum. The gain of integration is readily calculated from the mass of water that is held for each inch of water level around the normal operating level.

Since the primary disturbance originates from changes in steam flow, it is logical to structure the control such as to make feed water flow follow steam flow, and use to deviation in level as a slow resetting action to bring the required water inventory back to balance. The use of feed water steam flow and level as inputs to the control action gave rise to the term '3 element control'. From a hierarchical point of view, it is convenient to think in terms of a feed water sub loop control, whereby feed water flow is made to follow a feed water demand. This demand in turns is derived from steam flow (feed forward primary signal) and a correcting signal from a controller operating on drum level error.

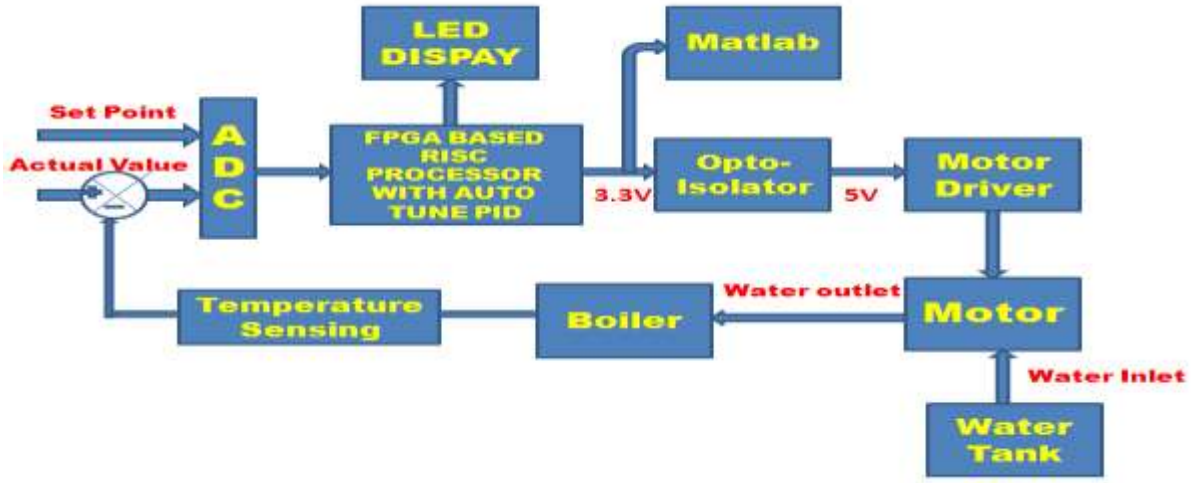

Fig. 3:- Block Diagram of Drum boiler feed water control system using Auto tune PID.

III Hardware Implementation:-

- FPGA based RISC processor with auto tune PID
- Opto-Isolator
- Motor Driver
- AC Induction Motor
- Water Tank

- Boiler
- Temperature Sensor

For the operation of drum boiler feed water control, the variable frequencies are Generated by the FPGA based RISC processor by using PWM application. Those variable frequencies are applied to motor through motor driver (L239D). As this is closed loop system, the frequency changes as error between actual value and set value is increased or decreased.

The above system consists of two potentiometers, one for the set point and another is for to adjusting the actual value coming from feedback. The difference between these two values are given to the Analog to Digital Converter (ADC), because the FPGA requires the digital input values but set value and actual value are the analog signals therefore, to convert analog values to digital values the PIC 18F4520 is used. It receives analog signals from the potentiometers and converted those values in to digital and gave to the FPGA. The FPGA based RISC processor contains the auto tune PID controller which is used for this process control application. For the implementation of RISC processor with auto tune PID the Numato FPGA sparten6 board (XC6SLX9) is used. By using Xilinx 14.2 web pack and i-sim simulator all system implementation is done. In this RISC processor, by setting the PID values for the single time, the PID controller controls the whole system for any change in the difference between set value and actual value. The FPGA based RISC processor receives the digital inputs from the ADC and based on those values the auto tune PID controller present in the RISC processor controls the system. The output of the PID controller is displayed on the matlab. By designing the simulink in the matlab, the current output of auto tune PID controller is observed in the matlab and at a same time the output of PID controller given to the motor driver circuit through opto-isolator. The optical isolator provides isolation between the outputs of RISC processor which is 3.3V and input of motor driver IC which is 5V.

As difference between set point (set temperature) and actual value (output of the temperature sensor) varies the PID controller varies the speed of the motor. As speed of the motor varies the motor feeds more water from the water drum to the boiler. The speed of the motor also depends on the boiler temperature. As boiler temperature increases which are sense by the temperature sensor that also increases therefore the difference between set and actual temperature are increases. Depending on this the speed of the motor varies to feed the water from the drum to the boiler to maintain desired temperature level of the boiler.

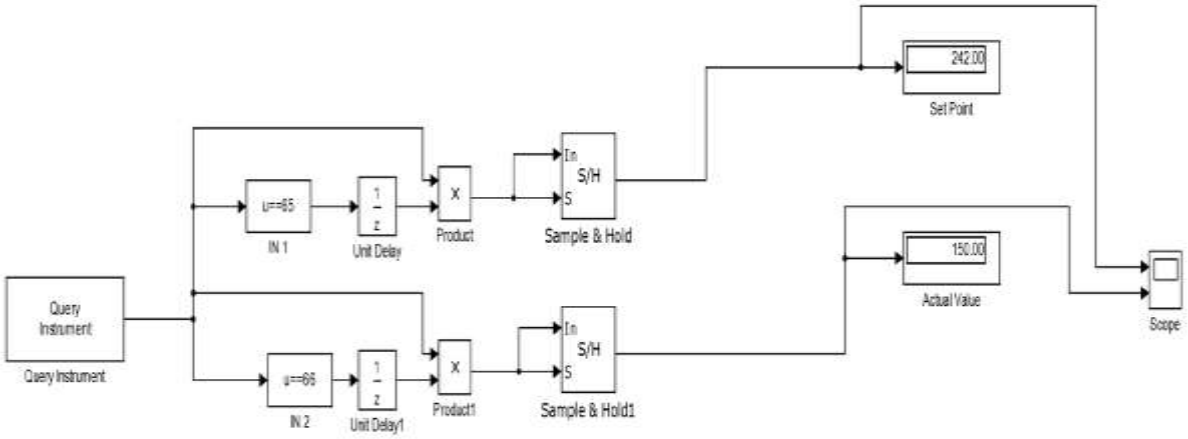

Fig. 4:- Simulink design for Drum boiler feed water control system using Matlab.

The above simulink designed in the Matlab 7.9 to observe the real time output of auto tune PID controller. In this the query instrument reads the real time output value of PID. As shown in fig. 2 the two displays are used to display real time set point and actual value and the block scope displays the waveform of the real time PID controller's output.

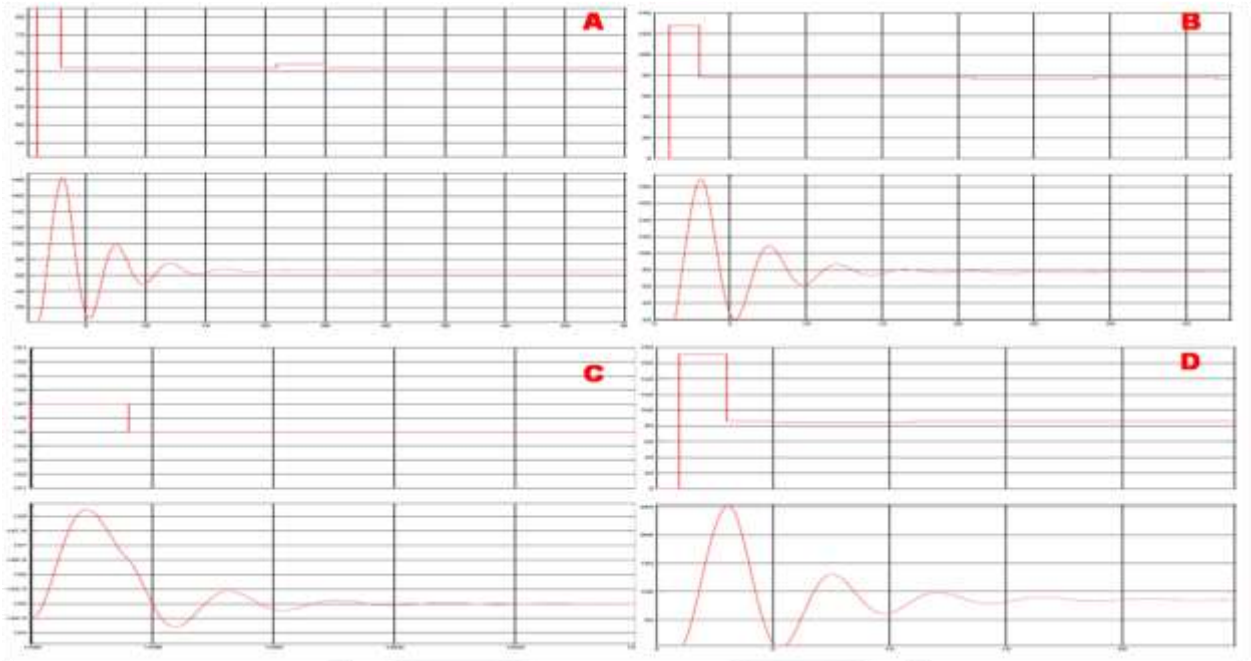

Fig. 5:- Real time output Wave forms with different set points and actual values in Matlab.

Sr. No.	Figure	Set Point	Actual Value	Rise Time (Sec)	Peak Time (Sec)	Settling Time (Sec)	Peak Overshoot %
1	A	123	58	0.9	2	14	5
2	B	128	50	0.7	3	14.5	5
3	C	160	15	0.8	2.5	15	5
4	D	170	84	1	2.2	15.5	5

Table 1:- Real time Output of Auto tuned PID controller with various set points and actual values in Matlab

The table no. 1 shows that the different set points and corresponding actual values. Depending on these values the output of auto tune PID controller varies.

IV Conclusion

The present paper deals with the design of FPGA based 8 bit RISC processor with PID controller for Drum Boiler Feed Water Control. The basic modules of this processor are programmed by using Verilog Hardware Description Language (VHDL), it is then verified the simulation result using XILLINX ISE 12.4 tool. The present 8 bit RISC processor performs the controlling action of drum boiler feed water control for sugar cane industry. It concludes from the table no 1 that, the settling time increases as increase in set point

V REFERANCES

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