IMPLEMENTATION OF ULTRA HIGH SPEED MULTILAYER ADDER LOGIC DESIGN USING QUANTUM-DOT CELLULAR AUTOMATA

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Abstract: ***Quantum-dot cellular automata, is among the most promising nanotechnologies for the alternative substitute to current Metal Oxide Semiconductor Field Effect Transistor (MOSFET) based devices. This technology promises of high switching speed, low power consumption and high device density in comparison to traditional CMOS technology. Several combinational and sequential logic circuits have been proposed using QCA. Therefore, lots of attention has been paid to design digital arithmetic QCA circuits. Adder circuits are the most widely investigated and analyzed, because adder operation can directly affect the performance of the digital system. In this paper, a new multilayer ultra-high speed QCA full adder circuit is proposed using single layer OMG and m-RMG gates, which computes Sum and Carry bits, respectively. The proposed adder circuit consists of less area, less circuit complexity and reduced clock delays. In addition, ultra-dense new 4-bit & 8-bit ripple carry adder circuits have been proposed using the presented one-bit multilayer adder circuit. Detailed structural analyses are performed in different aspects to authenticate the proposed adder circuit has achieved significant improvements in comparison to traditional approaches. QCADesigner tool Ver. 2.0.3 is used to verify the correct circuit functionality.***

Keywords: Nanotechnology, OMG and m-RMG, Multilayer, Full Adder, Ripple Carry Adder.

1. Introduction

The continuous scaling down of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices has lead to various short channel effects such as Sub-threshold Slope (SS) degradation, Drain Induced Barrier Lowering (DIBL) effect, threshold voltage roll-off. The dimensions of transistors shrinks, the close proximity between the source and the drain, reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region. Therefore, undesirable effects called the "short-channel effects (SCE's)" starts plaguing MOSFETs. For all practical purposes, it seems impossible to scale the dimensions of classical "bulk" MOSFETs below 20nm due to various SCE's that impinge the device characteristics [1].

Therefore, new alternative technologies are introduced as possible solutions to overcome the occurred problem in MOSFETs devices. Quantum-dot Cellular Automata (QCA) by neglecting the conventional transistor based technologies has attained considerable worldwide attentions due to its attractive characteristics such as ultra-high speed (THz), high device density, and low power consumption [2-3]. The basic building block of QCA circuit is majority gate; hence, efficient constructing QCA circuits using majority gates has attracted a lot of attentions, but some of them are not expandable [4-15]. Since every QCA, circuit can be implemented using majority and inverter.

Several studies have been reported about combinational circuit design, such as QCA Full Adder [4-16]. By connecting 'n', such one-bit QCA full adders, a carry look ahead (CLA) adder can be obtained. Initial adder designs were constructed with five majority gates (a fundamental QCA logic gate) and three inverters. However, the current trend on QCA designs has been changed using recreantly a new three-input Exclusive-OR (TIEO) gate [17]. This gate is simple in design and consists of fewer cells. Therefore, several new adder circuits have been proposed [17-23]. Exclusive-OR (XOR) is one of the most fundamental logical gate used in arithmetic circuits to compute sums.

In this paper, OMG [3], and m-RMG [2] have been used to design a new multilayer adder circuit. The proposed adder circuit consists of less area; reduced circuit complexity and latency. A detailed comparison with regard to various characteristics of proposed and conventional adder design is presented. The proposed adder circuit has achieved significant improvements in comparison to conventional adder designs. The functionality of the proposed full adder design has been testified to design a new 4-bit ripple carry flow adder circuits. All circuits have been verified to design a novel adder circuit.

2. QCA fundamental background

2.2 QCA cell structure

A basic QCA cell is shown in Fig. 1, each basic QCA cell consist of four quantum dots positioned at each corner of a square shaped cell and a pair electrons which able to tunneling in any quantum dots in each cell. Due to the columbic interaction between electrons, only two configurations exist for the electrons in the cells. In other words, only there are two models in each cell which their polarizations are designated as +1 and -1 and is symbolized by binary values of "1" and "0"[2,3].

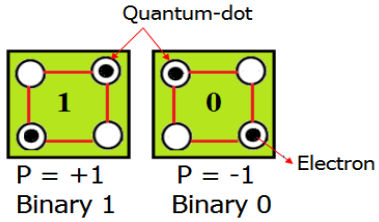


Fig. 1.QCA cell and two possible polarizations.

2.3 QCA wire structure

In Fig. 2 structure of 90-degree QCA wire is shown. In general, in order to implement QCA wire we need a number of cells, which we must inject a logical value in the input cell and after some delays this value propagates through the wire and finally at the output cell due to the electrostatic energy between cells [2,3].

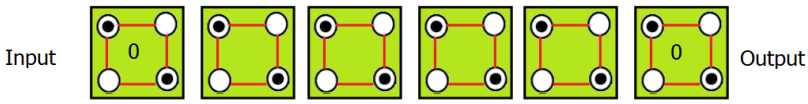


Fig. 2.90-degree QCA wire.

2.4 Inverter

Fig. 3 illustrates a QCA inverter gate. A random logical value could be injected at the input cell and the inverted logical value is accessible at the output cell [2,3].

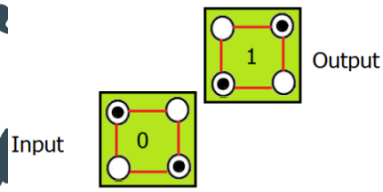
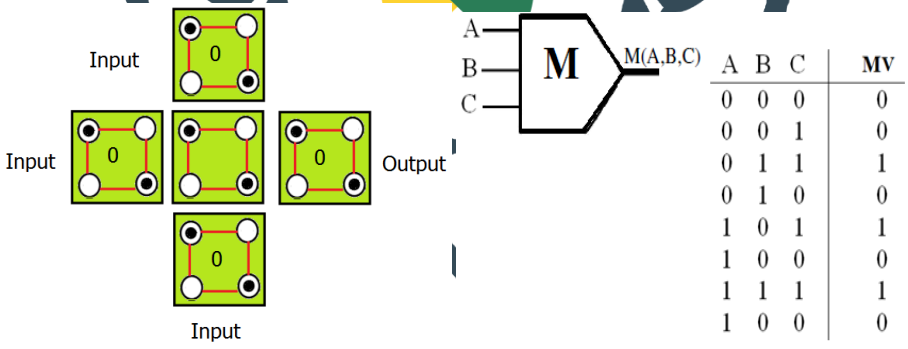


Fig. 3.QCA inverter.

2.5 Majority gate (MG)

In conventional QCA designs, three-input majority gate (MG); combination of 5-cells has a significant role in general circuit architecture. Fig. 4 illustrates the truth table; symbol representations and QCA three-input majority gate with three inputs of A, B, and C.

The logical output function of three-input MG gate is determined as MG = AB+AC+BC.



A	B	C	MV
0	0	0	0
0	0	1	0
0	1	1	1
0	1	0	0
1	0	1	1
1	0	0	0
1	1	1	1
1	0	0	0

Fig. 4.QCA three-input majority gate.

Therefore, circuit complexity and clock delays are the major issues in the QCA area and is associated with cell counts of any circuit. Keeping in view of these issues, new multi-input majority gates have been designed by researchers [7]. In Fig. 5, three five-input majority gates are displayed.

The logical output function of a five-input MG gate is determined as:

MG (A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE (1)

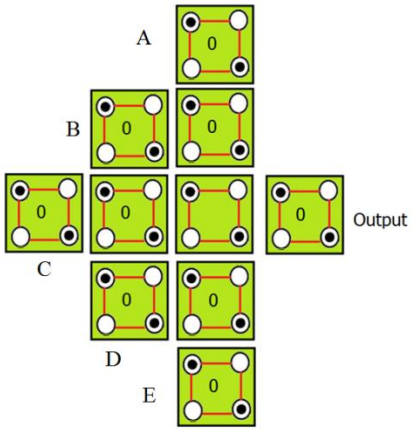


Fig. 5. Five-input majority gate (a) five-input majority gate in [7]

2.6 QCA clocking

QCA clocking zones is shown in Fig. 6. The QCA clocking consists of four zones. Clocking of QCA can be controlled by potential barrier energies between neighboring quantum-dots [24].

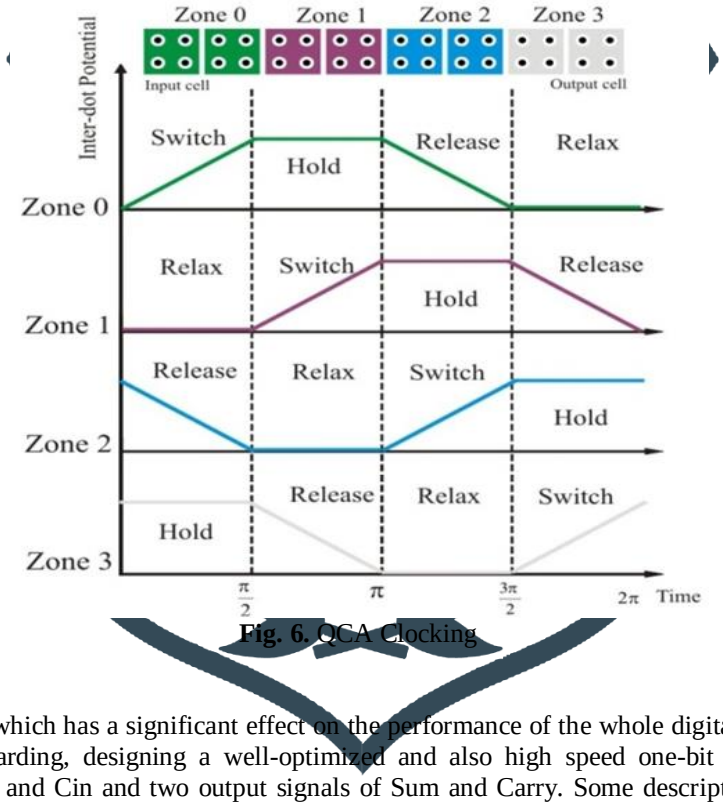


Fig. 6. QCA Clocking

3. Previous works

The basic unit in an arithmetic circuit which has a significant effect on the performance of the whole digital system is a one-bit full adder. Many researchers have been conducted regarding, designing a well-optimized and also high speed one-bit full adder. One-bit full-adder cell is constructed with three inputs of A, B, and Cin and two output signals of Sum and Carry. Some descriptions for Sum and Carry of full adder based on inverter and majority gate have been provided below section.

3.1. Majority gate-based designs for Full adder cell

One-bit full adder cell is one of the main components of arithmetic circuit and to date many designs have been proposed. The first design has been proposed by Tougaw et al. in the year 1994 based on five three-input majority gates. As is illustrated in the Fig. 7, this design is constructed by the mentioned majority gates and also only three inverter gates have been employed in this design [3]. This design got a huge attention from scientists to implement in the QCA area. Sum and Carry outputs has been calculated as:

Let us consider A, B, and Cin as the full adder inputs, majority gate based Carry can be achieved as follow:

$$Carry = M(A, B, C_{in}) \quad (2)$$

Therefore, Sum [3] expression is expressed as:

$$Sum = MV\left(MV\left(A, \overline{B}, C_{in}\right), MV\left(A, B, \overline{C_{in}}\right), MV\left(\overline{A}, B, C_{in}\right)\right) \quad (3)$$

As it is clear, a precise addition using this full adder requires five three-input majority gates and three inverters are required.

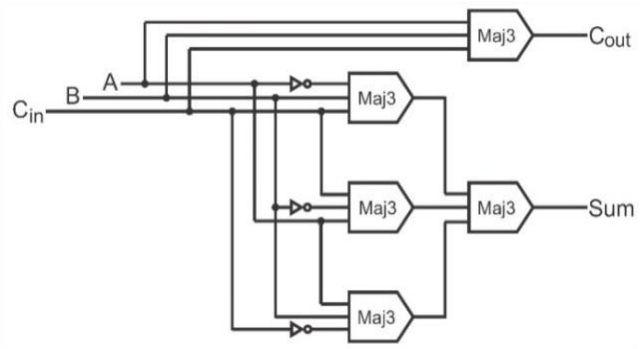


Fig. 7. First majority gate-based architecture for full adder cell in [3]

3.2. Three-input Exclusive-OR Gate

Three-input Exclusive-OR gates are implemented using the concatenation of two 2-input XOR gates. The main focus of these implementations is to reduce circuit complexity and increase efficiency. New logical wire crossing approach has been utilized to design three-input XOR gate [27]. It is constructed using two majority gates (one three-input and one five-input majority gates) as shown in Fig. 8(a). Another, three-input Exclusive-OR presented in [28] has been constructed using two 2-input XOR gates as shown in Fig. 8(b). However, sill research is continuous due to the current constraints of cell counts, clock delays and area occupation. Recently, a new 3-input XOR (TIEO) is proposed in [17], has an influential role in overall circuit performance in terms of area occupation, clock delays, and cell counts as compared to [27-28]. It is implemented using explicit QCA cell approaches with less latency lock delays as shown in Fig. 8(c).

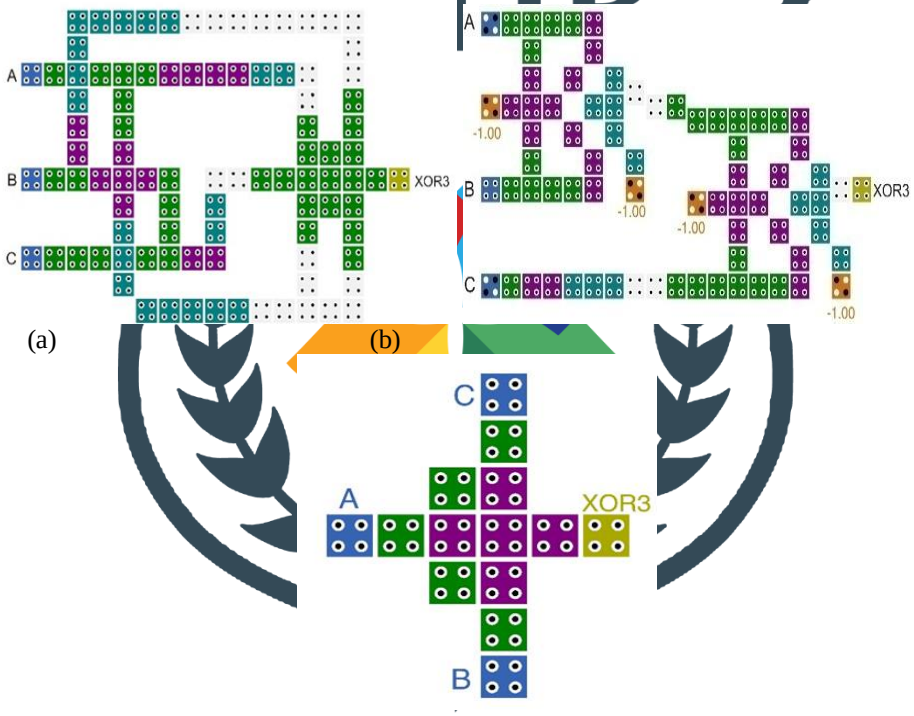


Fig. 8.(a) Three-input XOR gate in [26] (b) Three-input XOR gate in [27] (c)Three-input XOR (TIEO) gate using explicit interaction presented in [17].

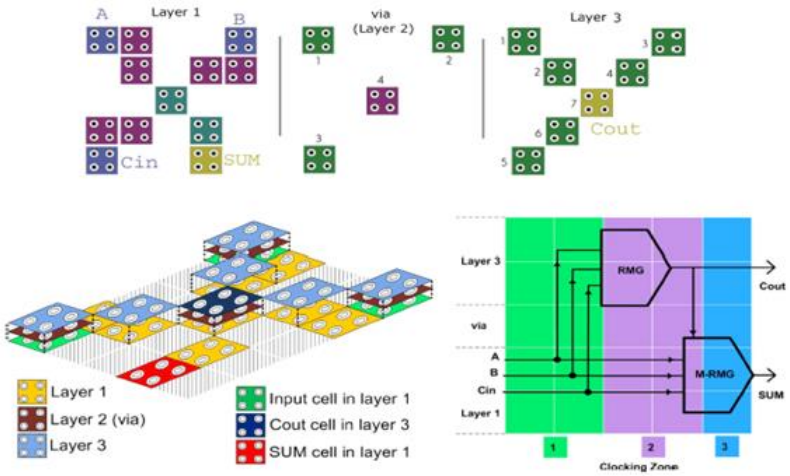
4. The Proposed Method

4.1. The Proposed 1-bit Adder

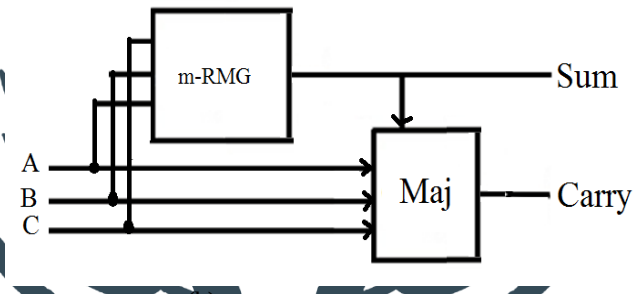
A new 1-bit multilayer full-Adder circuit has been implemented using OMG [3], and m-RMG [2]. In this paper, we have enhanced conventional multilayer full-adder circuit, shown in Fig. 9(a). This modification leads to increases the stability of conventional adder circuit during manufacture IC fabrication. We add some additional cells, besides replaced m-RMG gate with OMG gate, which computes sum bits and RMG with m-RMG gate that compute, carry bits. This adder design [2] has a difficulty using both rotating gates to compute sum and carry bits. Rotating cells are easily affected with low robustness and fabrication difficulties in QCA circuits [29-30]. The main focus of our design is make circuits less complex and produces strong coulombic coupling in QCA cells [29]. In our proposed design sum bits has been computes using standard wire (90-degree) OMG gate [3]. QCA technology can be ever going to challenge the current IC fabrication defects due to small geometry of QCA cells. Therefore it is necessary to resolve the interconnection and coupling problems using single layer standard wire mechanisms based gates (90-degree) very efficiently [3, 29]. This wire has a very high robustness at nano-scale and scalable solution as compared to other wire crossing mechanisms for design logic circuits.

The schematic representation of the proposed multilayer full-adder circuit has been shown in Fig. 9(b). The QCA layout of the proposed multilayer 1-bit full-adder circuit is shown in Fig. 9(c). It is basically implemented using single OMG [3] in concatenation with single modified-Rotating Majority Gate (m-RMG) [2]. The m-RMG is used to compute the Carry-bits. The simulation result of the proposed full-adder is shown Fig. 9(d).

Three layers have been used to construct the proposed Full-Adder circuit. The first layer (layer-1) is the major layer of the Full-Adder, in which three inputs (A, B, C) are applied with clock phase 1 to transmit the input signal to the first Original Majority gate (OMG), which computes the output (Sum-bits) as shown in Fig. 9((e). The second (layer-2) is the middle layer of the Full-Adder which acts via contacts Fig. 9(f), in which input signal is transmitted from first layer to third layer. The third layer (layer-3) conveys the input signals (A, B, C) to the clock phase 0. The m-RMG is used to compute the output (Carry-bits), in which clock phase 0 is used to calculate Carry-bits as shown Fig. 9(g). Therefore, two clock phases have been used to design 1-bit Multilayer Full-Adder. The proposed circuit consists of reduced, area, circuit complexity and clock delays. Circuit complexity (cell count) and clock delays are the main challenge for circuit performance. The design has lesser area of 0.02 μm^2, with the circuit complexity of 30 QCA cells and latency of 0.5 clock cycles.



(a)



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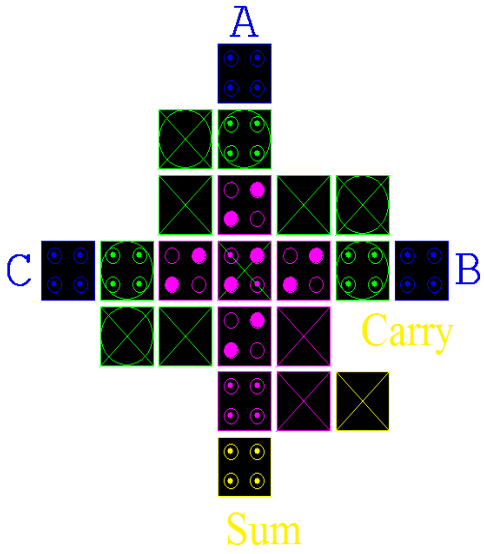

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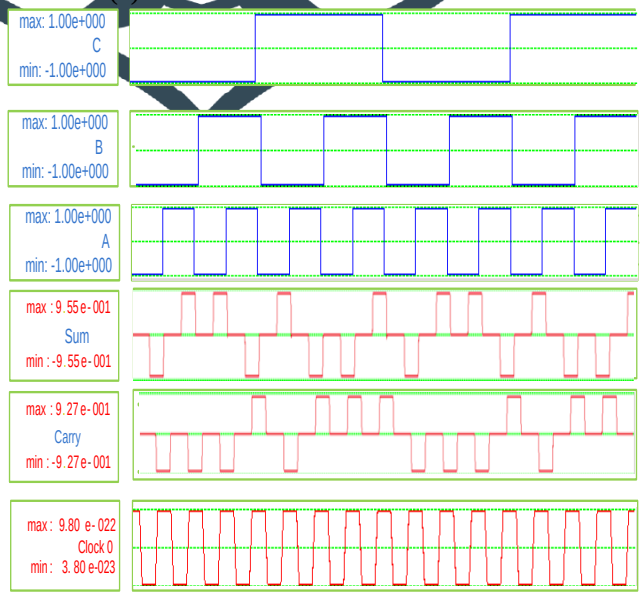
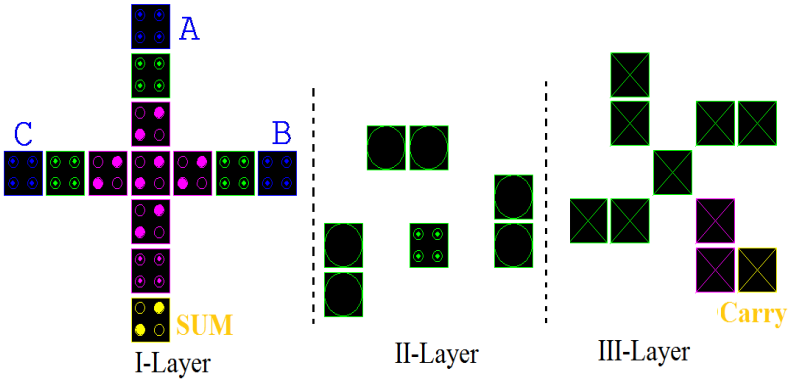


(d)



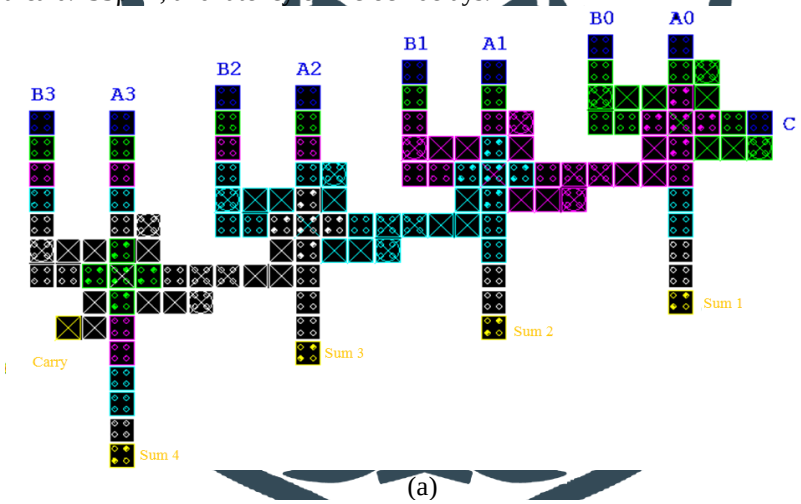
(e) (f) (g)

Fig. 9:(a) Schematic representation of Full-Adder (b) The QCA layout Adder (c) The simulation results (d) The layer-1 (e) The layer-2 (f) The layer-3

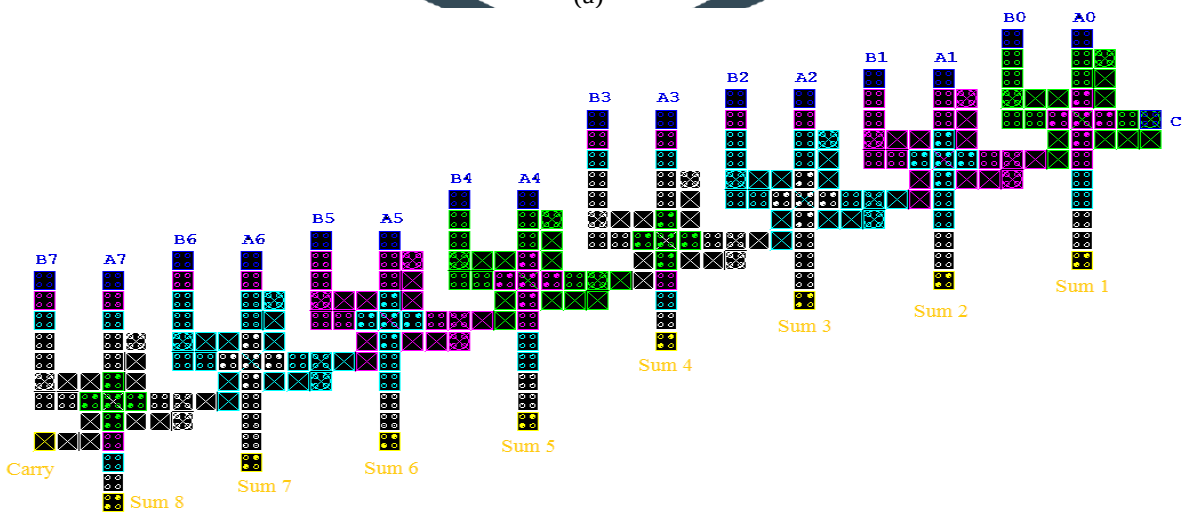
4.2. The Proposed 4-bit Adder

The QCA layout of the proposed 4-bit Ripple Carry Adder (RCA) is shown in Fig. 10(a). In the first layer A3–A0 and B3–B0 and Cin indicate the input cells and Sum4–Sum1 labels represents the Sum-output signal. Second layer acts as via contacts in which the input signal is transmitted into the third layer. The third layer is the calculation layer which computes Carry-outputs (indicated by Cout). The proposed circuit has circuit complexity of 173 QCA cells, an area 0.25μm^2, and latency of 1-clock delays.

The QCA layout of the proposed 8-bit Ripple Carry Adder (RCA) is shown in Fig. 10(b). In the first layer A7–A0 and B7–B0 and Cin indicate the input cells and S8–S1 labels represents the Sum-output signal. Second layer acts as via contacts in which the input signal is transmitted into the third layer. The third layer is the calculation layer which computes Carry-outputs (indicated by Cout). The proposed circuit has circuit complexity of 343 QCA cells, an area 0.155μm^2, and latency of 2-clock delays.



(a)



(b)

Fig.10: (a) The QCA layout 4-bit Adder (b) The QCA layout 8-bit Adder

5. Simulation results and Performance Evaluation

5.1 Simulation and Discussion

The proposed multilayer 1-bit adder and the proposed 4-bit & 8-bit Ripple Carry Adders have been simulated using the QCADesigner version 2.0.3 tool [30]. All of the simulation parameters and conditions are adopted as the default values. The circuit parameters and conditional areas are asserted in Table 1.

Table 1. Bistable approximation and coherence vector parameters.

Parameters	Bistable Approximation	Coherence Vector
Cell size	18 nm	18 nm
Layer separation	11.5 nm	11.5 nm
Clock low	3.8e−023 J	3.8e−023 J
Clock high	9.8e−022 J	9.8e−022 J
Clock shift	0	0
Clock amplitude factor	2	2
Relative permittivity	12.9	12.9
Radius of effect	65 nm	80 nm
Number of samples	50000	---
Convergence tolerance	0.001	---
Maximum iterations per sample	100	---
Temperature	---	1 K
Relaxation time	---	4.1356675e−14 s
Time step	---	1e−016 s
Total simulation time	---	7 e−011 s

5.2 Performance Evaluation

A new multilayer full adder circuit using OMG [3] and m-RMG [2] has been proposed in this paper. Here we have developed an extensive structural analysis in different aspects (Area, Cell Count& Clock delays) of full adder structures previously published in literatures [5-15] and our proposed design. The clock delays, complexity (cell count) and area are in comparison factors. Table 2, depicts the significant improvements in our proposed design in terms of circuit parameters. Accordingly, ultra-dense 4-bit& 8-bit ripple carry adder circuits have been proposedenjoying the proposed adder circuit.

The graphical comparison of the proposed full adder designs is illustrated in Fig. 11. The performance comparison parameters including area, clock delays and cell counts. The performance of the proposed design is superior in terms of clock delays as initiated by solid lines in comparison to [5-15]. However, it is observed in reference [9-11] consists of less area as compared to proposed design. But, in contrast, our adder design has less complexity and clock delays in comparison to [9-11]. In brief, the performance of the proposed multilayer one-bit adder designs is more superior in comparison to [5-15].

Table 2. Structural analysis of the one-bit full adders

Circuit	Area (μm^2)	Cell Count	Latency (Clock Delays)
Our Design	**0.02**	**30**	**0.5**
Ref. [2]	0.01	23	0.5
Ref. [5]	0.04	52	0.75
Ref. [6]	0.04	56	0.75
Ref. [7]	0.043	59	1
Ref. [8]	0.05	63	0.75
Ref. [9]	0.04	73	0.75
Ref. [10]	0.05	79	1.25
Ref. [11]	0.10	86	0.75
Ref. [12]	0.14	105	0.75
Ref. [13]	0.10	108	1
Ref. [14]	0.17	145	1.25
Ref. [15]	0.62	292	3.5

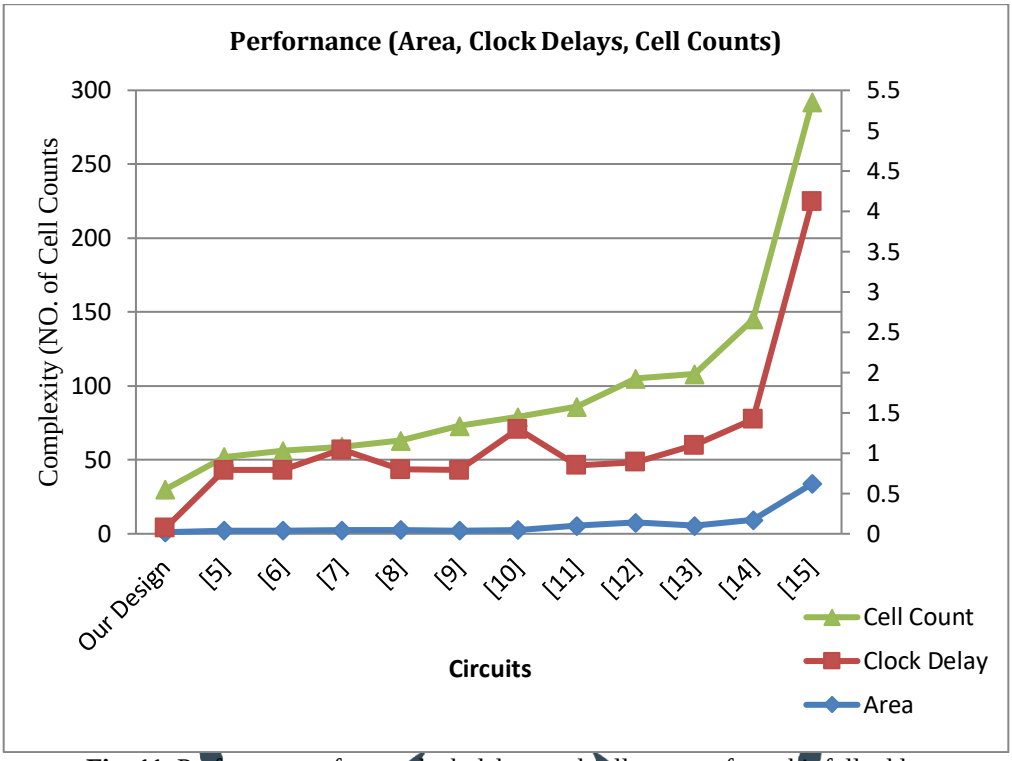


Fig. 11. Performance of area, clock delays and cell counts of one-bit full adder

6. Conclusion

In this research work, a new multilayer one-bit adder circuit using OMG and m-RMG gates has been proposed. The proposed adder circuit exploits the advantages of various circuit parameters in terms of area, clock delays and cell counts at nano-scale. The proposed adder circuit has been testified to design new well-optimized 4-bit & 8-bit ripple carry full adder structure for QCA. The proposed one-bit full adder circuit has been comprehensively compared to the previous proposed adder circuits available in the literature. It is inferred from the results that our proposed one-bit adder demonstrated the significant improvements in terms of circuit parameters. The design and simulation results of the present work have been verified using QCADesigner tool ver. 2.0.3.

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