DESIGN AND ANALYSIS OF 64 BIT MIPS PROCESSOR

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Abstract: ***This research paper presents design and implementation of a five phase pipelined 64-bit Microprocessor without Interlocked Pipeline Stages (MIPS), which is a type of Reduced Instruction Set Computing (RISC) based processor. The reason for RISC is to execute an smaller group of instructions one at a time, where CISC processor uses complex instructions to execute. This MIPS processor was composed with five phases of pipeline specifically Instruction Fetch (IF), Instruction Decode& Register Fetch (ID), Execution& Address Calculation (EX), Memory Access (MEM) and Write Back (WB) modules. The outlining procedure was finished utilizing a bunch of modules which are the ALU, Control Unit, Program Counter, MUX, Instruction Memory, Data Memory, CPU, Register File, Sign Extension. The main goal of this MIPS processor is to perform multiple instructions in a single clock cycle at a time and it is verified in the Hardware Description Language (HDL) - Verilog in Xilinx 14.3 system.***

Keywords- MIPS, RISC, Verilog, Xilinx.

I. INTRODUCTION

For the most part Microprocessors and Microcontrollers are all things considered made in the area out of two rule PC outlines: Complex Instruction Set Computing i.e. CISC and Reduced Instruction Set Computing i.e. RISC outline. The possibility of CISC relies upon Instruction Set Architecture (ISA) and it is intended to rearrange compilers errand. CISC can execute multi-step tasks, fundamentally PCs based CISC structures are intended to diminish the memory cost.

Be that as it may, when all is said in done extensive projects require more stockpiling and expansive memory ends up costly. So to tackle these issues the quantity of directions per program can be lessened by installing the quantity of activities in a Single direction there by influencing the guidelines to make more perplexing. Differentiated and their CISC basic, RISC processors consistently bolster an infinitesimal course of action of directions. RISC processor with CISC processor, the amount of rules in a RISC Processor is low while the amount of all around valuable registers, watching out for modes, settled guideline length and load-store configuration is more this accordingly supports the execution of directions to be done in a concise traverse thus achieving higher execution.

Execution of a Five-organize pipelined 64-bit High execution MIPS based RISC Core. MIPS (Microprocessor without Interlocked Pipeline Stages) is a RISC (Reduced Instruction Set Computer) outline. A RISC is a microchip that had been proposed to play out a little game plan of rules, with the purpose of extending the general speed of the processor. MIPS have 5 periods of pipeline viz. Rule Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MEM) and Write Back (WB) modules. The diverse modules being used are Instruction Memory, Data Memory, ALU, Registers et cetera. The purpose of this paper is to consolidate Hazard area unit and Data sending unit for capable execution of the pipeline. The confirmation of these is using Verilog-HDL. The primary objective of this MIPS processor is to play out Multiple directions in a solitary time cycle at once and it is confirmed in the Hardware Description Language (HDL) - Verilog in Xilinx 14.3 Kintex7 framework The module handiness and execution issues like region, control dissemination and postponement are researched using Xilinx 14.3 Kintex7 Tool.

At introduce, the ampleness of the RISC processors is generally recognized to be more noticeable than that of their CISC accomplices. Before their execution the rules are changed over into RISC headings in even the most standard CISC processors. The characteristics said above stress the arrangement nature of RISC in the market for introduced structures known as "Framework on-a-chip (SoC)".

The arrangement of a 64-bit Optimized MIPS RISC processor for applications logically embedded structures and moreover I attempted to differentiate that and the RISC processor having an effortlessness of pipelining. RISC is a blueprint thinking that has transformed into a standard in consistent and building applications. The processor executes most of the rules in single machine cycle influencing it to ideal for use in quick structures. The processor is made and executed on a FPGA board Spartan XC7K480T (KINTEX 7) using VHDL and VERILOG with the true objective that one can reconfigure it as showed by specific essentials of the goal applications. The processor is adequately powerful to be used as a stay singular dealing with segment and is non adequately particular to be used as a piece of multi-processor System on Chip.

The boss littler scale processors demonstrating reduced course set are SPARC, ARM, MIPS and IBM's PowerPC. RISC processor regularly has stack store outline. These shows there are two bearings for getting to memory which are a load rule set to stack data from the memory and store rule set to Write Back (WB) the data into memory without any rules.

II. Literature Survey

This article delineates a 8-bit RISC processor setup using Verilog Hardware Description Language (HDL) on FPGA board. The proposed processor is arranged using Harvard configuration, having separate course and data memory. The outstanding component of proposed processor is pipelining, used for improving execution, with the true objective that on each clock cycle one rule will be executed. Another fundamental component is that rule set contains only 34 bearings, which is uncommonly essential, easy to learn and littler. The proposed processor has 8-bit ALU, Two 8-bit I/O ports, serial-in/serial-out ports, Eight 8-bit all around helpful registers, 4-bit flag enroll and require based three vectored meddles. Another great position of the proposed processor is that it can execute programs with up to 262,144 rules in

Length, to such an extent, to the point that any reasonable tasks can be fitted into it. The proposed processor is physically minded Xilinx Kintex 7 Starter Board FPGA with 0.0517µs rule cycle.

This paper demonstrates the blueprint and execution of a low power five-organize parallel pipelined structure of a MIPS-64 consummate CPU. The distinctive squares fuse the data way, control justification, data and program memories. Peril acknowledgment and data sending units have been joined for beneficial use of the pipeline. A balanced plan is prescribed that prompts important power diminish by decreasing bothersome changes. Verilog design took after by amalgamation on to Xilinx Kintex 7 FPGA was done. On-chip appropriated memory of Kintex 7 was used for the data and the program memory use.

III. MIPS ARCHITECTURE

The accompanying outline demonstrates the fundamental architecture of a MIPS-based framework:

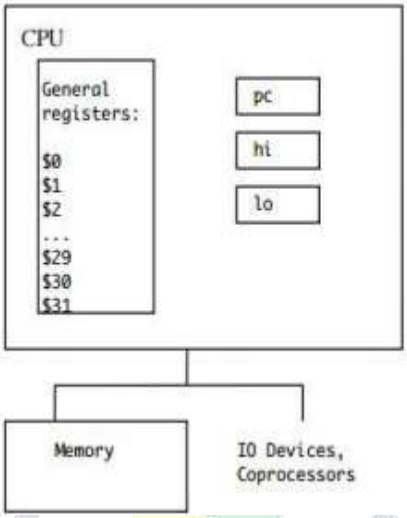


Fig. 1. Basic MIPS Architecture

Microprocessor without Interlocked Pipeline Stages (MIPS) is a RISC (Reduced Instruction Set Computing) engineering. Pipelined MIPS has five stages which are IF, ID, EX, MEM and WB. Pipelining suggests a couple of exercises in single data path at a comparative minute. Pipelining is used to enhance the limits of the RISC processor which is the reason behind its utilization in this sort of PC plan. A multi cycle CPU includes endless errands. So in the event that one errand happens, rather than sitting tight for the method to finish, meanwhile another task is begun in comparable data route in the meantime without interfering with the past endeavor. The methodology is thusly isolated into different pipelined stages. Following each clock another undertaking is incited in the pipeline stage to which the methodology is being supported to. The initiating is overseen without making any obstructions the past strategy. This makes synchronous utilization of all stages in the data way possible. This along these lines would addition have the capacity to the throughput of MIPS.

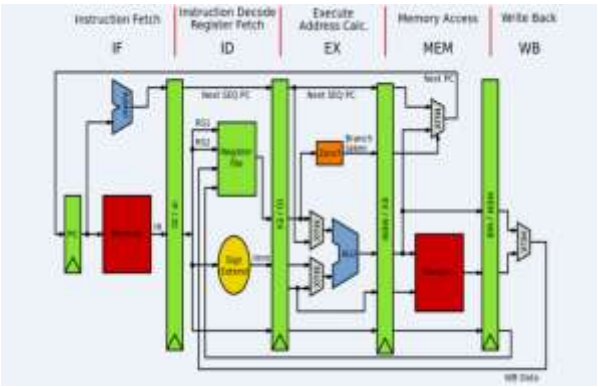


Fig.2. 5-Stage Pipelined MIPS

MIPS processor has been executed using five pipeline stages, which are Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory get to (MEM) and Write Back (WB). The division of these stages is expert by phenomenal registers known as pipeline registers. The purpose of these registers is to detach the periods of the rules so that there is no unsatisfactory information because of various headings being executed in the meantime. They are named in the midst of each of these: IF/ID Register, EX/MEM Register and MEM/WB Register. The data path showed in Fig. 2. is that of the MIPS pipelined processor.

3.1 Instruction Fetch (IF)

The Command handed-off to the Program Counter (PC) to get the guideline from the reserve memory is the thing that induces the essential pipelining task of the IF organizes. The capacity of PC and Instruction for the progressive check cycle is done in the IF/ID pipelined enroll as RAM (Random Access Memory)

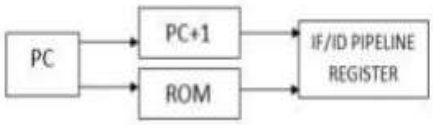


Fig. 3. IF Stage representation

IF stage for the most part relies on upon PC's represent value. Based on the PC value the processor gets the instructions from the cache and took after by which the Program Counter value is increased by 1. Subsequently, the IF/ID register gets this data took after by which the data is transferred to the decoder unit. The Instruction Fetch (IF) arrange task has been spoken to in Fig. 3.

3.2 Instruction Decoder (ID)

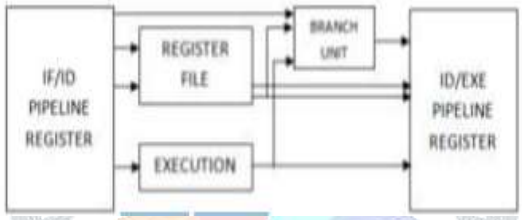


Fig. 4. ID Stage representation

The Opcode is given off to the decoder unit exactly when the direction is gained from the IF orchestrate. guideline Decoder ID arrange guides the controlling summon to the diverse units of the MIPS processor taking a gander at the Opcode of the bearings. Consequently the acquisition of data from the MIPS registers is finished by the Read Register. The Branch unit is besides combined into Instruction Decoder (ID) orchestrate. The Input data of ID mastermind is gotten from IF sort out as showed up in Fig. 2.This disentangling stage consolidates four unmistakable guidelines: Register (R) type, Immediate (I)type, Jump (J) sort and Input/output (I/O) type headings. Dependent upon these bearings the limit will be performed utilizing beforehand specified gatherings. Fig. 4. exhibits Instruction Decode (ID) sort out action.

3.3 Execute (EX)

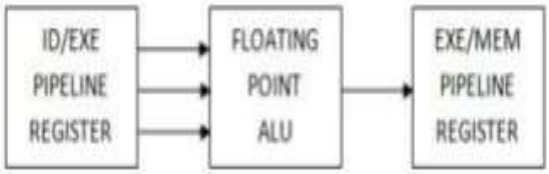


Fig. 5. Execution Stage (EX)

Speaking to Following the Instruction Decoder (ID), the rules are sent to execute stage(EXE or EX). Execute (EX) arrange performs Arithmetic and Logical Unit (ALU) shapes. Execution of exercises is the real piece of Execute (EX) compose, for instance calculating errands, for instance, development and differentiate or possibly AND. In particular, EX/MEM pipelined enroll gets the result upon the execution of specific rules (i.e. FP ALU). Execute compose depiction is showed up in Fig. 5.

3.4 Memory Access &Input/output (MEM)

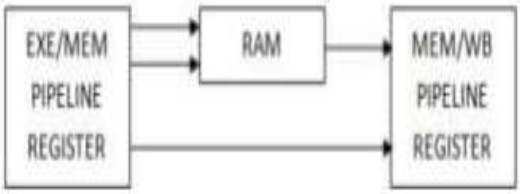


Fig. 6. Memory Access representation

The putting away and stacking of qualities alongside contributing and yielding information from the processor is the essential capacity of the memory get to (MEM) organizes. The outcome will be dispatched to the WB mastermind in a circumstance where the bearing is neither memory nor IO rule. After the result is figured the basic limit is to store the data esteems in the goal enlist. The Memory Access (MEM) arrange assignment is displayed in Figure 6.

3.5 Write Back (WB)

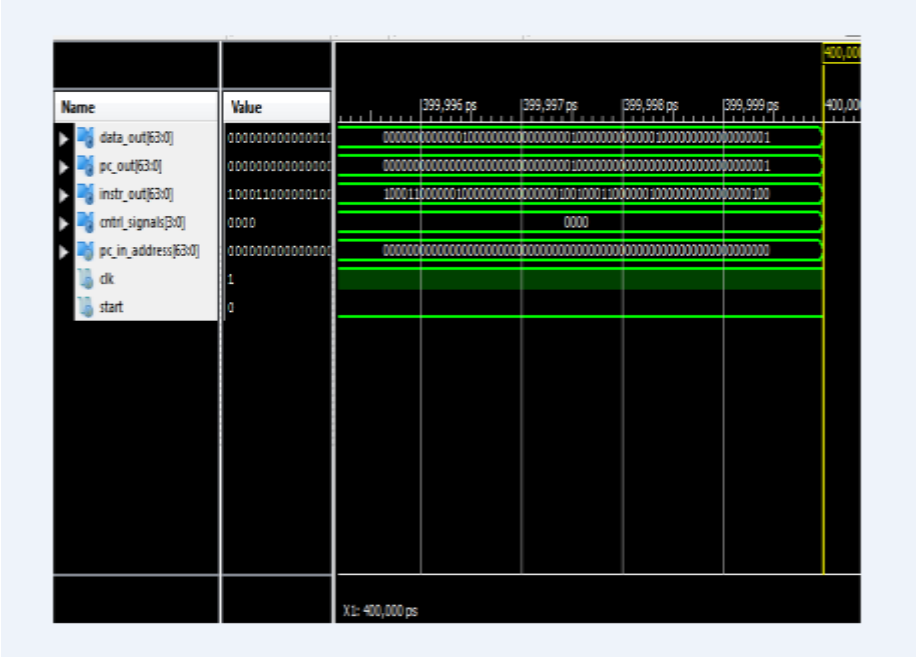
Fig. 7. Write Back representation

As indicated by Fig. 7., the Write-Back (WB) action is the last period of the RISC based MIPS outline which makes the result, store information and data and info information from insect to the enlist record. Making the data that has been gotten from the MIPS enroll to the objective enlist is the essential purpose of this stage.

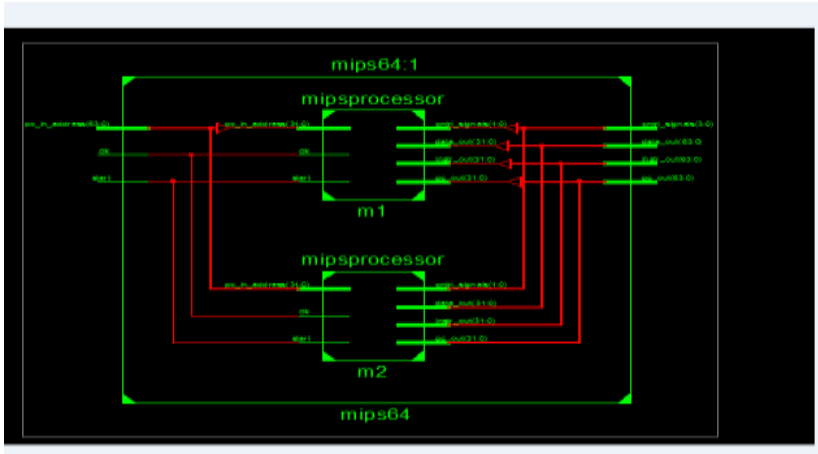
IV. Simulation Results

The written Verilog HDL Modules have successfully simulated and verified and synthesized using Xilinx ISE 14.3 kintex7.

Simulation result:



Synthesis Results:
RTL Schematic:



AREA:

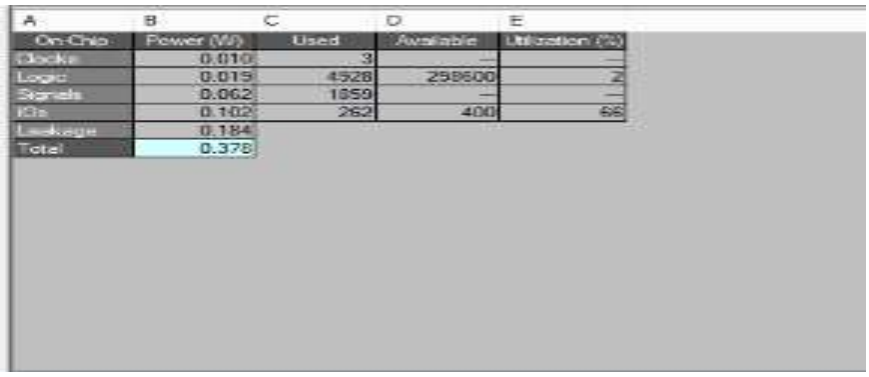
Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	11124	4656	238%
Number of Slice Flip Flops	190	9312	2%
Number of 4 input LUTs	22155	9312	237%
Number of bonded IOBs	262	232	112%
Number of GCLKs	1	24	4%

Timing report:

```
---------------------------------------------------------------------------
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 196 / 144
---------------------------------------------------------------------------
Offset:              7.446ns (Levels of Logic = 4)
  Source:            m2/instr_memery/data_29 (LATCH)
  Destination:       cntrl_signals<3> (PAD)
  Source Clock:      clk falling

  Data Path: m2/instr_memery/data_29 to cntrl_signals<3>
                                Gate     Net
    Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDE:G->Q             56   0.588    1.109  m2/instr_memery/data_29 (m2/instr_memery/data_29)
     LUT4:I2->O            1   0.612    0.000  m2/control_unit/Alu_op_or0002_F (N822)
     MUXF5:I0->O           6   0.278    0.721  m2/control_unit/Alu_op_or0002 (m2/control_unit/Al
     LUT4:I0->O            1   0.612    0.357  m2/control_unit/Alu_op<1>1 (cntrl_signals_3_OBUF)
     OBUF:I->O                 3.169          cntrl_signals_3_OBUF (cntrl_signals<3>)
    ----------------------------------------
    Total                     7.446ns (5.259ns logic, 2.187ns route)
                                      (70.6% logic, 29.4% route)
```

Power report:



A	B	C	D	E
On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.010	3	–	–
Logic	0.019	4528	298600	2
Signals	0.062	1859	–	–
IOs	0.102	262	400	66
Leakage	0.184			
Total	0.378			

V. CONCLUSION

This Research paper depicts a 64-bit Microprocessor without Interlocked Pipeline Stages (MIPS) based RISC processor is executed successfully with pipelining in Xilinx kintex7 14.3 Tool. In a five phase pipelining the execution of multiple instructions at a time in a single clock cycle is Achieved. Unlike other architectures MIPS has many market applications. The Cost of devices using MIPS is less and it support for graphics and long term support. Overall MIPS has Low cost huge functionality and high performance gives it to a bigger market than the rest.

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