Design an Efficient Architecture of SRAM on FPGA

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Abstract : From the past few decades it is observed that memory is a major part in power consumption of overall system. Therefore, low power memory designing is must for efficient system design. Here, first we design 16kb(kilobits) of SRAM using Verilog. To make it power efficient, we use IO standards. These IO standards used for module designing like ALU, Frame buffer, Multiplier etc. on FPGA. Our 16kb SRAM design is synthesized on Artix-7 FPGA. We used LVCMOS , HSTL and Mobile-DDR IO standard for comparison of power consumption. If memory design's requirement is noise immunity then we have to select HSTL IO Standard and at 1GHz frequency there is 72.60% of power is wasted and at 3.5 GHz frequency 34.09% of power is wasted in comparison with LVCMOS15 IO Standard. This wastage of power is because of extra transistor used in HSTL IO Standards' buffer design. Thus we have to switch for other IO Standard, for Low Power Memory design. For low power design we proposed LVCMOS15 IO Standard based SRAM design. From the power analysis we observed that if we used LVCMOS15 instead of HSTL then we saved the power consumption of SRAM, approx. 42% at 1GHz and 25% at 3.5 GHz. And also we compare the LVCMOS15 IO Standard with Mobile-DDR. From this comparison it is observed that , at 1GHz 27% of power is saved and at 3.5GHz 20% of power is saved if we use LVCMOS15 instead of Mobile-DDR.

Index Terms – Low Power, SRAM, FPGA, IO Standard

I. INTRODUCTION

From the past decades , researchers worked on memory designing to make it power efficient , area efficient , cheaper and faster. Efficient memory design has to provide less delay for faster operation. There is always trade-off between these parameters[1]. Means if we want higher speed then we have to compromise with power. According to Moore's law number of transistors are doubled after each 18 months. This is because of technology is getting shrinking to Nanometer scale. If technology is scaled down then number of transistors are more, if transistors are more then number of logic cells are more and so density of FPGAs increases. Therefore, new FPGAs are fabricated on 16nm node[1]. Now, as far as memory concerns , its design has to be efficient, and if we want to design such kind of memory on FPGA then selection of IO standards is better approach for this work. SRAM is static memory , provides random read-write operation and also provides faster performance compared to DRAM. Therefore, It has to be power efficient up to some extent. Off course there is trade off between power and speed but still if we select proper IO standard then it is possible to design efficient memory[7].

SRAM is the nearest memory to the processor which provides faster operation than any other memory. Its basic Architecture has 6 Transistor cell [8] as shown in Fig. 1. Back to back inverter is connected to retain the data in the cell. To access this bit of data, access transistors are used which are connected to bit lines. Its read and write operation requires pre-charging of bit lines, then according to internal data, discharging of bit lines will be performed. Sizing of cell for efficient read and write operation is must. Therefore, transistor sizing of SRAM cell is essential part of SRAM Design[8]. Fig.1 shows the basic structure of static memory cell, which consist of two PMOS pull up transistor(PM0,PM1) and two NMOS pull down transistor(NM0,NM1). Access transistors (NM2,NM3) are used to transfer the internal bit of data to bit lines(bl,bl_bar). Gate of Access transistors, is connected to word line(wrt). If wrt line is asserted then and then only read or write operation of cell can be happened.

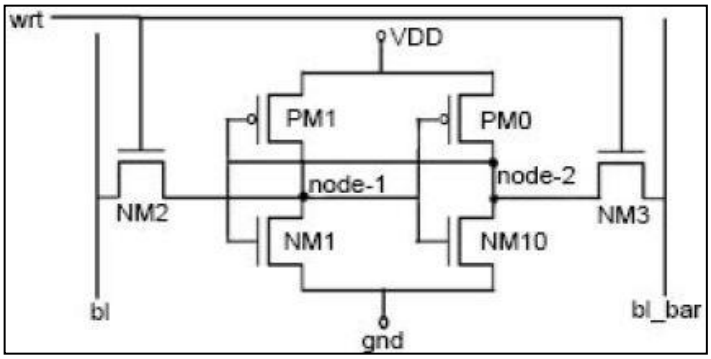

Fig. 1 SRAM 6 Transistor Cell [8]

FPGA is Field Programmable Gate Array, contains thousands of logic cells, Flip flops and many other digital blocks. All these modules present in CLB(Configuration Logic Block). CLB is one of the main block of FPGA. For communication between CLBs to IO pads or vice versa, programmable interconnects are there. Internal Architecture of FPGA contains CLBs, IO pads and Programmable interconnects as shown in fig.2[6]. From the past three decades, it is observed that process technology of FPGA is grown up[1]. Due to this, Ultra-scale FPGAs are fabricated on 16 nm technology node. Security of FPGA in terms of its storage data gains more attraction now a days. SRAM based FPGAs were build to provide better security[11]. The basic feature of SRAM that is its volatility is used for security purpose in SRAM based FPGAs.

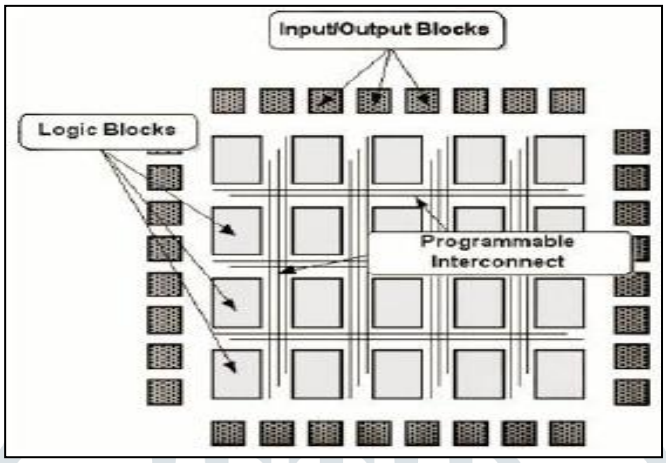

Fig.2 Internal Architecture of FPGA[6]

If power is cut off from the memory then its data does not present in it and no one can steal this bit streams(FPGA data) of FPGA. This kind of security feature is present in 7 series of Xilinx's FPGAs and Altera's Stratix FPGA. Basically military, industrial and space applications uses these FPGAs. Section II is about different IO standards provided by FPGA, Section III is about IO standard related results. At last, Section IV is about conclusion and future work.

II. DIFFERENT IO STANDARDS PROVIDED BY FPGA

IO standards used as buffer, provides different configuration i.e. internal supply voltage, output driver supply voltage, reference voltage etc. These buffers resides between IO blocks or IO pads and Logic blocks of FPGA. When any signal transmitted from port to logic block or vice versa , there is a chance of noise added into this signal and signal gets disrupted. This phenomena of disrupting signal is called transmission line effects , due to which actual data will not sent/receive at desired location. To reduce these kind of effects, buffers in terms of IO standards are used. Different IO standards provided by FPGA are High speed trans-receiver logic(HSTL)[2], Stub Series Terminated logic(SSTL)[7],[10], Low voltage Digitally control Impedance with Half Impedance (LVDCI_DV2)[7],Low voltage Transistor Transistor logic(LVTTL)[6], Low voltage CMOS(LVCMOS) [7],[4]and Mobile DDR(Double Data Rate)[6]. These IO Standards have different Families, which are operated on different supply voltages. Some of these family is mentioned here.

A. HSTL IO Family:

HSTL mainly classified into output buffer supply voltage like HSTL_II_18 has 1.8V VCCO. HSTL_II_12 has 1.2V VCCO.Fig.3 shows the various family members of HSTL family. HSTL is technology independent IO standard. Used for mainly durability of hardware.

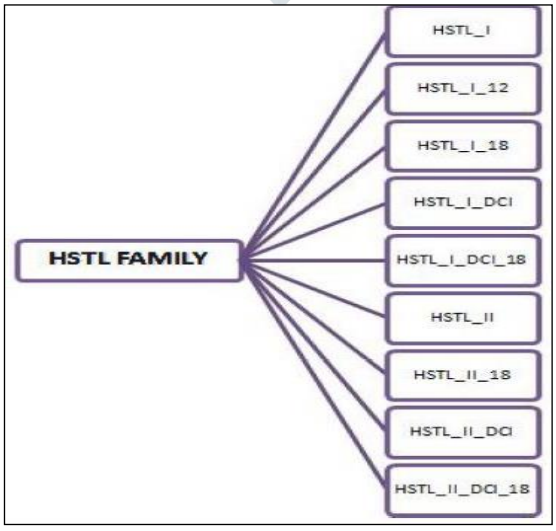

Fig.3 Family of HSTL Standard[2]

In HSTL class I IO Standard output buffer is push pull amplifier and input buffer is differential amplifier. As shown in the below figure input buffer requires parallel termination resistor. This termination resistor is used to minimize the reflection of signals.

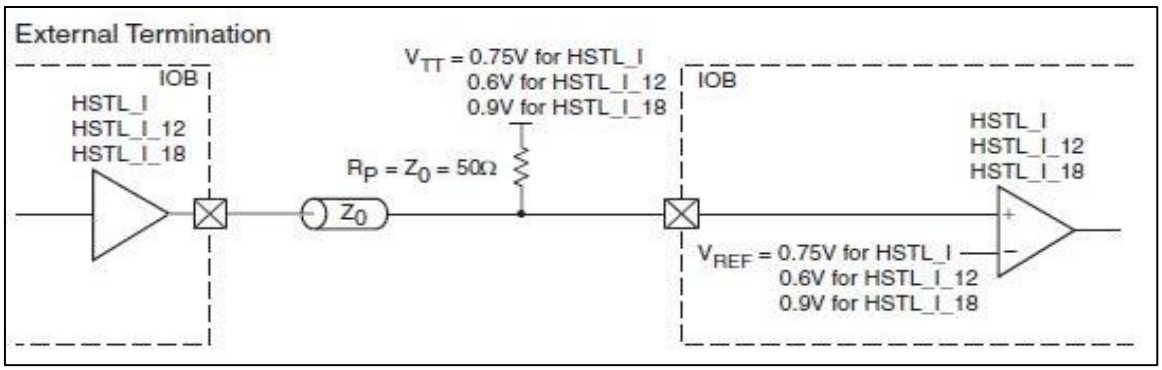

Fig.4 HSTL Class I IO Buffer[12]

In HSTL class II IO Standard output buffer is push pull amplifier and input buffer is differential amplifier as present in HSTL class I. As shown in the below figure input buffer and output buffer ,both requires parallel termination resistor. This termination resistors is used to minimize the reflection of signals. At higher frequency , this class II design proves to be more power efficient.

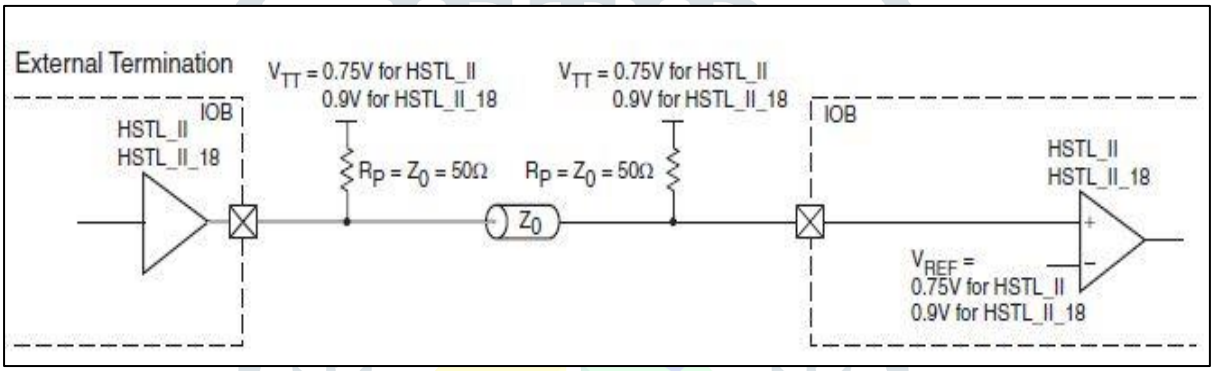

Fig.5 HSTL Class II IO Buffer[12]

B. LVCMOS IO Family

Low Voltage CMOS is generally used for Low Power Application like 3.3V, 2.5V, 1.8V, 1.5V and 1.2V application. It also has various Family types as shown in Fig.4. LVCMOS is upgraded version of LVTTL.

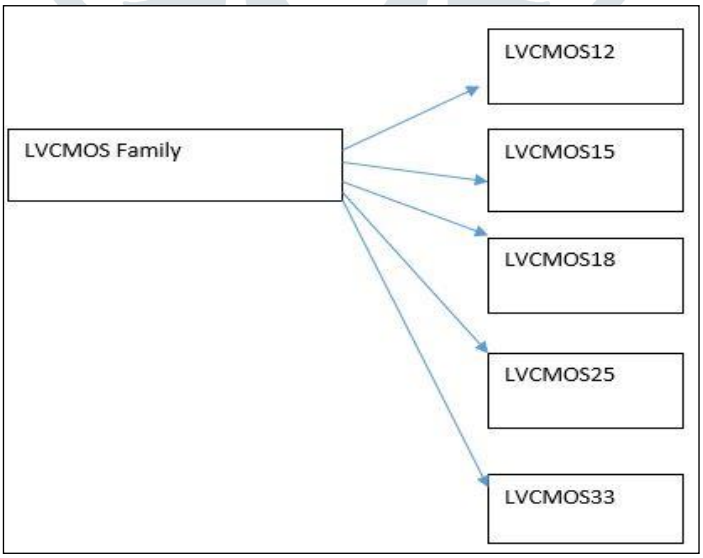

Fig.6 Family of LVCMOS[2]

Below figure is schematic of LVCMOS unidirectional termination. Left sided buffer is output buffer which takes input from FPGA and send signals to IO ports via its output terminal. Right sided buffer is input buffer which takes input from IO port and send this signal to FPGA. Impedance is Z0 which is used for matching the impedance between output-input buffer. If impedance is matched then reflection of signal gets minimized.

Unidirectional termination means termination from output buffer to input buffer only not from input to output buffer. Sometimes Vtt(termination voltage) is needed in LVCMOS IO Standard. This Vtt is apply to termination resistor for minimizing the signal reflection.

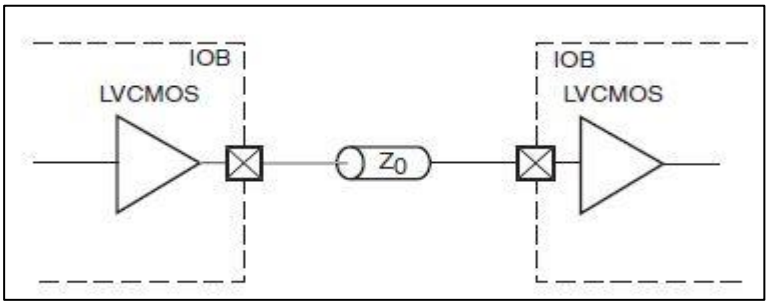

Fig.7 LVCMOS IO Buffer[12]

C. Mobile_DDR IO Standard

This IO standard is has single ended CMOS based input buffer. It is used for 1.8V application. It is used as Low Power IO Standard. It used for double data rate (DDR) transmission of data. It is not needed to use Vtt or Vref because it is single ended. We used this IO standard in our memory design.

III. LITERATURE SURVEY

For designing SRAM Architecture we had gone through different research papers , published in conferences and journals. These papers is completely based on IO Standard based work. First paper's objective is to design power efficient memory circuit on 28nm FPGA with power efficient IO Standard at different operating frequency. They use HSTL IO Family for designing memory. The efficient IO Standard used in their work is HSTL class II DCI at 1THz, HSTL class I_12 at 100GHz and 10GHz and at 1GHz, HSTL class I is power efficient. Next paper's objective is design power efficient RAM on Spartan 3E. They uses LVCMOS12 and LVCMOS25 IO Standards. At 100GHz , LVCMOS25 IO Standard is power efficient and at 100MHz LVCMOS12 IO Standard is power efficient. In next paper memory was designed by HSTL, LVCMOS, SSTL, HSLVDCI and LVDCI_DV2 IO Standard. Among them LVCMOS15 and LVDCI_DV2 is power efficient IO Standards. We observed that there is another approach to design Power efficient memory , which is thermal aware memory. In this work, researchers operate memory with different operating frequency and different operating temperature. Here, they had not used any IO Standard but they operate memory with different temperature and they identified that if temperature gets decrease then power consumption of RAM gets minimize. Their main objective is to identify proper operating temperature at which power consumption is low. Next Paper has the comparison between Mobile_DDR and LVTTL IO Standard. In this paper main objective of researchers is , identification of power efficient IO Standard among Mobile_DDR and LVTTL, to design power efficient RAM on 28nm Artix-7 FPGA. Thus they identify that Mobile_DDR IO Standard is power efficient in comparison with LVTTL. Our base paper is about SRAM design, which is synthesized on 28nm Artix-7 FPGA and uses HSTL_I, HSTL_II, HSTL_I_18 and HSTL_II_18 IO Standard. Among them at 1GHz to 2.5GHz, HSTL_I is power efficient and at 3GHz and 3.5GHz, HSTL_II is power efficient. Next section is about proposed work.

IV. PROPOSED SRAM DESIGN

This design of SRAM is based on IO Standards. Proposed design is of size 16Kb. We synthesized this design in Verilog. We used "reg" keyword for storing the output bits. First we compare LVCMOS25, LVCMOS18 and LVCMOS15 IO Standard with each other to identify power efficient IO Standard of SRAM. We use different operating frequency for this comparison. Then we had compared the HSTL IO Standard with LVCMOS15 IO Standard, to identify how much power is saved for SRAM design. At last there is a comparison between Mobile-DDR and LVCMOS15 to identify the power tradeoff with speed.

A. Power Analysis of SRAM with LVCMOS IO Family at different operating frequency:

TABLE 1:Power Consumption of SRAM at 1.5GHz frequency with LVCMOS IO Standards

IO Standard	Clock	Signals	BRAM	IO	Leakage	Total
LVCMOS25	0.007	0.003	0.021	0.154	0.086	0.271
LVCMOS18	0.007	0.003	0.021	0.087	0.083	0.201
LVCMOS15	0.007	0.003	0.021	0.065	0.081	0.178

From the above table it is observed that Clock, signals and BRAM power consumption constant but IO Power and Leakage power varies. IO power for SRAM with LVCMOS25 IO standard is more and with LVCMOS15 IO Standard it is less. Therefore, total power consumption of SRAM, with LVCMOS15 IO Standard is less. Therefore, we had selectected LVCMOS15 IO Standard for SRAM design at 1.5GHz.

TABLE 2 : Power Consumption of SRAM at 2.5GHz frequency with LVCMOS IO Standards

IO Standard	Clock	Signals	BRAM	IO	Leakage	Total
LVCMOS25	0.012	0.006	0.035	0.256	0.086	0.395
LVCMOS18	0.012	0.006	0.035	0.146	0.083	0.281
LVCMOS15	0.012	0.006	0.035	0.109	0.082	0.243

From the above table it is observed that IO Power consumption is 0.256w with LVCMOS25 IO Standard and 0.109w for LVCMOS15 IO Standard. Also leakage power consumption is 0.086w and 0.082w for LVCMOS25 and LVCMOS15 IO standard respectively. Therefore, LVCMOS15 IO standard is used for SRAM design at 2.5GHz.

TABLE 3: Power Consumption of SRAM at 3.5GHz frequency with LVCMOS IO Standards

IO Standard	Clock(w)	Signals(w)	BRAM(w)	IO(w)	Leakage(w)	Total
LVCMOS25	0.017	0.008	0.049	0.358	0.087	0.518
LVCMOS18	0.017	0.008	0.049	0.204	0.083	0.361
LVCMOS15	0.017	0.008	0.049	0.152	0.082	0.308

From this table it observed that , total power consumption of SRAM with LVCMOS15 is 0.308w and with LVCMOS25 it is 0.518, so ultimately we can say that LVCMOS15 is power efficient IO Standard for SRAM design at 3.5GHz. Therefore, we conclude that LVCMOS15 can be used for SRAM design on FPGA at all these operating frequency. Next subsection is about comparison between LVCMOS15 and HSTL IO Standards.

B. Comparison between HSTL IO Standard and LVCMOS15 IO Standard

This comparison is done to identified how much power is saved , if we use LVCMOS15 IO Standard instead of HSTL IO Standard.

TABLE 4: Comparison between HSTL and LVCMOS15 IO Standard at 1.5GHz

IO Standard	Clock(w)	Signal(w)	BRAM(w)	IO(w)	Leakage(w)	Total
HSTL_I	0.007	0.005	0.021	0.172	0.083	0.286
LVCMOS15	0.007	0.003	0.021	0.065	0.081	0.178

Here, if we use LVCMOS15 IO Standard instead of HSTL_I then we save 37% of power for SRAM. From the table it is observed that clock and BRAM power consumption is same but IO and Leakage power consumption varies. But signal power decreases by 0.002w with LVCMOS15 IO Standard.

TABLE 5: Comparison between HSTL and LCMOS15 at 2.5 GHz

IO Standard	Clock(w)	Signals(w)	BRAM(w)	IO(w)	Leakage(w)	Total
HSTL_I	0.012	0.008	0.035	0.217	0.082	0.354
LVCMOS15	0.012	0.006	0.035	0.109	0.082	0.243

Here, we saved 31.35% of power for SRAM , if we use LVCMOS15 instead of HSTL IO Standard because total power consumption is less with LVCMOS15 IO Standard. From the above table it is observed that signal power decreases by 0.002w with LVCMOS15 IO Standard.

TABLE 6: Comparison between HSTL and LVCMOS15 at 3.5GHz

IO Standard	Clock(w)	Signals(w)	BRAM(w)	IO(w)	Leakage(w)	Total
HSTL_II	0.017	0.011	0.049	0.254	0.082	0.413
LVCMOS15	0.017	0.008	0.049	0.152	0.082	0.308

Here, we saved 25.42% of power for SRAM, if we use LVCMOS15 instead of HSTL_II IO Standard because total power consumption with HSTL_II is more and with LVCMOS15 it is less. In the next subsection, we compare the Mobile-DDR IO Standard with LVCMOS15 IO Standard.

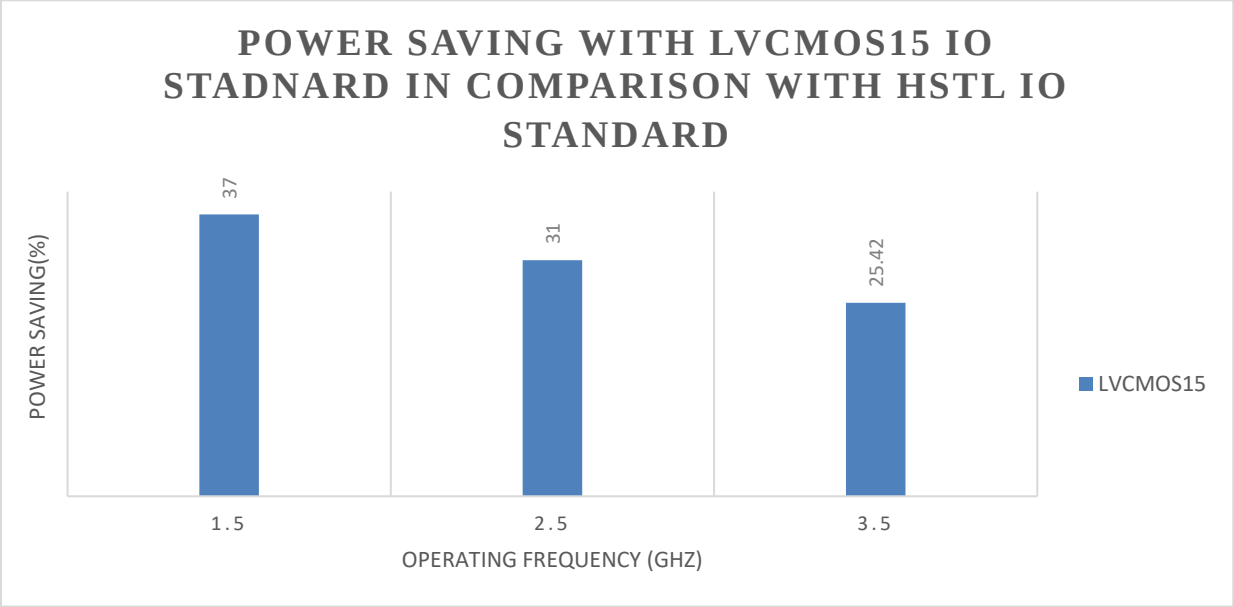

Fig.8 Power Saving of SRAM with LVCMOS15 IO Standard in Comparison with HSTL IO Standard

C. Comparison between Mobile_DDR IO Standard and LVCMOS15 IO Standard

Mobile_DDR IO Standard has two features. It can be used for low power memory bus and for Double Data rate transmission on the memory bus. Here, first we compare Mobile_DDR IO Standard with LVCMOS15 to identify which of these IO Standard is power efficient for SRAM design. Then we calculate the power tradeoff for Mobile_DDR IO Standard.

TABLE 7: Comparison between Mobile_DDR and LVCMOS15 at 1.5GHz

IO Standard	Clock(w)	Signals(w)	BRAM(w)	IO(w)	Leakage(w)	Total
Mobile_DDR	0.007	0.003	0.021	0.125	0.083	0.239
LVCMOS15	0.007	0.003	0.021	0.065	0.081	0.178

Here, if we use LVCMOS15 IO Standard instead of Mobile_DDR for SRAM design then, we save 25.52% of total power for SRAM. Form this table it is observed that total power consumption is 0.178w with LVCMOS15 and 0.239w with Mobile_DDR IO Standard.

TABLE 8: Comparison between Mobile_DDR and LVCMOS15 at 2.5GHz

IO Standard	Clock(w)	Signals(w)	BRAM(w)	IO(w)	Leakage(w)	Total
Mobile_DDR	0.012	0.006	0.035	0.177	0.083	0.313
LVCMOS15	0.012	0.006	0.035	0.109	0.082	0.243

Here, if we use Mobile_DDR IO standard then total power consumption is 0.313w. Thus if we use LVCMOS15 IO Standard at 2.5GHz then, we save 22.36% of power. Here, Clock, BRAM and signal power is constant.

TABLE 9 : Comparison between Mobile_DDR and LVCMOS15 at 3.5GHz

IO Standard	Clock(w)	Signals(w)	BRAM(w)	IO(w)	Leakage(w)	Total
Mobile_DDR	0.017	0.008	0.049	0.230	0.083	0.386
LVCMOS15	0.017	0.008	0.049	0.152	0.082	0.308

Here, if we use LVCMOS15 IO Standard then we save 20.20% of power for SRAM at 3.5GHz frequency. Mobile_DDR IO Standard also provide low power feature but compare to LVCMOS15 IO Standard it is less power efficient , as it is observed from the above comparison. Below figure is about power saving of SRAM with LVMCOS15, at different operating frequency.

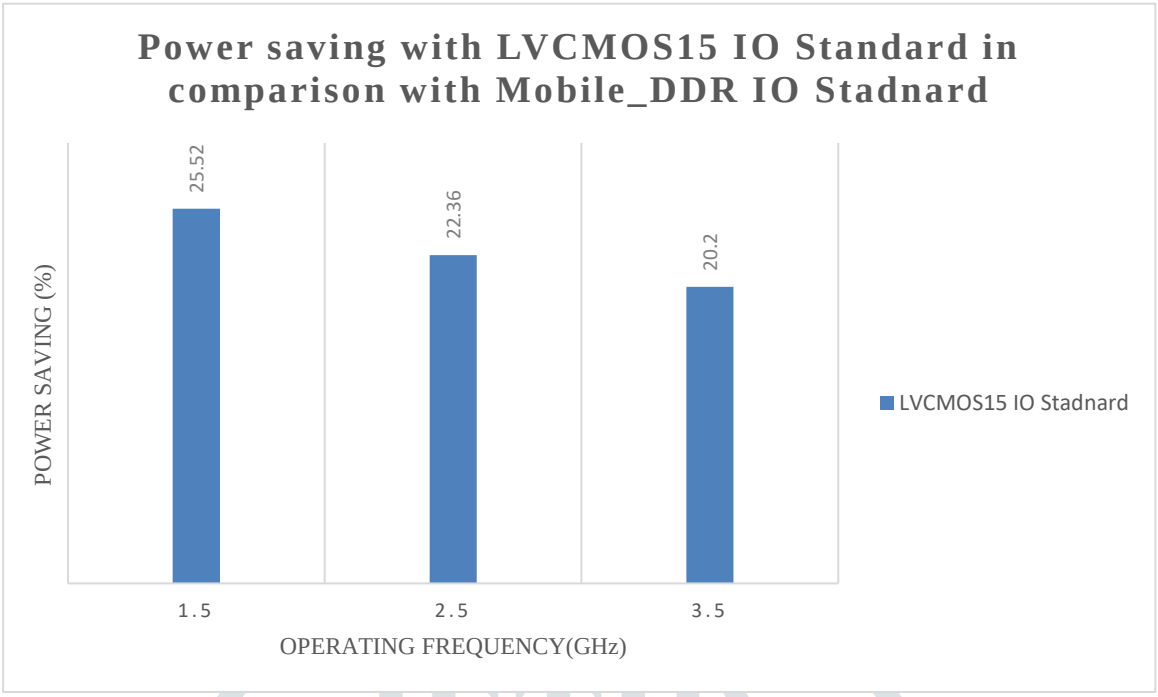

Fig.9 Power Saving of SRAM with LVCMOS15 IO Standard in comparison with Mobile_DDR IO Standard

Form this above figure, we can observed that, if we use LVCMOS15 instead of Mobile-DDR IO Standard then at 1.5GHz we save 25.52% of total power, at 2.5GHz we save 22.36% of total power and at 3.5Ghz we save 20.2% of total power for SRAM. Next section is about power tradeoff with speed for Mobile_DDR IO Standard and power tradeoff with noise immunity for HSTL IO Standards in comparison with LVCMOS15 IO Standard.

V. POWER TRADEOFF

In this section we provide the power tradeoff in percentage for HSTL IO Standards and Mobile_DDR IO Standard. Subsection A and B gives this information.

A. Power tradeoff with noise immunity:

If our memory design requires noise immunity then HSTL IO Standards are better. At that time we have to compromise with power and we have to avoid the selection of LVCMOS15 IO Standard. This power tradeoff is shown in the below figure.

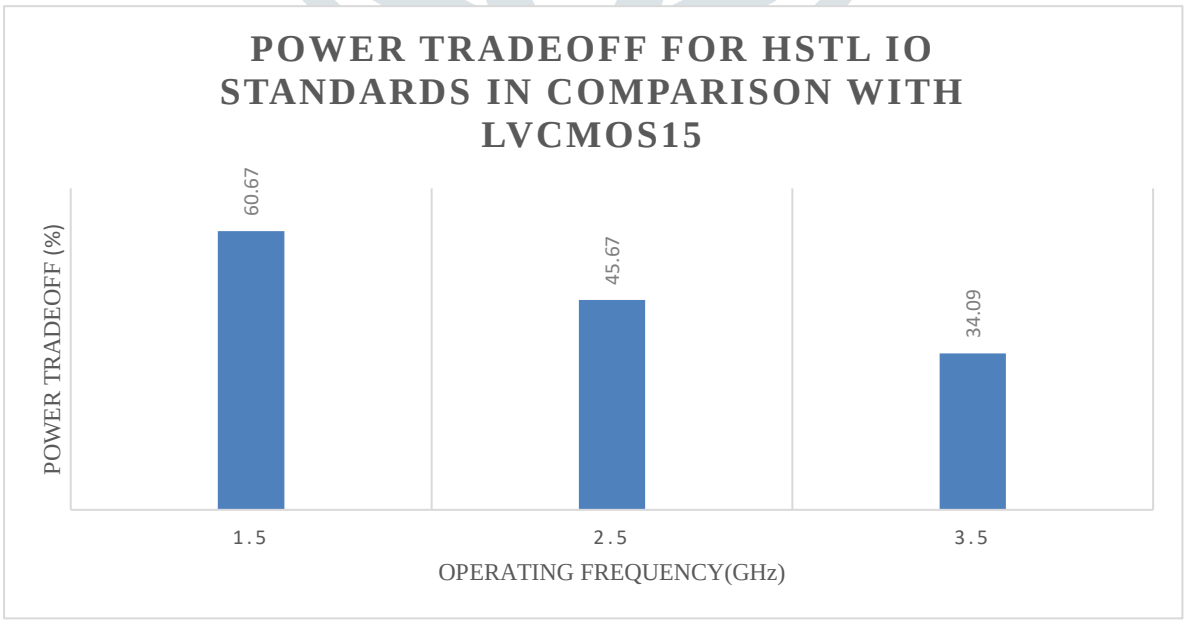

Fig.10 Power Trade-off for HSTL IO Standard in Comparison with LVCMOS15

As shown in the above figure, at 1.5GHz operating frequency of SRAM, if we use HSTL class I IO Standard instead of LVCMOS15 then 60.67% of power is wasted , at 2.5GHz 45.67% of power is wasted and at 3.5GHz 34.09% of power is wasted. Here, these wastage of power is present because we select the HSTL IO Standard in stead of LVCMOS15 IO Standard. Now, the selection of HSTL IO Standard is must , because we want noise immunity as well as we want the minimum wastage of power. Thus at that time , 3.5GHz operating frequency is good choice, because at 3.5GHz wastage of power is less compared to 1.5GHz and 2.5GHz. Therefore, an SRAM can be design with 3.5GHz frequency with the use of HSTL class I IO Standard, with minimum wastage of power.

B. Power tradeoff with speed:

If memory design requires speed in terms of double data rate transmission then Mobile_DDR IO Standard provides this feature but we have to compromise with power. Because we used Mobile-DDR IO Standard rather than LVCMOS15 so definitely we have to compromise with power. This power trade off is shown in the below figure.

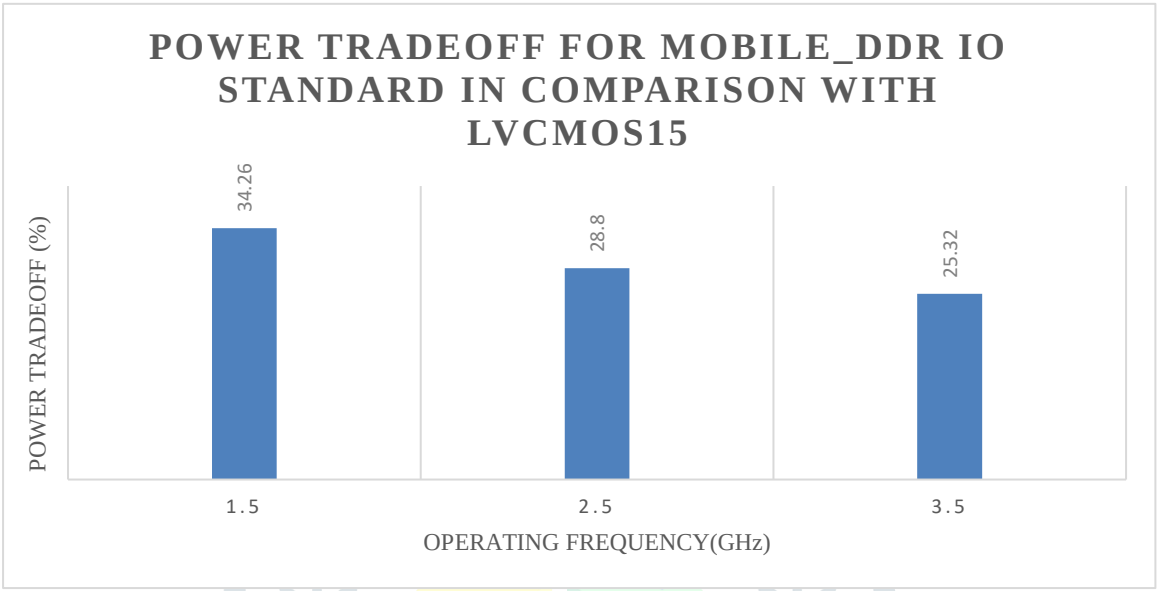

Fig.11 Power Trade-off for Mobile_DDR IO Standard in Comparison with LVCMOS15

From this figure we observed that, if we use Mobile_DDR IO Standard then at 1.5GHz operating frequency 34.26% of power is wasted, at 2.5GHz 28.8% of power is wasted and at 3.5GHz 25.32% of power is wasted. It is obvious thing that we have to compromise with power if our requirement is speed. But this power tradeoff analysis is done to identify the proper operating frequency which provides less amount of wastage of power and at this frequency we can use Mobile_DDR IO Standard for SRAM design.

VI. CONCLUSION

We synthesized our 16Kb of SRAM on Artix-7 FPGA. We used different operating frequency for SRAM and different IO Standard , to identify the power efficient IO Standard. At 3.5 GHz, we saved 25.42% of power if we use LVCMOS15 instead of HSTL IO(class II) standard and at 1.5 GHz, 37% of power is saved if we use LVCMOS15 IO Standard instead of HSTL IO(class I) standard. Also we saved 20.20% of power at 3.5GHz and 25.52% of power at 1.5GHz, if we use LVCMOS15 IO Standard instead of Mobile_DDR IO Standard. If speed is concerns then it is better to operate SRAM with Mobile_DDR IO Standard at 3.5GHz frequency because at this frequency percentage of power tradeoff is less compared to 2.5GHz and 1.5GHz frequency. If noise immunity is concern then it is better to operate SRAM with HSTL IO(class II) at 3.5GHz frequency because at this frequency percentage of power tradeoff is less compared to 2.5GHz and 1.5GHz frequency.

VII. FUTURE SCOPE

We synthesized our SRAM Design of 16Kb on 28nm FPGA. One can implement this design of SRAM on FPGA Hardware to check its compatibility with FPGA Chip. On hardware, how much SRAM power is consumed at different operating frequency with Mobile_DDR IO Stadnard can be checked. Also this SRAM can be implemented and design on 16nm FPGA.

ACKNOWLEDGMENT

I would like to thank my project mentor Mr. Tarun Agrawal for his technical support. Also I would like thank my college guide Mrs. Shivi Shukla for her motivation and encouragement for this research.

REFERENCES

[1] M. Stephen,"Three Ages of FPGAs: A Retrospective on the First Thirty Years of FPGA Technology ", Proceedings of the IEEE, USA, vol. 103, No.3, March 2015.

[2] Sweety, B. Pandey, T. Kumar and T. Das, "Design of Power Optimized Memory Circuit Using High Speed Transreceiver Logic IO Standard on 28nm Field Programmable Gate Array ", IEEE International Conference on Reliability, Optimization and Information Technology-ICROIT,India, February 2014.

[3] J. Moore and M. Stephen, "FPGAs Security: Motivations, Features and Applications," Proceedings of the IEEE, vol. 102, No.8 August 2014.

[4] D. Singh, B. Pandey and M. Pattanaik ,"IO standard based Low Power design of RAM and Implementation on FPGA," Journal of Automation and Control Engineering, vol.1, No.4, December 2013.

[5] G. Verma, M. Aditi, B. Pandey, "Thermal and Power Aware Internet of things enable RAM design on FPGA," IEEE 2nd International Conference on Computing for Suitable Global Development, New Delhi, INDIA, March 2015.

[6] A. Kumar, G. Sharma, T. Agrawal and D. Agrawal, "A Designing of Random Access memory using Different IO standard Technology," ICCCNT,TX,USA, July 2016

[7] R. Kaur, J. Kumar and S. Nagah, "IO standard based Low Power Memory Design and Implementation on FPGA," IEEE 2nd International Conference on Computing for Suitable Global Development, New Delhi, INDIA, March 2015.

[8] A. Pathak, D. sachan, "A modified SRAM based Low Power Memory Design", 29th IEEE International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID),4-8 January, 2016

[9] M. Bansal, R. Saini and N. Bansal, "HSTL I/O Standard Based Environment Friendly Energy Efficient ROM Design on FPGA", IEEE 2nd International Conference on Computing for Sustainable Global Development (INDIACom), New Delhi,INDIA,March,2015

[10] M. Bansal, R. Saini, B. Pandey and Hussain "SSTL I/O Standard Based Environment Freiendly Energy Efficient ROM Design on FPGA", Proceedings of the 3rd Intrnational Symposium on Environment-Friendly Energies and Applications, Paris, France, 2014

[11] M. Stephen,"FPGA Secutiry: Motivations, Features and Applications", Proceedings of the IEEE, USA, vol. 102, No.8, March 2015.

[12] https://www.xilinx.com/support/documentation/user_guides/ug471_7Series_SelectIO.pdf