Design and Functional Verification of DDR SDRAM Controller to Access Multiple Banks

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Abstract-Synchronous DRAM (SDRAM) has become a one of the most important memories of choice due to its significant features like high speed, burst access and pipelining. The high-end applications like Motorola MPC8260 or Intel Strong Arm uses processors which has the interface to the SDRAM by its processor's built-in peripheral module. However, for other applications, there is a need for the controller to provide proper commands for SDRAM such as initialization, read/write operations and memory refresh. But in normal 64-bit controllers only one bank of SDRAM can be accessed at a time so there is a need to access multiple banks to increase read/write access speed. Our work will focus on designing and verifying a 128-bit DDR controller to perform read/write on multiple banks at same time. The proposed design is implemented using Xilinx ISE 14.3.

Keywords — Synchronous Dynamic Random-Access Memory (SDRAM), Double Data Rate (DDR).

I.INTRODUCTION

Memory is the most important concern for any device that is manufactured today. Hence the demand for memories with high speed, high efficiency are increasing. For high throughput of memories there is a need for the controller with high clock frequency which controls the memory. As the clock speed of the controller increases, the designing of the controller ends up complex. So, there is need to design the controller with double and quad data rates. In this paper, the double data rate SDRAM controller is implemented to access multiple banks.

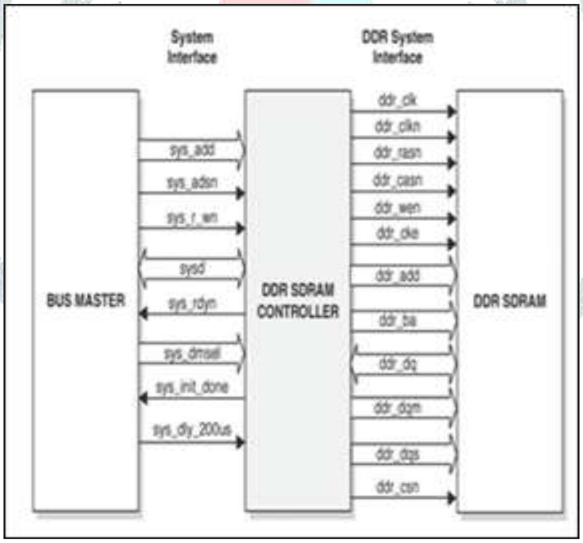


Fig. 1. DDR SDRAM controller system

We use synchronous DRAM (SDRAM) because of its high speed and pipelining capability. In top-line applications, worked in peripherals are available to give applications access to memory. In other applications, the memory controller is to be outlined to give read and write commands, commands to refresh the memory and other similar commands. In this paper, the SDRAM controller is situated between the SDRAM and Bus Master. Figure 1 demonstrates the block diagram of the DDR SDRAM Memory Controller that is in the middle of the bus master and SDRAM [2]. The bus master can be a microprocessor depending on the application.

SDRAM's are divided in view of their data transfer rates as Single data rate SDRAM in which the information is exchanged on each rising edge of clock whereas in double data rate (DDR) SDRAM's the data is exchanged on each rising edge and each falling edge of the clock and as a result, the efficiency is increased. DDR SDRAM Controllers are faster and effective than its counter parts. They permit information exchange at a quicker rate without much increment in clock frequency and bus width.

II.DDR SDRAM CONTROLLER ARCHITECTURE

The Controller architecture of DDR SDRAM is shown in Figure 2. It is divided into three modules namely:

1.Main control module

2.Signal generation module
3.Data path module.

The bus master provides address and data to the memory controller which generates command signals and depending upon these signals data is read or written from or to SDRAM respectively. Two state machines and a refresh counter are present in the main control module. The purpose of using state machines in the main control module is for the initialization of the SDRAM and for generating the commands to the SDRAM. In the main control module Initial FSM generates iState while command FSM generates cState which are according to the signals given by the bus master. Based on iState and cState signal generation module generates address and command signals to SDRAM. The data path module acts like a bridge in between bus master and SDRAM which transfers data between bus master and SDRAM.

The important features of DDR SDRAM Controller are as follows
1.The controller simplifies Read and Write operations to DDR SDRAM
2. The initialization of DDR SDRAM is done using separate state machines internally.
3.The read and the write cycle access time is enhanced based on the parameters like CAS latency and burst length of the DDR SDRAM.
4.DDR SDRAM is refreshed automatically by the controller.
Three sub modules are present in main control module they are:
1.Initialization FSM module (INIT_FSM).
2.Command FSM module (CMD_FSM)
3.Counter module

A. Main control module
Before the normal memory access can be performed from DDR SDRAM it must go through the process of initialization by a series of commands which is done by initialization FSM. The responsibility of initialization finite state machine in the main control module is to initialize the DDR SDRAM controller so it can be ready for normal memory access.

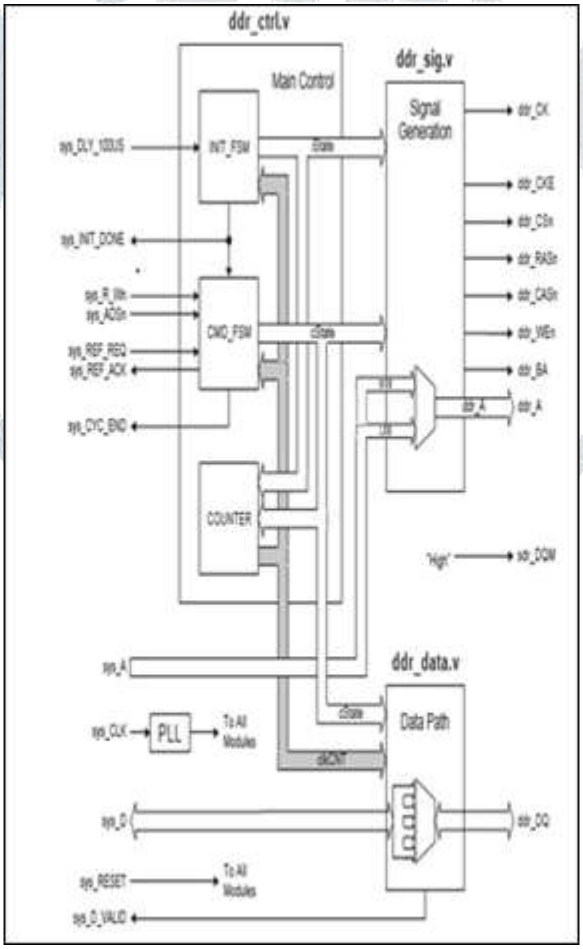


Fig. 2. DDR SDRAM Controller Architecture

The state diagram of the initialization FSM (INIT_FSM) is shown in Figure 3. Initialization FSM will be in i_IDLE state until reset signal is high. After 100us of clock stabilization delay the controller will be active to read or write the data when reset signal is low.sys_dly_100us is the signal which constantly checks for this process and when sys_dly_200us is high it is the indication that the clock stabilization delay has taken place. The DDR is initialized once clock/power stabilization is over after which the state of initialization FSM changes from i_IDLE to i_NOP state. After one clock cycle initialization FSM will again change its state to i_PRE from i_NOP .

PRECHARGE command will be generated by the initialization FSM in i_PRE state which will be given to the all banks which are present in SDRAM.After the generation of PRECHARGE command by the initialization FSM, the controller will then switch to the next state which is AUTO REFRESH state after a time delay of i_tRP.Two AUTO REFRESH (i_AR1, i_AR2) commands are present in initialization FSM after i_PRE state as shown in Figure 3. DRAM memory is refreshed using these refresh commands. The next state after refresh is i_MRS state termed as LOAD MODE REGISTER which comes after satisfying a time delay of i_tRFC1 and i_tRFC2 .The duty of LOAD MODE REGISTER state is to set SDRAM to a specific mode of operation. The next state will be i_ready state after satisfying a time delay of i_tMRD. Now if initialization FSM is in i_ready state it indicates that SDRAM is ready for normal memory access. Once i_ready state is reached the signal sys_INIT_DONE becomes high which indicates that initialization of DDR SDRAM is completed. For The PRECHARGE, AUTO REFRESH, LOAD MODE REGISTER states the commands used respectively are i_PRE, i_AR, and i_MRS.

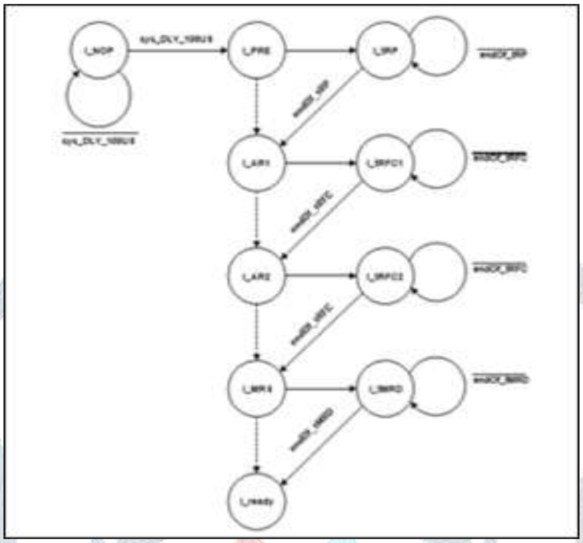


Fig. 3. Initialization FSM

The read, write operations of the SDRAM are controlled by COMMAND FINITE STATE MACHINE (CMD_FSM) shown in Figure 4.

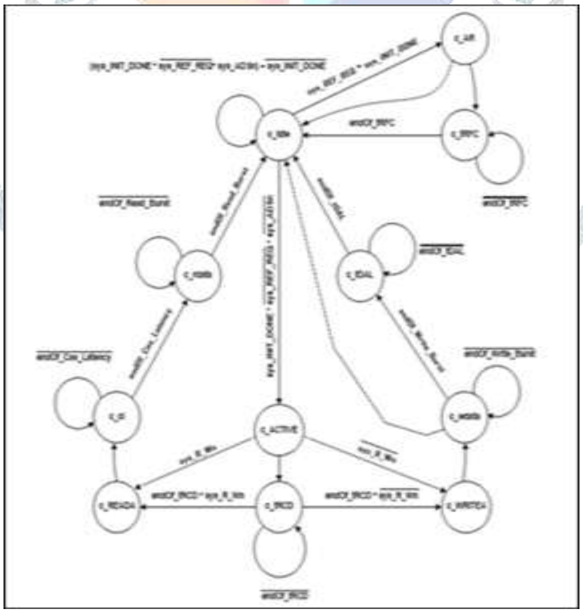


Fig. 4. Command FSM

During reset of SDRAM the CMD_FSMwill be in C_IDLE state. Even After SDRAM comes from reset CMD_FSM will be present in c_IDLE until sys_INIT_DONE is low which means that SDRAM initialization is still not completed. Initialization of SDRAM is completed when we get sys_INIT_DONE signal as high. Now the controller will enter auto refresh, read or write modes depending upon the signals. After initialization is completed and when the latch_ref_req is high, the controller refreshes SDRAM by entering into auto-refresh state. The controller enters active state once the latch_ref_req goes low. To open each row for read or write operation ACTIVE command is issued. Sys_R_Wn is the signal which determines either data is to be written to SDRAM or read from SDRAM. If sys_R_Wn is high then controller reads from SDRAM as signal c_READA goes high when sys_R_Wn is high. If sys_R_Wn is low controller writes to SDRAM as c_WRITEA is high when sys_R_Wn is low.In read operation the time delay of c_cl should be satisfied before controller reads data from SDRAM and transfers it to bus master.

After read operation is completed the controller switches to c_IDLE state. To perform write operation the controller switches from c_WRITEA to c_wdata state to write data from bus master to SDRAM, and then switches to c_tDAL. After data is written the controller switches to c_IDLE state.

B.Data path module

The data path module to perform read and write operations is shown in figure 5.The data path module depends on cState to perform read/write operations data path module depends upon cState generated by the CMD_FSM in the Main Control module. Data path module acts as a bridge between bus master and SDRAM for performing read/write operations.

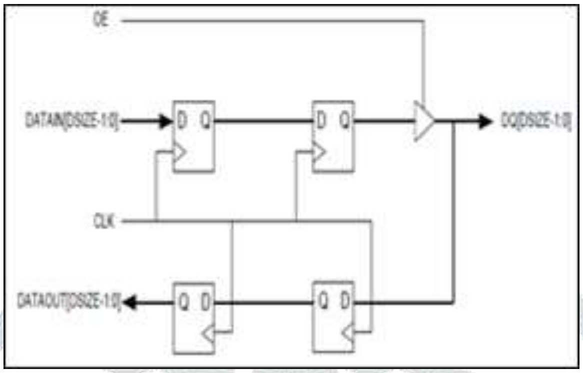


Fig. 5. Data Path Module

C.Signal generation module

Command signals to the DDR SDRAM will be generated by DDR SDRAM Signal generation module. ddr_add is the command signal for generating addresses while for selecting column and row address the command signals are ,ddr_casn and ddr_rasn; for. iState and cState generates these command signals which are received from the CMD_FSM and INIT_FSM present in the Main Control module.

III.DDR SDRAM INTERNAL ARCHITECTURE

SDRAM's have multi-bank architecture and organized in banks, rows and columns as shown in figure 6. The accessing of memory in SDRAM is done in the following sequence of operations as below

1.The requested row is activated and copied to the row buffer of the corresponding bank.

2.Read and/or write bursts are issued to the active row.

3.The row is precharged and stored back into the active row.

The above sequence of operations is done by memory controller to access data in SDRAM by giving corresponding commands. But when bit size of memory controller is less we can access only one bank at a time.

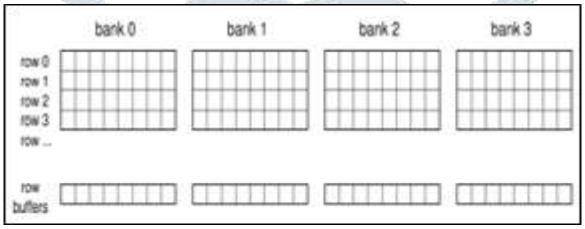


Fig. 6. DDR SDRAM Internal Architecture

Each sequence of operation is depicted by the following figures

1.The requested row is activated and copied to the row buffer of the corresponding bank shown in figure 7.

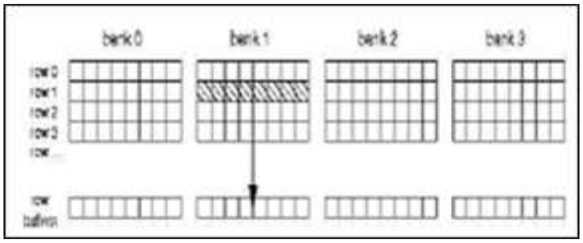


Fig. 7. DDR SDRAM Row Activation

2.Read and/or write bursts are issued to the active row is shown in figure 8.

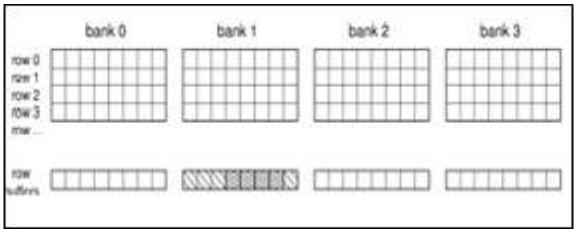


Fig. 8. DDR SDRAM Read/write bursts

3.The row is precharged and stored back into the memory array is shown in figure 9.

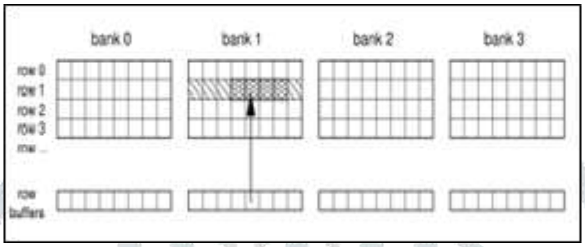


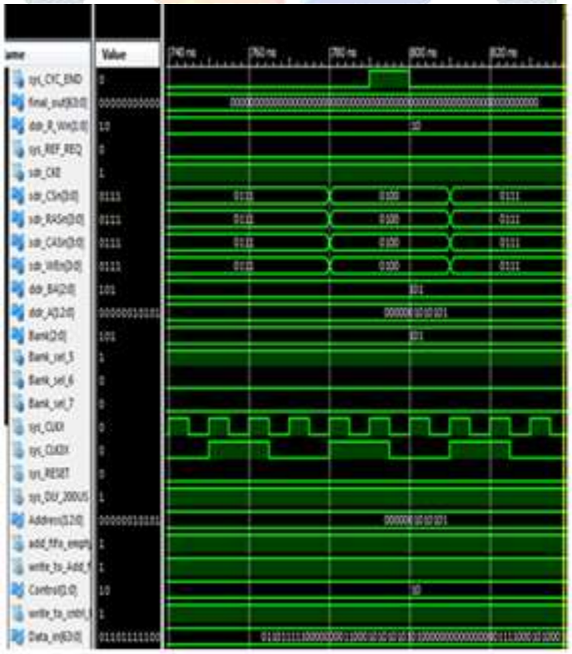
Fig. 9. DDR SDRAM Row Precharge

Normally when DDR SDRAM controller data width is 64-bit it is possible only to access one bank of SDRAM at a time. So, in our project we are increasing the data width of DDR SDRAM controller to 128-bit so that Bank control bits are increased so that we can access multiple banks at same time.

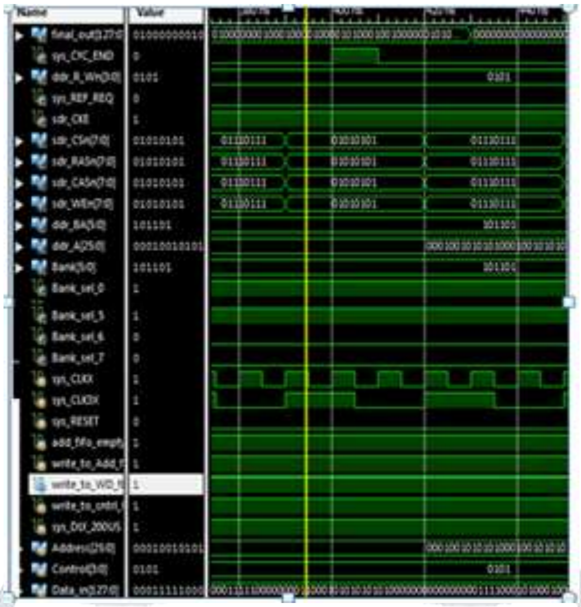
IV.EXPERIMENTAL RESULTS

The Design is simulated after combining the BUS Master, DDR SDRAM Controller and the DDR SDRAM. Verilog HDL is used to model the controller. The written Verilog HDL Modules have successfully simulated and verified using Xilinx ISE 14.3.

Simulation result:



Simulation result of 64-bit DDR controller.



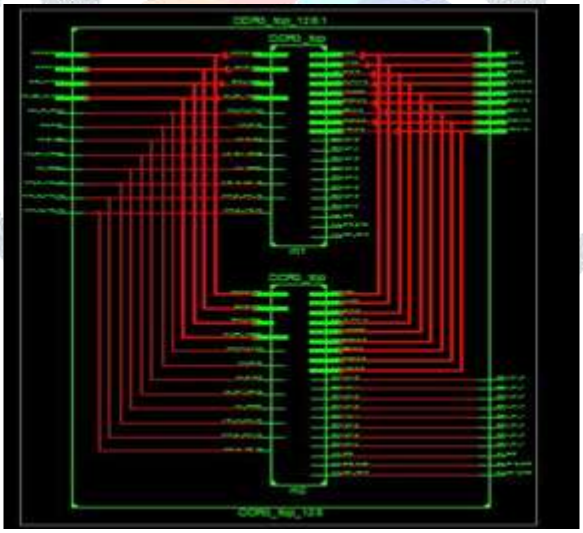
Simulation result of 128-bit DDR controller

Figures show the timing diagram of for both 64-bit and 128-bit controller. In 64 -bit controller only one bank of 8 banks can be accessed at one time. In 128-bit controller two banks can be accessed at same time of total 8 banks.

Due to increase in the number of banks the data speed can be increased i.e. the data can be written into the multiple banks simultaneously. Similarly, data can be read from the multiple banks at same time which increases the speed of read and write operation.

The RTL Schematic of 128-bit DDR SDRAM controller is shown in below. From the figure it can be depicted that two 64-bit DDR SDRAM controllers are instantiated into a single module to form 128-bit DDR SDRAM controller.no other changes are made to architecture 64-bit controller.

RTL Schematic:



RTL Schematic of 128-bit DDR controller

Synthesis Results of 128-bit DDR SDRAM controller is shown in the below Table 1 for SPARTAN-3E FPGA

TABLE 1:

Synthesis summary		
No of slice flipflops	580 of 9312 used	6% utilized
No of 4 input LUT’S	719 of 9312 used	7% utilized
No of GCLKS	2 of 24 used	8% utilized
Total delay(ns)	6.160	

V.CONCLUSION

Design of Double Data Rate (DDR) SDRAM Controller is designed for 128 bits to access multiple banks at same time. The DDR SDRAM Controller architecture is implemented in Verilog HDL. The Synthesis results are obtained using Xilinx ISE 14.3. Future work may include pipelining of many DDR SDRAM'S to same controller which can be done applying some specific algorithm.

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