DESIGN IMPLICATIONS OF ALL DIGITAL PHASE LOCKED LOOP – A STATE OF ART REVIEW

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Abstract: All Digital Phase Locked Loop (ADPLL) is a category of PLL whose all efficient blocks are realised in purely digital form and it is most frequently used in the field of digital communications. The paper presents a review on different designing techniques of ADPLL blocks implementation, i.e., Phase Detectors (PD), loop filters, Digitally Controlled Oscillators (DCO) along with their compatibilities and implications. There are several challenges in the designing of each block of ADPLL that will be considered while designing. These are also detailed in the paper.

Keywords: **ADPLL, Phase detectors, loop filters, DCO**.

I. INTRODUCTION

Phase Locked Loop (PLL) is an analog circuit which receives a reference input and performs control operation on it to adjust the output signal in phase with the reference signal. The output signal frequency is programmable, rational multiple of a fixed input frequency. When phase and frequency of input and reference signals are synchronised, the PLL is said to be synchronised. The PLL found applications in the clock recovery, high performance microprocessors, cellular phones, computers, televisions, radio, motor speed controller, DSP based carrier phase and symbol tracking algorithms, GPS receivers and communication systems. Standard PLL suffers from noise coupling, their integration in deep sub micron technologies is much tougher and usable voltage ranges decrease with every new integration step [13]. Last but not the least extensive re-design has to be done any time the technology or frequency specification is changed [15].

All Digital Phase Locked Loop (ADPLL) overcomes these difficulties. ADPLL yield better portability, stability, programmability, testability, minimise the design cost and time. ADPLL is less sensitive to external noise and process, voltage and temperature (PVT) variations because all building blocks are realized with digital circuits [3].

The rest of the paper is organised as under. Second section discusses the ADPLL architecture in detail. Third section describes the ADPLL lock procedure for word signal; fourth section compares various parameters of the existing ADPLL and their consequences. In section five the various ADPLL are compared based on some performance parameters and existing problems followed by the conclusion.

II. ADPLL – ARCHITECTURE

A standard ADPLL is a negative feedback system that consists of three major blocks a Phase Detector (PD), digital loop filter, a Digitally Controlled Oscillator (DCO) and a programmable frequency divider (divide by N) is optional to match the frequency of the two signals [7]. All blocks of ADPLL are realised digitally completely. Digital means firstly system consists exclusively of logical devices. Secondly, the signals within the system are digital i.e. either they are binary or word signals. Lastly all fundamental blocks must be implemented by purely digital components. The block diagram of ADPLL is shown in Fig. 1.

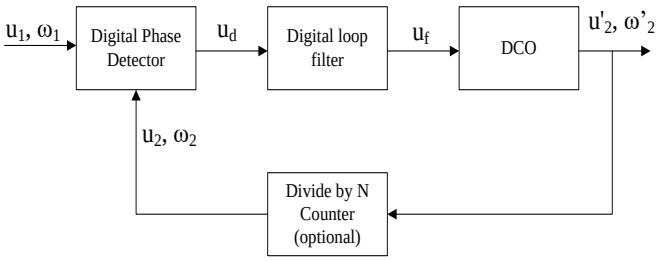

Fig.1 ADPLL Block Diagram [12]

u_1 is the reference signal and its frequency is ω_1. u_2 is the DCO generated signal with frequency ω_2. The digital phase detector compares these two signals and generates an error signal u_d. This u_d signal is either phase error or phase and frequency error signal. On the basis of error signal digital loop filter generates the control signal u_f for the DCO. Depending upon the control

signal u_f, DCO increases or decreases the frequency of the signal and generates and output u'_2 with frequency ω'_2. This frequency can either similar or be higher than the reference signal in terms of frequency. If it is higher, then one additional block divide by N counter is used which divides the DCO generated output u'_2 by a factor N which is multiple of 2 and generates the signal u_2 with frequency ω_2.

2.1 Phase Detector

Phase Detector (PD) produces one or more Pulse Width Modulated (PWM) signals representing the phase difference between the two signals viz. reference signal and frequency divider output. Phase detector falls into two broad categories based on memory. First category is memory – less phase detectors which are based on the multiplier circuit. These are:

2.1.1 EXOR Phase Detector

It uses the digital input waveforms for phase detection. It is based on the assumption that two signals are symmetrical square waves [6]. The output is averaged and integrated. It may lock to a multiple of clock frequency i.e. it also locks on harmonics of the input. When signals are not symmetrical then averaged signal gets clipped at some intermediate level. Due to clipping of signal loop gain reduces and results in smaller lock – in range and pull – out range. It has good noise rejection and suitable for communication applications.

2.1.2 JK Flip Flop Phase Detector

It is edge triggered circuit and signals waveform symmetry is not important. A positive edge appearing at 'J' input makes output HIGH and a positive edge appearing at 'K' input makes output LOW [6]. As it is edge sensitive circuit it can only be used only when no cycles of reference signal are missing.

2.1.3 Phase Frequency Detector (PFD)

It not only detects the phase difference but also the frequency difference between the reference signal and the feedback signal. Basically it acts as a tri – stable device. The actual state of PFD is determined by the positive going transients of the two signals which it received at the inputs. The two outputs viz 'UP' and 'DN' of the PFD have to be converted to a single output by using some circuitry which drives the loop filter [16]. The duty cycle of the output signal depends on the ratio of the two frequencies [6] as shown in Fig. 2.

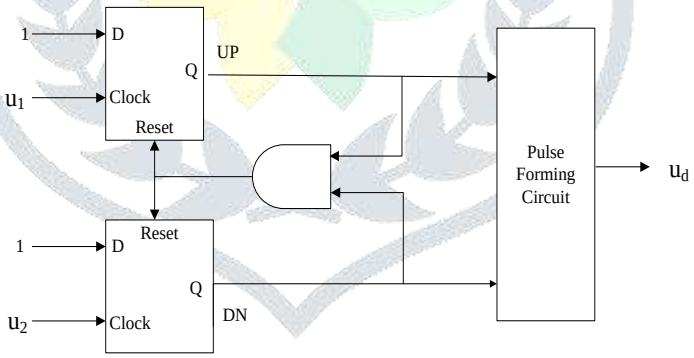

Fig.2. PFD Block Diagram [16]

The PFD overcomes the problem of locking on a harmonic of the data encountered in EXOR PDs. PFD has the advantage of large frequency range but it has poor noise rejection and dead-zone problem. Dead zone is a small difference in the phase of inputs that a PFD will not be able to detect.

Second category is memory based PD which requires sequential circuits such as gates and flip-flops (FF). They are used when the input signals are free from noise and have well-defined level transitions. They are having extended phase detector range, improved frequency acquisition and insensitive to input signal levels. When digital word signals are used instead of bit signals number of additional phase detector circuits are available in this category. The PD's are:

2.1.4 Flip flop based PD

It is an evolution of simple JK – FF phase detector. A FF counter based PD uses an edge triggered SR – FF in combination with a counter [1]. The counter is reset on every positive edge of the reference signal. The output of the FF is used to gate the high frequency clock signal into the counter. The content of the counter is proportional to the phase error which is n – bit output [6] as shown in Fig. 3.

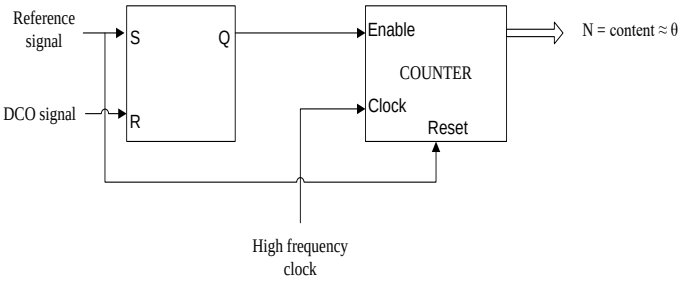

Fig.3. Flip Flop based PD Block Diagram [6]

2.1.5 Nyquist Rate PD (NRPD)

The name stems from the Nyquist theorem, which states that a sampled signal can be reconstructed only when the sampling rate is more than twice the highest frequency component present in the signal. This PD is used if the input is an analog signal [1]. In Fig. 4 the analog signal is converted into a digital signal using an Analog to Digital Converter (ADC) sampled at a rate greater than the Nyquist rate. Both signals are word signals and are multiplied together by a software multiplying program [21]. Average value of the multiplier is filtered out by a succeeding digital loop filter.

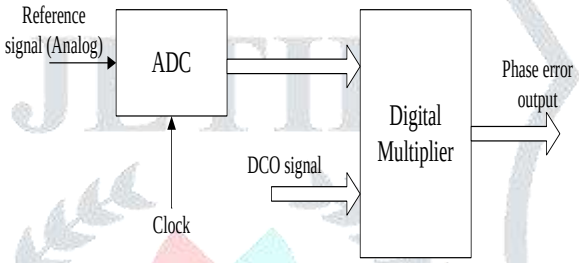

Fig.4. NRPD Block Diagram [6]

2.1.6 Zero crossing PD

In this detector, reference signal is analog signal and the other signal which is received from DCO is binary signal. The reference signal is converted into digital signal using ADC. The positive transition of binary signal is used to clock the ADC so the reference signal is sampled once during every reference cycle. The output signal of ADC is proportional to the phase error of the two signals and is held in a register until next conversion is completed [6].

2.1.7 Hilbert transform PD

Hilbert transformer is the key element of this PD. The special feature of this transformer is its gain is one at all frequencies. For this PD, DCO is used to generate two signals which are in – phase quadrature and clock signal is required to perform all the operation whose frequency is M times signal frequencies [6].

2.1.8 Digital averaging PD

In this PD, the trigonometric functions are obtained by simply averaging the output of the multiplier over an appropriate period of time. It is suitable for the software implementation.

2.2 Digital loop filter

All digital phase detectors are not compatible with all types of digital loop filters. The inputs of digital loop filter select which type of phase detector can be used with it. There are various types of digital loop filter:

2.2.1 UP/DN Counter

The UP/DN Counter is the simplest type of loop filter, which is used in conjunction with the PFD. It can also be used in conjunction with EXOR or JK – FF PD's. The PD's used should deliver two pulses namely UP/DN based on the comparison between frequencies of the two inputs. These PD output pulses are used to increment or decrement a counter and the output is weighted sum of these UP/DN pulses. It has the limitation that it is very crude approximation as the pulses do not contain any information about the actual magnitude of the phase error. These pulses are a result of the relative comparison of the two signals [6] shown in Fig.5.

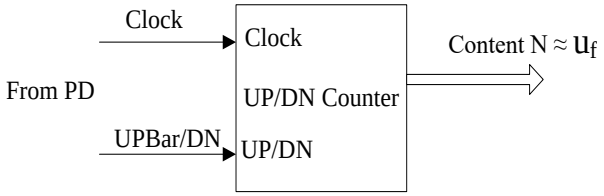

Fig.5. UP/ DN counter loop filter [6]

2.2.2 K Counter loop filter

It works together with the EXOR or the JK – FF PD's. A K Counter loop filter uses two independent counters, UP and DN counters to generate Carry and Borrow Signals. The output of PD controls the operation of the two counters. K is the modulus of the both the counters and is a power of 2. It generates two outputs 'Carry' and 'Borrow' signals which are used to control the frequency of a DCO signal shown in Fig. 6.

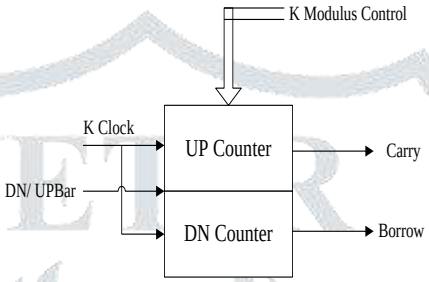

Fig.6. K counter loop filter [6]

2.2.3 N before M counter

It operates in conjunction with a PD generating UP/DN pulses such as a PFD and generates two output pulses 'Carry and 'Borrow' as shown in Fig. 7. The N-before-M counter uses two counters, the divide by M counter and the divide by N counter where M > N always. The Carry pulse is generated when a majority of N pulses have been 'UP' pulses. Similarly, the Borrow pulse is generated when a majority of N pulses have been 'DN' pulses. The performance of this filter is non linear [6].

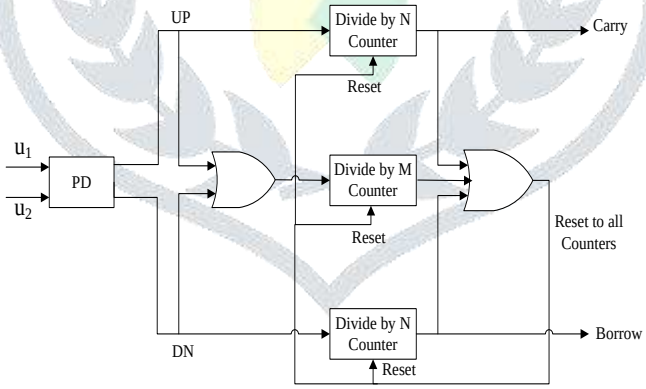

Fig.7. N before M counter loop filter [6]

2.2.4 Digital Filter

It is compatible with an n- bit parallel input signal and generate n - bit output signal. Its architecture is complicated.

2.3 Digital Controlled Oscillator

The key component for an ADPLL is the DCO which dictates the maximum frequency, the frequency range and the resolution. For some applications these features of DCO are the chief considerations [7]. For word signals, the main criterion for DCO designing is to provide enough control word resolution and maintain acceptable jitter [5]. There are different types of oscillator:

2.3.1 Path delay oscillator

The Path Delay Oscillator proposed in [21] contains logic gates to form a closed ring oscillator with an odd number of inversions. It occupies a small area and has a wide tuning range [8]. It is not suitable for high frequency requirements. The operating frequency is lower and phase noise is poorer compared to analog oscillator.

2.3.2 Schmitt trigger based current driven oscillator

The design uses Schmitt trigger inverter, a big capacitor and several control MOS transistors [19]. Due to high capacitance, the capacitor is usually connected externally. The external capacitance makes the system complicated and degrades the performance.

2.3.3 Current starved ring oscillator

It is designed by using MOS switches to obtain different frequencies. Its benefit is having good linearity and hence finds its application in microprocessor systems [20]. The size of this DCO is large and may cost a lot of hardware.

2.3.4 Divide by N counter DCO

It is suitable when filter generates n – bit parallel output. It uses a fixed high frequency oscillator and a divide by N counter to scale down the high frequency shown in Fig. 8.

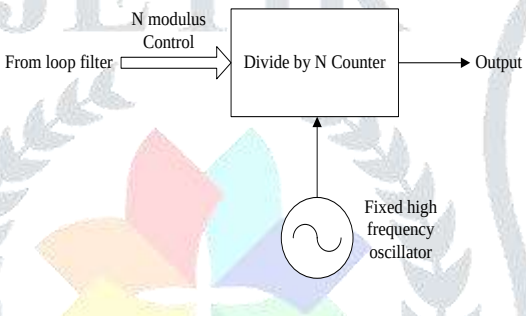

Fig.8. Divide by N counter DCO [13]

2.3.5 Increment – decrement (ID) counter

This DCO is used in conjunction with those filters that generate two pulses Carry and Borrow pulse. It is sensitive on the positive going edges of the input pulses and uses a toggle flip flop shown in Fig. 9.

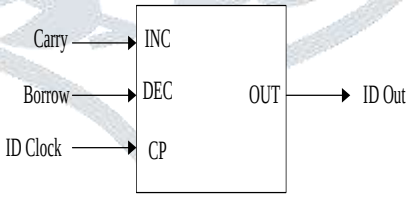

Fig.9. ID counter DCO [18]

2.3.6 Waveform synthesizer DCO

It is ideal for software implementation and generates sine wave of different frequencies shown in Fig. 10. It generates lower frequency signals with higher resolution.

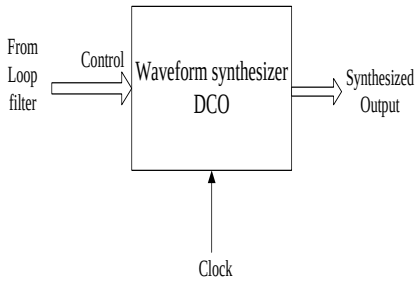

Fig.10. Waveform Synthesizer DCO [6]

Among them ring oscillator is most widely used along with other digital components to maintain the jitter specifications. In general, for the word signal, DCO consists of two stages one is coarse-tuning and second is fine tuning stages [11]. These two stages generate the coarse control code and fine control code in different locking modes of DCO. The DCO frequency is updated with respect to these signals from digital loop filter. Because of PFD dead band zone and the reference clock noise, the DCO control code has small variations in phase [3].

2.4 Programmable Frequency Divider

In order to match the frequency of the output of the DCO signal with reference signal sometimes it is required to divide the frequency of DCO with some factor N which is a multiple of 2. It also compensate for the phase error.

III. ADPLL LOCK PROCEDURE

When the signal is word signal, the phase locked procedures for the ADPLL is done in four steps: frequency acquisition, phase acquisition and frequency and phase maintenance respectively. In frequency acquisition mode, frequency search algorithms are used to capture the frequency. Generally binary search algorithm is used which sweeps the DCO frequency range to match the reference signal. It changes the DCO coarse control word based on the output of the PFD. When the frequency is locked with the reference signal frequency the frequency acquisition mode is completed and the ADPLL enters into the phase acquisition mode. The filter increments or decrements the DCO control word until the PD senses a change in the phase polarity of the reference and the DCO signal. Phase acquisition mode is completed when PD senses the change in polarity. At the end of phase acquisition mode ADPLL enters into the frequency maintenance mode and phase maintenance codes [7]. In these modes a special algorithm is applied to maintain the required frequency and phase by changing the DCO fine control word to eliminate the frequency and phase error between reference signal and DCO divide by N signal [17]. After the DCO coarse tune and fine tune steps, a stable feedback loop is settled and a signal may be generated to indicate the frequency is locked successfully depending on the circuit design [16].

IV. DISCUSSION

There are few parameters of ADPLL that decides the performance of it. Most important parameters are lock range, lock – in time, phase error, jitter. With technology advancement the numbers of transistors are increasing on the chip day by day. In the VLSI era of portable devices power dissipation is a major concern. For the power reduction there are certain techniques to be used which may require some extra circuitry which in turn increases the area. A trade off between area and power dissipation should be managed. Second issue in designing is jitter which is defined as the frequency domain analysis of rapid short term fluctuations in the phase of the wave caused by time domain instabilities. Phase jitter can be made small by increasing the clock frequency. The comparison among various parameters is shown in Table1.

Table 1- Comparison of various ADPLL Parameters

Performance Parameter	**[3]**	**[8]**	**[9]**	**[10]**	**[4]**	**[5]**
Process	0.18µm CMOS	0.13µm CMOS	0.18µm CMOS	0.35µm CMOS	65nm CMOS	0.18µm CMOS
Area	0.7735 mm^2 without output buffer	0.42 mm^2	0.084mm^2	0.45*0.24 mm^2	6600 μm^2	0.1785 mm^2
Power Dissipation	35 mW @ 1.25 GHz	7.22 mW	7.2 mW @ 1 GHz		780 µW @ 900 MHz	5.49 mW @ 1 GHz

Frequency Range	253.9MHz – 1.367GHz	1.9 GHz – 3.1 GHz	96.1 MHz – 1.014 GHz	1.68GHz	0.39 GHz – 1.41 GHz	860MHz – 1 GHz
Supply voltage	1.8 V	1.2 V – 1.8 V	1.8 V	3.3 V	0.8 V	1.8 V
Peak to Peak jitter	32.5 ps @ 1.25 GHz	60 ps @ 2.4 GHz	35.6 ps @ 1 GHz	123 ps @ 1.68 GHz		28.75 ps @1 GHz
RMS Jitter	8.884 ps @ 1.25 GHz	4.01 ps @ 2.4 GHz	4.3 ps @ 1 GHz		1.7 ps @900 MHz	1.31 ps @ 1 GHz

V. CHALLENGES IN ADPLL

There are several challenges in the design of the ADPLL. Phase noise of the ADPLL is high compared to mixed signal design [15]. The main challenge in the design of phase detector is to obtain very high operating frequency with minimal power dissipation [2] and due to reset path in the phase detector reset delay is introduced produce a large dead zone. Therefore operating frequency and dead zone problem should be considered while designing the PD. Wide operating range decline the maximum frequency range [7]. The major block that contributes to power consumption is DCO. Due to the switching delays glitches are introduced into the oscillator. In a portable device era power consumption should be minimum so that battery can run more time without charging.

VI. CONCLUSION

In this paper we discuss about the different types of implementation that are possible for each block and with their pros and cons. The comparisons of various existing ADPLL are compared in terms of various parameters and their analysis. Existing ADPLL structure faces some challenges. The future work is to design a low power small dead-zone PFD and the DCO for higher operating range and its implementation.

VII. ACKNOWLEDGEMENT

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REFERENCES

[1]. C. W. Chang, K. Y. Chang, Y. H. Chu, S. J. Jou, " Near-threshold All- Digital PLL with dynamic voltage scaling power management", *Electronics Letter*, Vol. 52, No. 2, pp. 109 – 111, January 2016.
[2]. R.K.Sutar, M.Jasmin and S. B. Hemalatha, "Implementation of Low power ADPLL", International journal of Innovative research in Computer and communication Engineering", 3733 – 3739, Vol. 3, Issue 4, April 2015.
[3]. J.M.Lin , C.Y. Yang, "A Fast Locking All- Digital Phase Locked Loop With Dynamic Loop Bandwidth Adjustment*", IEEE Trans. On Circuits and Systems*, Vol. 62, No. 10, pp. 2411 – 2422, Oct. 2015.
[4]. W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, A. Matsuzawa, " A Fully Synthesizable All-Digital PLL Interpolative Phase Coupled Oscillator, Current-output DAC, and Fine- resolution Digital Varactor using Gated edge Injection Technique", *IEEE Journal of Solid – State Circuits*, Vol. 50, No.1, 2015.
[5]. Y. H. Ho, C. Y. Yao, " A low – jitter Fast – locked All – Digital Phase – Locked Loop with Phase – Frequency – Error Compensation*", IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2015, in press.
[6]. Roland E. Best, "Phase-Locked Loops: Design, Simulation & Applications", *McGraw-Hill Professional Engineering*, 4th Edition .
[7]. C. W. Tzeng, S. Y. Huang, P.Y.Chao, "Parameterized All- Digital PLL Architecture and its Compiler to Support Easy Process Migration", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 3, pp. 621 – 630, March 2014.
[8]. M. Song, I. Sung, S. Pamarti, C. Kim, " A 2.4 GHz 0.1- Fref- Bandwidth All- Digital Phase- Locked Loop With Delay- Cell- Less TDC", *IEEE Transactions On Circuits and Systems –I: Regular Papers*, Vol. 60, No. 12, pp. 3145 – 3151, Dec. 2013.
[9]. P. Y. Chao, C. W. Tzeng, S. Y. Huang, C.C. Weng, S.C. Fang, " Process- Resilient Low-Jitter All-Digital PLL via Smooth Code- Jumping", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 21, No. 12, pp. 2240 – 2249, December 2013.
[10]. S.K.Kao, F.J.Hsieh, "A fast locking PLL with all digital locked-aid circuit", *International J. Of Electronics*, Vol. 100, No.2, pp. 245- 258, Oct. 2013.
[11]. K. H. Cheng, J. C. Liu, H. Y. Huang, "A 0.6V 800 MHz All- Digital Phase- Locked Loop with a Digital Supply Regulator", *IEEE Transactions on Circuits and Systems – II: Express Briefs*, 2012, in press.
[12]. V. Kratyuk, P.V. Hanumolu, Un – Ku Moon, K. Mayaram, "A Design Procedure for All – Digital Phase Locked Loops based on a charge pump phase locked loop analogy*", IEEE Trans. On Circuits and Systems – II : Express Briefs*, Vol. 54, No. 3, pp. 247 – 251, March 2007.
[13]. S. Moorthi, D. Meganathan, D. Janarthanan,P.P. Kumar, J.R.P. Perinbam, " Low jitter all digital phase locked loop based clock generator for high speed system on-chip applications", *International J. Of Electronics*, Vol.96, No. 11, pp. 1183-1189, Nov. 2011
[14]. M. Kumm, H. Klingbeil, P. Zipf, "An FPGA based Linear All-Digital Phase-Locked Loop", *IEEE Transactions on Circuits and Systems – : Regular Papers*, Vol. 57, N0. 9, pp. 2487 – 2497, Sept. 2010.
[15]. H. Eisenreich, C. Mayr, S. Henker, M. Wickert, R. Schuffny, " A novel ADPLL design using successive approximation frequency control", *Microelectronics Journal 40 Elsevier*, pp. 1613 – 1622, 2009.
[16]. C. C. Wang, C.C. Huang, S. L. Tseng, " A low-power ADPLL using feedback DCO quarterly disabled in time domain", *Microelectronics Journal 39 Elsevier*, pp. 832 – 840, 2008.

[17].C. C. Chung, C. Y. Lee, "An All- Digital Phase Locked Loop for High- Speed Clock Generation", *IEEE Journal of Solid State Circuits*, Vol. 38, No. 2, pp. 347 – 351, Feb. 2003.
[18]. Hiroomi Hikawa, "FPGA implementation of self organizing map with digital Phase Locked Loops", *Neural Networks 18*, pp. 514 – 522, 2005.
[19]. R. Fried, " Low –power digital PLL with one cycle frequency lock –in time for clock syntheses up to 100 MHz using 32,768 Hz reference clock", *Proc. IEEE*, Vol. 84, pp. 291 – 294, Feb. 1996.
[20]. J. Dunning, G. Gareia, J. Lindberg and E. Nuckolls, " An all – digital phase –locked loop with 50 – cycle lock time suitable for high performance microprocessors", *IEEE Journal of Solis – State Circuits*, Vol. 30, pp. 412 – 422, April 1995.
[21]. R. Saban and A. Efendovich, "A fully – digital, 2 – MB/sec CMOS data separator", *ISCAS'94*, Vol. 3, pp. 53 -56.