A 13 LEVEL ASYMMETRIC MULTILEVEL INVERTER WITH REDUCED NUMBER OF DEVICE COUNT.

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Abstract : In this paper an envelope type topology for asymmetrical MLI with less number of switches is proposed. This topology produces 13 levels with 10 switches and 4 DC sources. The features of the proposed topology are better quality than similar topologies with reduced count of semiconductors switches and DC sources. The main advantage of proposed topology is to create a negative level without any additional circuit which reduces the voltage stress on the switches. To achieve higher levels cascade connection is also possible of this topology. The performance of the proposed topology is validated by using MATLAB Simulink simulation.

***Key Words*- Asymmetric, components, Matlab, E-Type, multilevel inverter, Power Converter.**

A. INTRODUCTION

Multilevel inverters (MLIs) have many of advantages such as high quality output voltage, operation in high voltage/power, low stress on switches, etc. Multilevel converters are many arrangements of semiconductor switches with DC links to create n-level output waveform. Multilevel converters have a wide range of applications which has rapidly developed the power electronics with very good possibility for further development [1].They can be used in photovoltaic systems, wind farms, and HVDC systems. They are classified into three main categories [2]: Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascade H-Bridge (CHB). In 1981, NPC was introduced as the first multilevel converter which can be used in medium voltage applications. In 1990s, Flying Capacitor was presented and in 1996, CHB was reintroduced. The design of MLI based on the number of voltage levels, number of semiconductors, output quality, required DC sources and DC link capacitors, THD amplitude, maximum voltage level, creating positive and negative level, modularity, switch stress and total standing voltage (TSV).

Researchers presented different types of modular multilevel inverters. As shown in Fig.1.a, each level is created by two switches and one source in [3]. These levels are connected in series together to achieve positive voltage levels and an auxiliary H-bridge circuit is used to create alternative voltage. Note that, H-bridge switches tolerate more voltages than other switches. As shown in Fig.1.b, the stresses of H-bridge switches are divided between each sub-module [4]. Two capacitors are added for each DC source to reach additional voltage levels with the penalty of using more components. Researchers tried to reach more levels with lower components. Asymmetric MLI which have unequal DC links become interesting so as to improve the quality of output waveform by minimizing the number of components. Modules are arranged based on optimal using of DC links by reduced switches.

The main important factors of MLI design for high voltage applications are high voltage stress on the switches of the output H-bridge. Therefore, a redesign is vital to reduce the stress of the switches by dividing H-bridge voltage into all sub-modules in order to have a uniform stress on every switch which in turn leads to the increasing number of semiconductors and total standing voltage (TSV) of the module. This paper aims to achieve maximum capacity from DC link by a suitable arrangement of switches which improves economic implementation cost, switching frequency, TSV, number of levels, and THD. It presents a new asymmetric multilevel module based on cascade category which creates negative voltage without any additional circuits. Also, it makes 13 levels by reduced switches. The proposed system illustrates multilevel inverters including module description, switching patterns, cascade connection and comparison table with similar modules. Selective harmonic elimination (SHE) is also introduced for for eliminating harmonics.
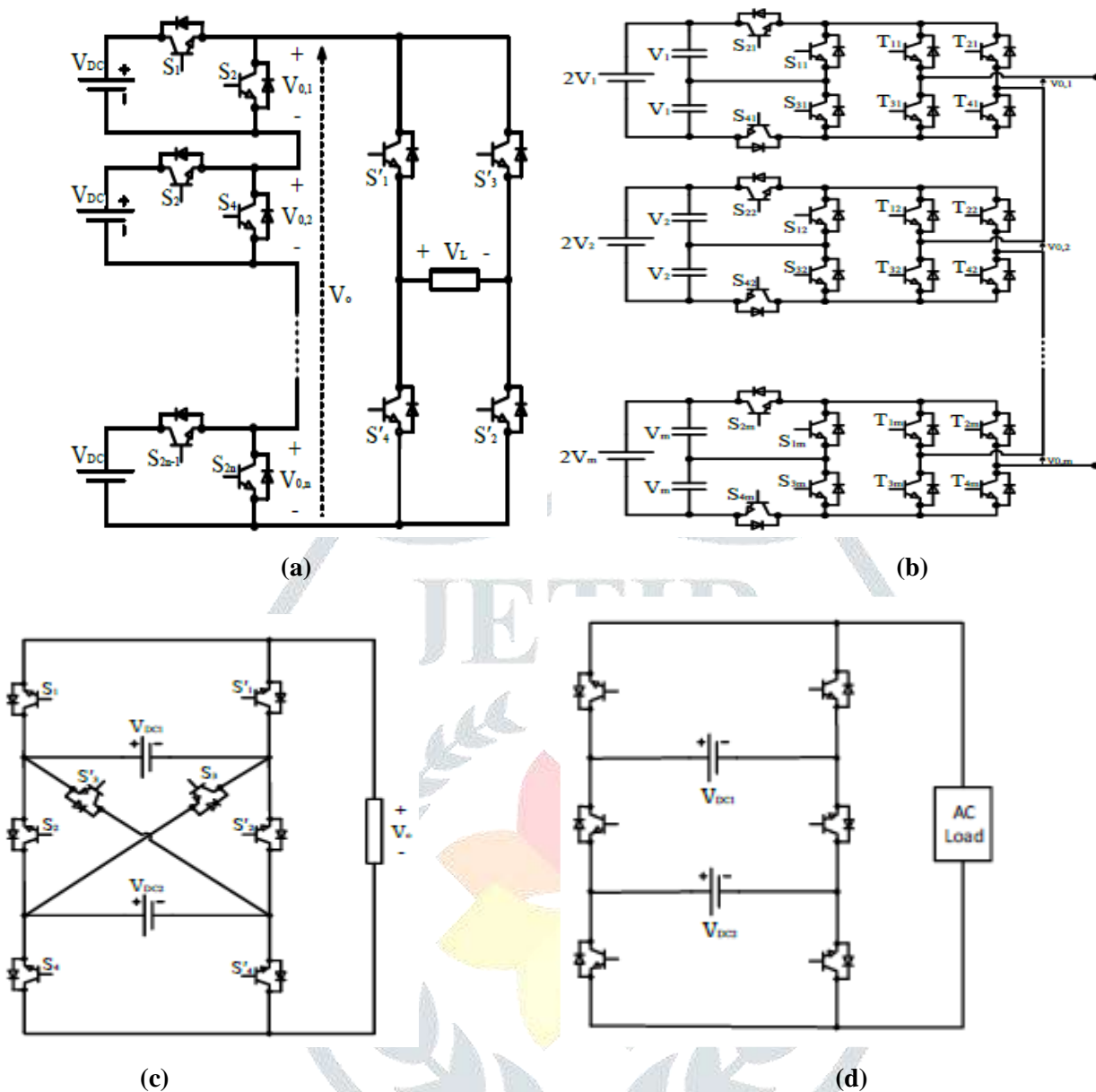
Fig.1 Some topologies of multilevel inverter

B. LITERATURE REVIEW:

A comparative study between the mentioned topology and other famous ones is considered here regarding the required number of semiconductors, DC links, capability to generate negative voltage level and the required number of switches. Among these topologies are: NPC, FC, CHB. According to Table I, the required number of semiconductors (switches and diodes), number of DC links are reduced down to $5(NL-1)/6$ and $(NL-1)/3$ respectively which are lower than other topologies. Note that in this topology a negative voltage level can be obtained without any additional circuit. This ability along with lower components and stress on the devices confirms that the proposed inverter can perform well in comparison with other existing ones.

TABLE I
Comparison Of Some Modular Multilevel Inverter Topology

	NPC	FC	CHB	PROPOSED (E -Type)
No. of switches	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$5(N_L-1)/6$
No. of Diodes	N_L+1	$2(N_L-1)$	$2(N_L-1)$	$5(N_L-1)/6$
No. of DC links	$(N_L-1)/2$	(N_L-1)	$(N_L-1)/2$	$(N_L-1)/3$
Negative level	With at least two	With at least two	With H bridge	Inherent

arms	arms		

C. METHODOLOGY:

A general schematic diagram of a typical asymmetrical multilevel inverter with two DC links for description of multilevel operation is shown in Fig 2. Unequal DC links can be arranged with different connections (through switching components) in order to achieve high number of voltage levels.
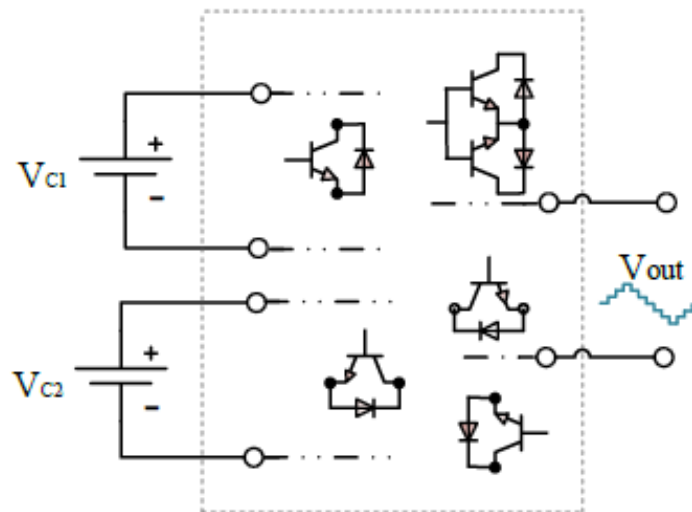

Fig.2 The basic structure of asymmetric MLI

For example, assuming VC1=VDC and VC2=2VDC voltage levels of $\pm VDC$,$\pm 2VDC$ and $\pm 3VDC$ can be obtained by choosing suitable paths from switches and DC links based on the module topology. Using this idea for MLI, a different ratio of DC source voltages may be utilized to generate different levels with number of output voltage. An elimination in harmonic content peak with a same switching frequency and the same configuration is approximately expected by increasing the number of levels of the output voltage in the asymmetrical inverter.

Module Configuration:

This proposed system introduces a new topology of asymmetric multilevel modular with a new component arrangement including 10 switches, 10 diodes and 4 DC sources (two $2VDC$, two $1VDC$) labeled as Envelope type (E-Type). This arrangement synthesizes voltage sources create 13 levels (6 positive level, 6 negative level and zero level) without any extra circuit. The main concept of this circuit is to create different paths from different sides of a DC source to be connected to other sources. Fig.4 shows the E-Type asymmetrical module in where DC sources are placed in the middle of the circuit and are connected together to form different voltage levels via surrounding switch (S1-S6). A bidirectional switch (S7) is required to avoid short circuit of the DC sources on left or right sides of the module. Another bidirectional switch (S8) is also needed to achieve the voltage levels of ±5. Different switching conditions of this structure are shown in Fig.3 and Table I.
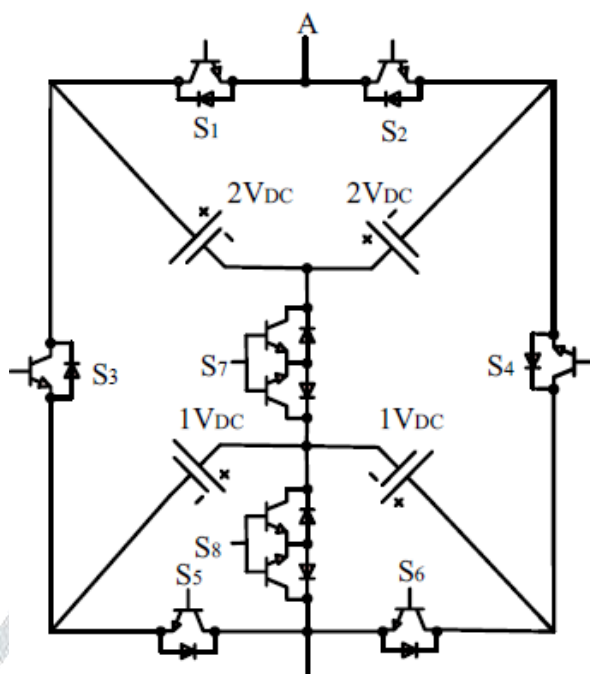
(a) Envelope topology
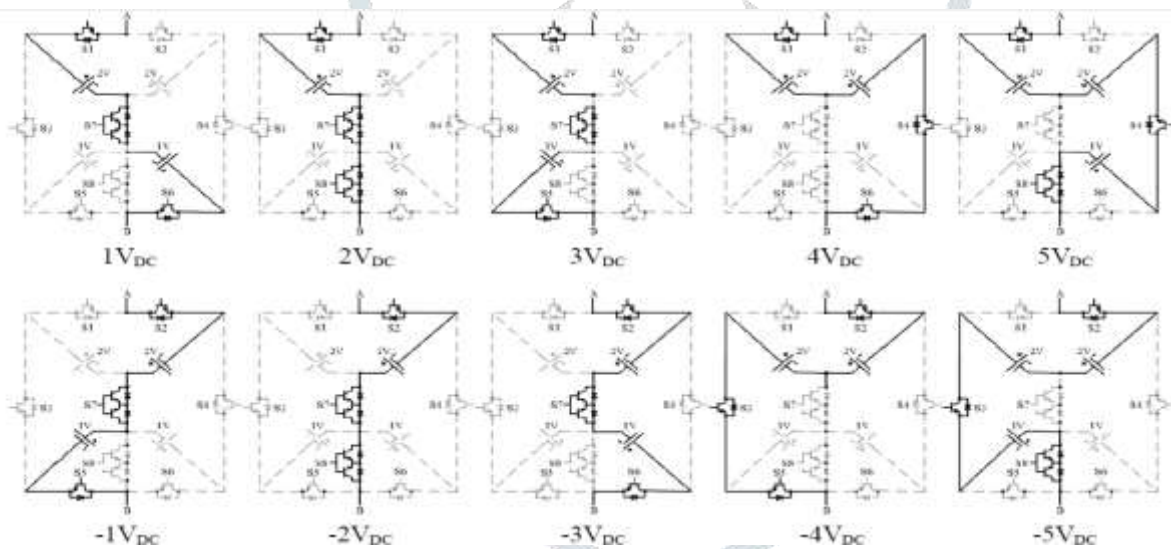
(b) Switching sequences
Fig. 3 E-Type module MLI of proposed system

TABLE II
SWITCHING TABLE

		S1	S2	S3	S4	S5	S6	S7	S8
positive level	$1V_{DC}$	1	0	0	0	0	1	1	0
	$2V_{DC}$	1	0	0	0	0	0	1	1
	$3V_{DC}$	1	0	0	0	1	0	1	0
	$4V_{DC}$	1	0	0	1	0	1	0	0
	$5V_{DC}$	1	0	0	1	0	0	0	1
	$6V_{DC}$	1	0	0	1	1	0	0	0
Negative level	$-1V_{DC}$	0	1	0	0	1	0	1	0
	$-2V_{DC}$	0	1	0	0	0	0	1	1
	$-3V_{DC}$	0	1	0	0	0	1	1	0
	$-4V_{DC}$	0	1	1	0	1	0	0	0

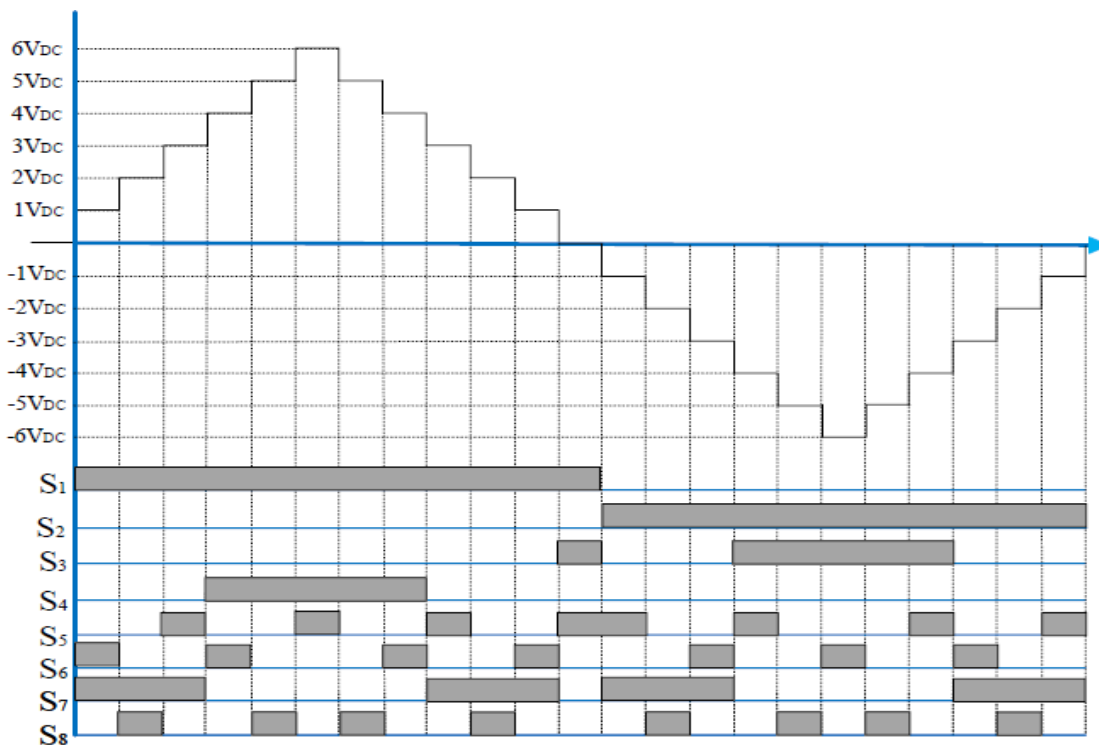|									
-5V$_{DC}$	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
-6V$_{DC}$	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**0**

Fig.4 Switching Pattern Of Proposed Converter In One Cycle

Table II shows, switch pairs (S1, S4) and (S2, S3) belong to positive and negative levels, respectively. In addition, (S1, S2) and (S3, S4) cannot be on at the same time. Fig.4 of proposed inverter shows output voltage with the associated pulse pattern in one cycle of fundamental voltage. As shown in Fig.4, switches S1, S2, S3, S4 and S7 are turned on and off in low frequency which reduces switching losses to a great extent. Other switches also operate in a reasonable switching frequency. Table II shows number of voltage levels, semiconductor components, DC sources and drivers based on number of module units (n) and number of desired levels (NL).

TABLE III
EQUATIONS OF E-TYPE MODULE

	Based on number of module units	Based on number of desired levels
Levels	12n+1	N_L
Number of switches	10n	$5(N_L-1)/6$
Number of Diodes	10n	$5(N_L-1)/6$
Number of DC Links	4n	$(N_L-1)/3$
TSV	20n	$10(N_L-1)/6$

Number of levels are in the form of 12n+1 (n=1, 2, 3, ….)

Fig.3(b) shows all switching states of E-type module. The designing of the proposed module and their switching paths are smartly selected in such a way that there are no positive pole of DC links on the anode side of diode to conduct. Thus, diodes prevent short circuiting of the switches. Also Fig.3(b) illustrates the switching paths does not form any close loop for DC links. It guarantees that short circuiting will be not occurred in E-type module. Multiple pulse width modulation technique is used for control purpose.

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D. SIMULATIONS RESULTS:
Experimental results are carried out to verify the results of simulation and analysis in order to achieve a 13-level sinusoidal waveform. Each level is considered 50 volts, and thus there are two 50 volts and two 100 volts DC sources.

Fig.5 of the proposed E-Type module shows voltage waveform for 10 Hz (Fig.5.a), 50 Hz (Fig.5.b) and 100 Hz (Fig.5.c). FFT analysis for one cycle is illustrated in Fig.5.d where THD is 7.60% of simulation waveform.
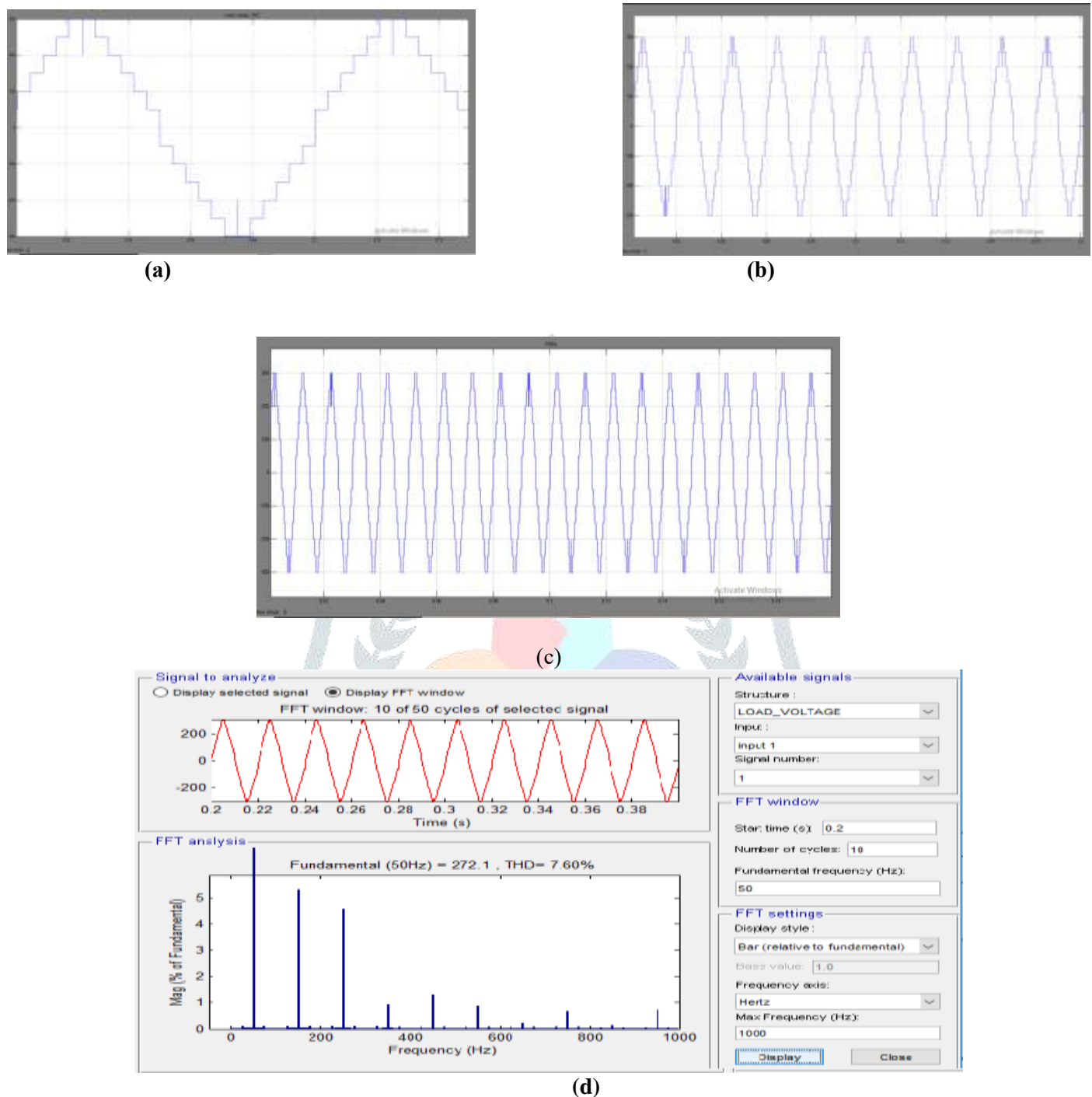

(a)

(b)

(c)

(d)

Fig.5 FFT analysis and Output voltage of proposed system

E. CONCLUSION: In the proposed system a new multilevel inverter topology named as Envelope Type which can produce thirteen levels with reduced switches. As this module can be easily modularized, higher levels are possible with high output voltage, low stress on semiconductors and reducing the number of devices. It uses different paths in case of malfunction for a switch which causes an improvement in the reliability of the inverter. The main feature of the existing module is its ability to produce both positive and negative output voltage without use of H-bridge circuit.

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