IMPLEMENTATION OF LOW POWER HALF ADDER IN GDI TECHNOLOGY

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Abstract: ***Adders are used in processors in the arithmetic logic units, to calculate addresses, table indices, and other similar operations. Half Adders are frequently required in VLSI (Very Large Scale Integration) from processors to application specific integrated circuits (ASICs). The speed and power dissipation are the important parameters which should be taken into consideration in digital circuits. In this paper, proposed 1 bit half adder is implemented in 180nm technology at 1.8V using GDI (Gate Diffusion Input) technique which shows better results in comparison to previous half adders. The proposed half adder is also simulated in 130nm and 90nm technology using GDI technology at 1.2V and 0.9V respectively. Power consumption, propagation delay, Power Delay Product and Energy Delay Product are compared and analyzed.***

Index Terms: Very large scale integration, Adders, Power dissipation

I. INTRODUCTION

Adder circuit is a combinational digital circuit that is used for adding two numbers. A half adder is a type of adder, an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value. It has two inputs, called A and B, and two outputs S (sum) and C (carry). The common representation uses a XOR logic gate and an AND logic gate shown in Fig.1. [2] The truth table of half adder is shown in Table I. Besides addition, adder circuits can be used for a lot of other applications in digital electronics like address decoding, table index calculation etc. A fast and energy efficient adder plays a vital role in electronics industry. Adder contributes substantially to the total power consumption of system. With the technology scaling to deep submicron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip [3]. Therefore, in realizing Modern VLSI (Very Large Scale Integration) circuits, low power and high speed are the two predominant factors which need to be considered. Today, there are an increasing number of portable applications requiring small areas low power high throughput circuitry [4]. Since number of integrated transistors becomes double in once in 18 months, there is a much need to fabricate low power VLSI chips. Portable consumer electronic products powered by batteries are another factor for low power VLSI Design, since the battery technology alone cannot solve the low power problem [5]. In order to achieve energy efficient and low power VLSI circuits, a novel low power half adder using GDI (Gate Diffusion Input) technology which is in turn designed with less number of transistors is implemented.[7]

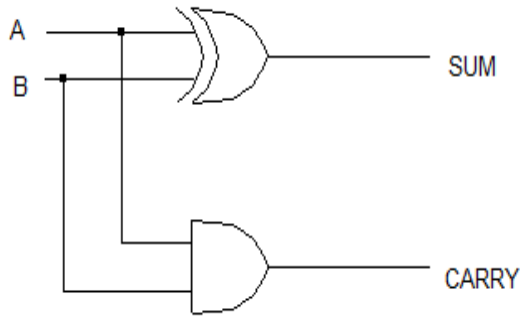

Fig. 1 Half Adder [2]

Table I. Truth Table of Half Adder [2]

Input		Output	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

II. PREVIOUS WORKS

(1.) CMOS Logic

Complementary metal oxide semiconductor (CMOS) is a technology for constructing integrated circuits shown in Fig.2. The outputs of the PMOS and NMOS transistors are complementary such that when the input is low, the output is high, and when the input is high, the output is

low. PDN (Pull down network) network application is used to create low state in output and PUN (Pull up network) network application is used to create high state in output. CMOS design technique has relatively simple fabrication process but in order to drive wires quickly, large width transistors are needed [6]

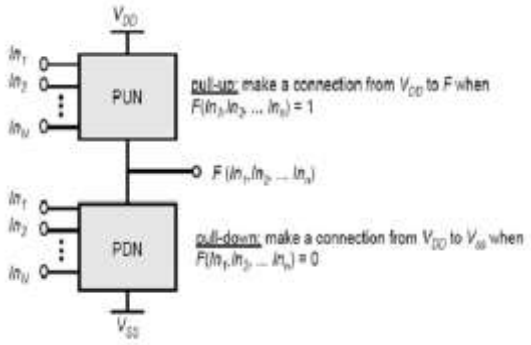

Fig. 2 CMOS Logic [6]

(2.) TG Logic

A transmission gate (TG), or analog switch, is defined as electronic elements that will selectively stop or pass a signal level from the input to the output shown in Fig.3. When the voltage on node A is a Logic 1, the complementary Logic 0 is applied to node Abar, allowing both transistors to conduct and pass the signal at IN to OUT. When the voltage on node A is a Logic 0, the complementary Logic 1 is applied to node Abar, turning both transistors off and forcing a high impedance condition on both the IN and OUT nodes.[6]

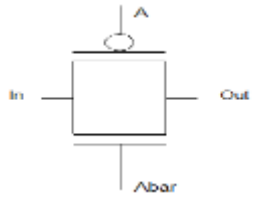

Fig. 3 TG Logic [6]

(3.) GDI technique

The GDI (Gate Diffusion Input) method is based on the use of a simple cell as shown in Fig. 4. GDI cell contains three inputs G (the common gate input of the nMOS and pMOS transistors), P (input to the outer diffusion node of the pMOS transistor) and N (input to the outer diffusion node of the nMOS transistor).The out node (the common diffusion of both transistors) may be used as input or output port, depending on the circuit. The source of the PMOS in a GDI cell is not connected to VDD while the source of the NMOS in a GDI cell is not connected to GND. This feature gives the GDI cell two extra input pins to use which makes the GDI design more flexible in comparison to usual CMOS design. [7] In this paper half adder has been implemented using GDI technology.[8]

Fig. 4 GDI basic cell [7]

Table II. Various functions of GDI basic cell [8]

N	P	G	OUT	FUNCTION
0	B	A	AbarB	F1
B	1	A	Abar + B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	AbarB + AC	MUX
0	1	A	Abar	NOT
Bbar	B	A	AbarB + ABbar	XOR
B	Bbar	A	AB + AbarBbar	XNOR

PREVIOUS HALF HDDERS:

(1) 18T Half Adder

It is shown in Fig.5.The drawback of this adder is that it has higher delay. [1]

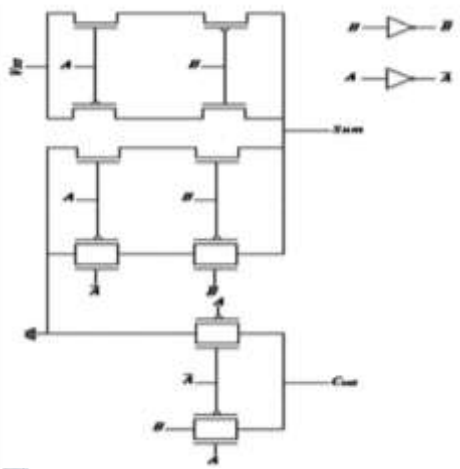

Fig. 5 18T Half Adder [1]

(2) MUH Half Adder

It is shown in Fig.6.The drawback of this adder is that its power dissipation is higher. [1]

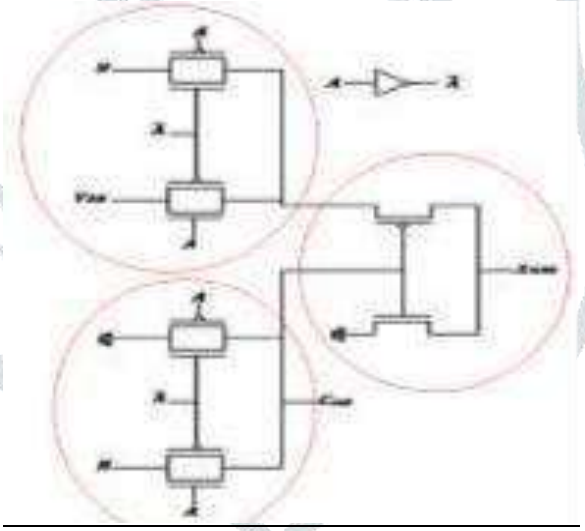

Fig. 6 MUH Half Adder [1]

III. PROPOSED CIRCUIT

A low power half adder is implemented using GDI technology which uses 6 transistors. It has been compared with 18T half adder and MUH half adder presented in paper [1] and shows better results. Proposed half adder has been implemented in 180nm, 130nm and 90nm technologies at 1.8 V, 1.2 V and 0.9 V respectively. Schematics have been prepared using Tanner tool shown in Fig7, Fig.9 and Fig.11. All the simulation results have been carried out using TSPICE program simulator and waveforms are shown in Fig.8, Fig.10 and Fig.12. Comparison of power dissipation, propagation delay, Power Delay Product and Energy Delay Product[9] has been analyzed in Table III and Table IV.

Significant parameters used in this paper:

Power Dissipation: It is the sum of static power, dynamic power and short circuit power dissipated[10] and is calculated by using equation (1).

Ptotal = Pdynamic + Pshort circuit + Pstatic (1)

Propagation Delay: It is an average of amount of output delay for changing the state from low to high and amount of output delay for changing the state from high to low as shown in equation (2).

Delay = (tpLH + tpHL)/2 (2)

Power Delay Product: It is the product of average power consumption and propagation delay as shown in equation (3).

PDP = Pavg * tp (3)

Energy Delay Product: It is the product of PDP and propagation delay as shown in equation (4).
EDP = PDP * tp (4)

Schematic and waveforms of Proposed Half Adders:

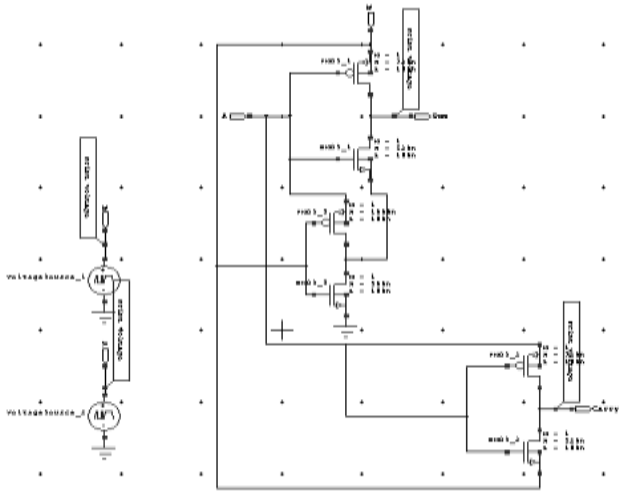

Fig. 7 Schematic of proposed 180nm half adder

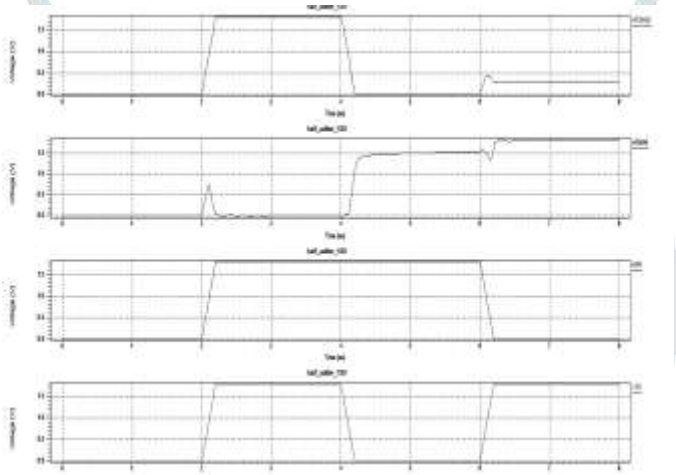

Fig. 8 Output waveform of proposed 180nm half adder at 1.8V

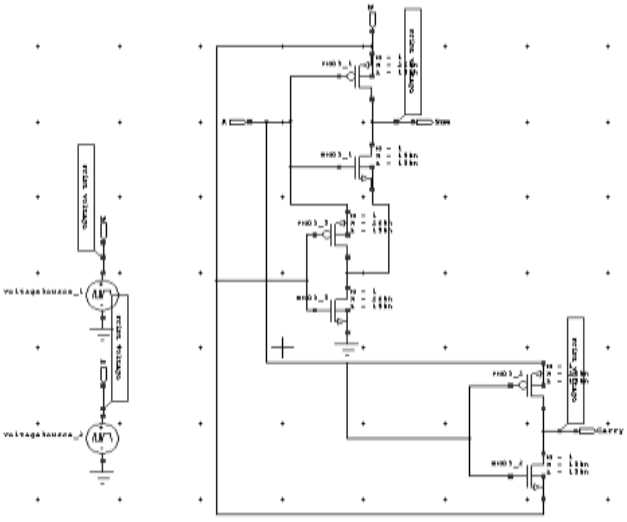

Fig. 9 Schematic of proposed 130nm half adder

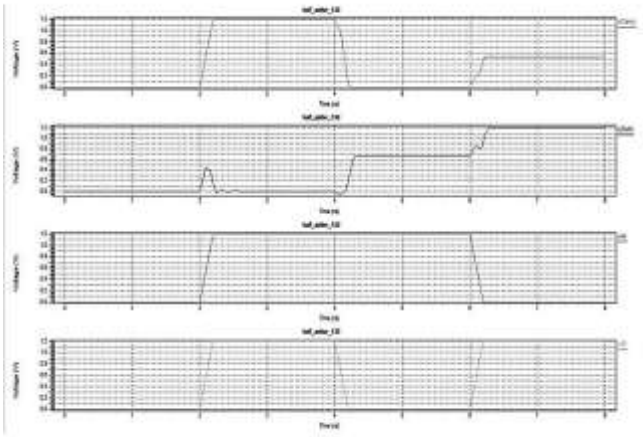

Fig. 10 Output waveform of proposed 130nm half adder at 1.2V

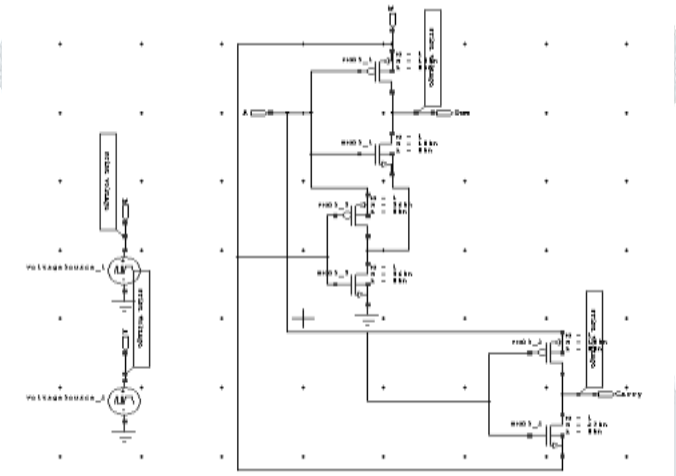

Fig. 11 Schematic of proposed 90nm half adder

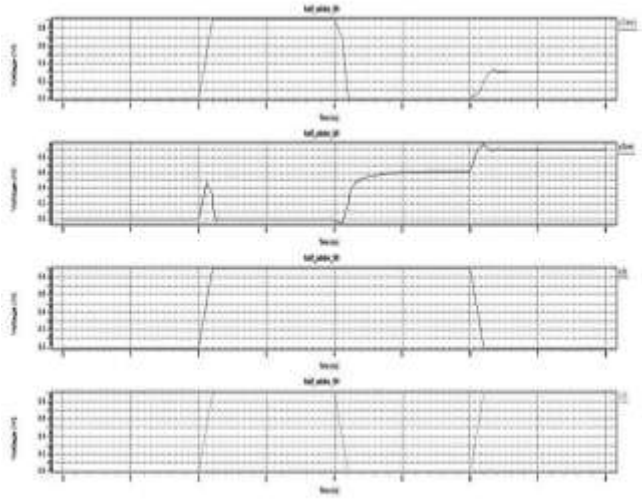

Fig.12 Output waveform of proposed 90nm half adder at 0.9V

IV. SIMULATION RESULTS

Comparison of previous and proposed half adder in 180nm technologies files at 1.8 V is shown in the Table III. Whereas 130 nm half adder is simulated at 1.2V and 90nm half adder is simulated at 0.9 V and simulation results is shown in Table IV.

Table III. Comparison of 18T half adder, MUH half adder and Proposed Half Adder in 180nm technology at 1.8V

Parameters	18T Half Adder (180nm)	MUH Half Adder (180nm)	Proposed Half Adder (180nm)
Power (uW)	4.34	10.4	3.2016
Delay (ps)	136.95	34.9	5.2070
PDP (*10^-17)	59.4	36.2	1.6671
EDP (*10^-27)	81.398	12.6	0.086806

Table IV. Simulation result of proposed half adders in 130 nm and 90 nm technologies at1.2V and 0.9V respectively

Parameters	Proposed Half adder (130nm)	Proposed Half adder (90nm)
Power (uW)	2.5322	0.52305
Delay (ps)	18.120	23.142
PDP (*10^-17)	4.5882	1.2104
EDP (*10^-27)	0.83136	0.28012

V. CONCLUSION

In this paper half adders are proposed in different foundries. 180nm half adder has lowest power consumption, propagation delay, power delay product and energy delay product in comparison to previous 18T half adder and MUH half adder. Proposed half adders have been implemented using six transistors which makes them area efficient. On comparing 180nm, 130nm and 90nm proposed half adders we conclude 180nm half adder has lowest delay whereas 90nm has lowest power consumption. Depending on the focus of designer different designs can be used.

VI. ACKNOWLEDGMENT

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VII. REFERENCES

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