A REVIEW ON COMMON MODE VOLTAGE REDUCTION TECHNIQUES

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Abstract: ***Inverters have vast applications in the industries, but the issue of common mode voltage have been aroused and caused serious side effects. There are numerous control strategies and hardware solutions for reducing the common mode voltage. Common mode voltage reduction through control techniques have gained importance because of their cost effective solution when compared to hardware techniques. Near state, active zero state, remote state are space vector based PWM techniques and carrier peak positioning, carrier phase shift techniques are carrier based strategies for reduction of common mode voltage (CMV). A review on CMV reduction PWM techniques and also on some hardware topologies was done.***

Index Terms – Common Mode Voltage, RCMV control strategies, Space vector based PWM, Carrier based PWM.

I. INTRODUCTION

The efficiency and wide range control of motor drives is possible with the voltage source inverters. Inverter switches are operated with pulse width modulation to obtain required output voltage. Inverter output voltage characteristics are improved by increasing the frequency. In process of reducing harmonics of output voltage and enhancing the dynamic characteristics breakdown of motor insulation, shaft voltage, Electromagnetic Interference (EMI), bearing currents are caused. The number of working hours of motor and the entire system decreases [12, 13].

As there is raise in the switching frequency it provokes problem of CMV that reduces reliability and security of entire system by achieving EMC standards. CMV can be mitigated in two ways either by control techniques or with hardware. Additional power devices, passive and active filters, common mode choke and topologies like four phase inverters [6-9] are some techniques in hardware for CMV mitigation. Difficulty in design of system parameter and control, cost, size rises as they necessitate extra components that is capable of CMV suppression. In control techniques adjustment of inverter modulating algorithm or control signals are capable of mitigating the CMV.

Changes were made in carrier based modulation, space vector modulation and selected harmonic modulation are considered as reduced CMV PWM (RCMV PWM) [2-5]. Among different control techniques space vector based strategy have gained good attention. For different level inverters we can apply these RCMV control strategies. If the available source is three phase supply, a typical adjustable speed drive system consists of a front end diode rectifier, voltage source inverter and induction motor. In these type of systems the voltage between the star point and ground is known as common mode voltage (CMV) [4]. Therefore the voltage$v_{ng} = v_{nm} + v_{mg}$. But the voltage v_{nm} is very much lesser than v_{mg}

$$V_{CMV} = \frac{v_{am}+v_{bm}+v_{cm}}{3} \quad (1)$$

The CMV is not zero in the traditional inverters because the output voltage is not exact sinusoidal voltage. With change in voltage vectors the CMV value also changes. The value of the CMV varies in between $\pm\frac{V_{DC}}{6}$ and $\pm\frac{V_{DC}}{2}$ based on the voltage vector. In RCMV control strategies zero voltage vector is eliminated because it causes maximum CMV value.

In the section-2 a brief RCMV control strategies based on space vector modulation and carrier based modulation are presented. In last section-3 the entire paper is concluded.

II. CONTROL STRATEGIES FOR REDUCTION OF COMMON MODE VOLTAGE

2.1 Space Vector Based Common Mode Voltage reduction Technique:

2.1(a) Space vector Pulse Width Modulation:

The concept of the SVPWM relies on representation of inverter output as space vectors or space phasors. Space vector representation is valid for both transient and steady state conditions in contrast to phasor representation which is valid only for steady state conditions. The concept of space vector arises from rotating air-gap MMF in a three-phase induction machine. Hexagon consists of six distinct sectors spanning over 360 degrees with each sector of 60 degrees. Space vectors are stationary while reference vector V_s^* is rotating at a speed equal to fundamental frequency of inverter output voltage. It circles once for one cycle of the fundamental frequency. In implementing SVPWM, reference voltage is synthesized by using nearest two neighboring active vectors and zero vectors. The choice of active vectors depends upon sector number in which reference is located. Hence, it is important to locate the position of reference voltage. Once reference vector is located, vectors to be used for SVPWM implementation has to be identified. The output voltage frequency of inverter is same as speed of reference voltage and output voltage magnitude is same as magnitude of reference voltage. Calculate dwell times of vector. Time of application of different space vectors are calculated using 'equal volt-second principle'. According to this principle, product of reference voltage and sampling/switching time (T_s) must be equal to product of applied voltage vectors and their time of applications, assuming that reference voltage remains fixed during the switching interval [14].

Below equation is a volt second balance equation

$$v_s^* T_s = V_1 t_a + V_2 t_b + V_0 t_0$$
$$T_s = t_a + t_b + t_0 \quad (2)$$

By applying zero state vector followed by two adjacent active state vectors in a half switching period. In next half of switching period is mirror image of first half.

2.1(b) Active Zero State Pulse width modulation:

AZSPWM involves utilizing the two adjacent voltage vectors along with two opposing active voltage vectors with equal duty cycle to provide cancellation and create an effective zero state. For example, as shown in Fig. 1 in A1, the adjacent state voltage vectors V_4 and V_6 are accompanied by the active zero pairs of V_2 and V_5 . Thus in A1, the optimal sequence is$(V_2 - V_6 - V_4 - V_5 - V_4 - V_6 - V_2)$. The CMV is reduced to $\pm\frac{V_{DC}}{6}$ since the zero states are avoided. The method is linear in the whole inverter hexagon, unlike NSPWM. Scalar PWM implementation of the method is straightforward as the modulation wave of SVPWM and the alternating polarity carrier wave are used to generate the pulse pattern of the method. Similar to NSPWM, this method also has two bipolar line-to-line voltage pulses. While in NSPWM, only one line-to-line voltage has bipolar pulses. The primary performance limitation of AZSPWM1 involves its two bipolar line-to-line voltage pulses. Regardless the M_i range, the zero-voltage time interval between the bipolar pulses periodically decreases within a fundamental cycle. Depending on the adjacent voltage vectors used the AZSPWM is classified as AZSPWM1, AZSPWM2, AZSPWM3.If the adjacent voltage vector and its opposite vector is utilized then it is AZSPWM3 or if the adjacent active state is utilized then it is known as AZSPWM1/AZSPWM2. The Fig.1 is AZSPWM1

Duty Cycle calculation:

$$d_{j+1} = \frac{2\sqrt{3}}{\pi} M_i \sin\left(\theta - \frac{(j-1)\pi}{3}\right) \quad (3)$$

$$d_j = \frac{2\sqrt{3}}{\pi} M_i \sin\left(\frac{j\pi}{3} - \theta\right) \quad (4)$$

$$d_{j-1} = d_{j+2} = \left(1 - d_{j+1} - d_j\right)/2 \quad (5)$$

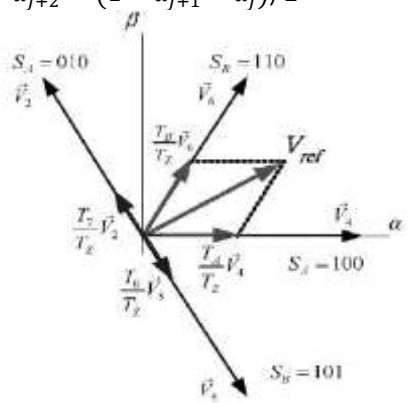

Fig.1 Reference vector generation for AZSPWM3 [10]

2.1(c) Remote State Pulse width modulation:

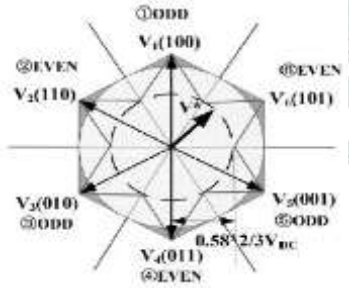

Fig.2 RSPWM [11]

As shown in Fig.2 RSPWM is a space vector based CMV reduction technique either odd or even states are utilized for generation of the reference vector. Reduction of harmonic distortion and increasing peak value of reference voltage can be done by modifying the space vector algorithm. The sectors are rotated 30^o with respect to standard space vector sectors. This increases maximum value of reference voltage to $0.5*\left(\frac{2V_{dc}}{3}\right)$.

2.1(d) Near State Pulse width modulation:

The conventional SVPWM method utilizes the two adjacent voltage vectors (to the reference voltage vector) and the two zero-voltage vectors to program the PWM pulses. The NSPWM method utilizes a group of three-voltage vectors to match the output and reference volt-seconds. These three voltage vectors are selected such that the inverter voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized (as shown in Fig.3). Thus, in addition to the adjacent voltage vectors, a near-neighbor voltage vector is utilized. Hence, it is named "near state." Note that the zero states are not utilized in NSPWM.The utilized voltage vectors are changed every 60◦ throughout the space For example, for the region between 30◦ and 90◦ (B2), the applied voltage vectors of NSPWM are V1, V2, and V3 [4]. Utilizing the near-state voltage vectors defined above, the complex variable volt-seconds balance equation and the PWM period equation for NSPWM can be written in a generalized form for region Bi in the following equation, where T_s is the PWM period:

Volt-Second balance equation:

$$V_{i-1}t_{i-1} + V_i t_i + V_{i+1}t_{i+1} = V_{ref}T_s \quad (6)$$

Sampling Time (T_s):

$$t_{i-1} + t_i + t_{i+1} = T_s \quad (7)$$

Duty Cycle calculation:

$$d_{j-1} = 1 - \frac{2\sqrt{3}}{\pi} M_j \sin\left(\theta - \frac{(j-2)\pi}{3}\right) \quad (8)$$

$$d_j = -1 + \frac{3}{\pi} M_j \cos\left(\theta - \frac{(j-2)\pi}{3}\right) + \frac{3\sqrt{3}}{\pi} M_j \sin\left(\theta - \frac{(j-2)\pi}{3}\right) \quad (9)$$

$$d_{j+1} = 1 - \frac{3}{\pi} M_j \cos - \left(\theta - \frac{(j-2)\pi}{3}\right) - \frac{\sqrt{3}}{\pi} M_j \sin\left(\theta - \frac{(j-2)\pi}{3}\right) \quad (10)$$

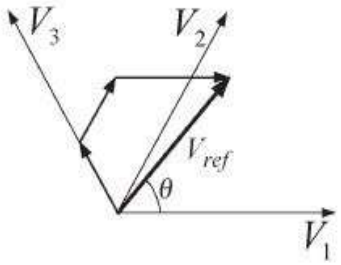

Fig.3 NSPWM reference vector in sector B_2 [4]

2.1(e) High performance PWM:

High performance PWM is a combination of AZSPWM1 and NSPWM. Advantage of this technique is that NSPWM is best method in high modulation range and AZSPWM is better for lower modulation range. So the advantages of these methods are combined [2]. In Fig.4 the flow chart of high performance PWM is shown.

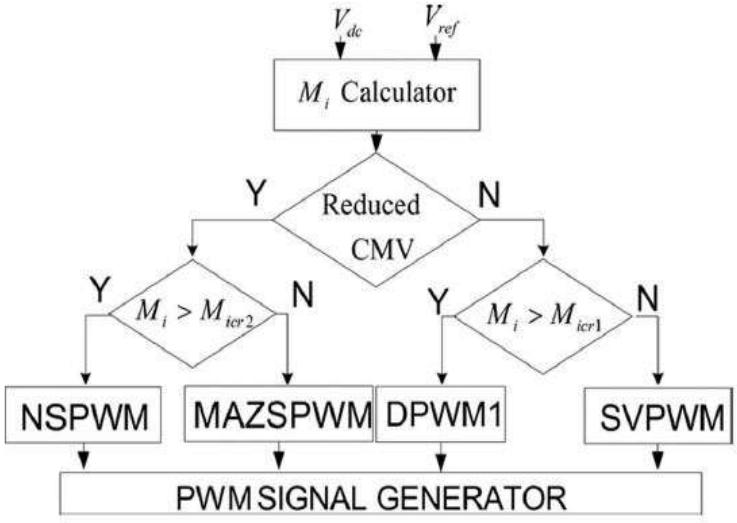

Fig. 4 Flow chart of HP PWM [2]

2.2 Carrier Based Pulse Width Modulation strategies:

2.2(a) Carrier Phase Shift Modulation:

The frequency of the three phase carrier waves is same and they are phase displaced from each other by $\frac{T_c}{3}$. In this probability of zero state occurrence is decreased.

Let us consider the modulating wave of phase A, phase B and phase C are: $V_{Aref} = M_a sin\varphi$, $V_{Bref} = M_a \sin(\varphi - \frac{2\pi}{3})$, $V_{Cref} = M_a \sin(\varphi - \frac{4\pi}{3})$ where $\varphi = 2\pi f t$ here f_o is the fundamental frequency. As the carrier frequency is much greater than the modulating wave frequency, so the modulating sinusoid is assumed to be constant. This method is applicable up to modulation index of $\frac{2}{3}$.

For modulation index greater than $\frac{2}{3}$ the peak CMV will be between $\pm\frac{V_{DC}}{2}$

$$|V_r| > V_t = \frac{1}{3} + \sqrt{\frac{3}{4}M_i^2 - \frac{1}{3}} \quad (11)$$

Where V_r is reference voltage and V_t is the threshold voltage

$$|\Delta t_z| = \frac{T_c}{6} - \frac{T_c}{8}|V_r| - \frac{\sqrt{3}}{8} T_c \sqrt{M_i^2 - V_r^2} \quad (12)$$

2.2(b) Carrier Peak Position Modulation (CPPM):

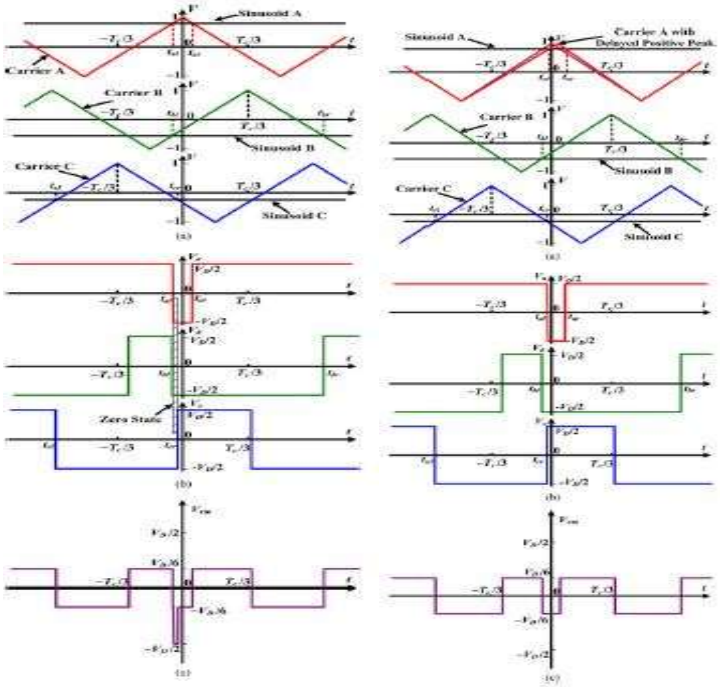

Fig.5 shows the difference between the CPS PWM and CPPM technique [5]

By changing the peak position of triangular carrier the zero states in the sinusoidal pulse width modulation is restricted and peak value of CMV is decreased for any modulation index. Where t_{ar}, t_{br}, t_{cr} are the rising edges of the pulses in SPWM t_{af}, t_{bf}, t_{cf} are the falling edges of pulses in S.P.W.M. When the carrier peak of phase A is delayed (as shown in Fig.5) i.e., $t_{ar} > t_{cf}$ it will eliminate the zero voltage vector. The other way to eliminate the zero state is by advancing the peak position of the carrier such as$t_{af} < t_{br}$. In this cases delaying of the carrier peak is preferred because delaying time is smaller than advancing time. If $V_{Cref} \geq V_{Bref}$ then delaying the position of Phase-A negative pulse has least change whereas if $V_{Cref} < V_{Bref}$ then advancing the position of phase-A negative pulse has least change. The time for which the zero state can be maximum restricted is Δt_{zmax}that can be either advanced or delayed. The Zero state can also be avoided by advancing or delaying the carrier for a period of $2\Delta t_{zmax}$. The frequency of the carrier and the pulse width are kept constant [5].

$$V = {4t}/{T_c} + 1$$
$$V = {2(2t + T_c)}/{(2\Delta t_p + T_c)} - 1 \quad (13)$$

Where

$$V = |V_{ref}|, t_{ar} = \frac{(|V_{ref}| - 1)T_c}{4}$$
$$t_{ar1} = \frac{(|V_{ref}|+1)(2\Delta t_p + T_c)}{4} - \frac{T_c}{2} \quad (14)$$
$$\Delta t_2 = t_{ar1} - t_{ar}, \qquad \Delta t_p = \frac{2\Delta t_p}{(1 + |V_{ref}|)}$$

Considering the effect of dead time leg's output current and voltage are related to each other, load impedance and output current are also related to each other. The switching time gets delayed when the dead time effect is considered.

$$|V_{ref}| > V_t = \frac{1}{3} + \frac{2t_d}{T_c} + \sqrt{\frac{3}{4}M_i^2 - 3\left(\frac{1}{3} + \frac{2t_d}{T_c}\right)^2} \quad (15)$$

And

$$|\Delta t_z| = \frac{T_c}{6} - \frac{T_c}{8}|V_{ref}| - \frac{\sqrt{3}}{8}T_c\sqrt{M_i^2 - V_r^2} + t_d \quad (16)$$

Whereas V_{ref} is the reference voltage

Δt_z is change in zero time

Δt_p is change in peak time

2.3 Topologies for CMV reduction:

2.3(a) Balanced Inverter:

Each phase leg of balanced inverter have three series switches. The top and bottom switches are chosen in such a way that device voltage capability is half of the DC bus voltage and they are also switched simultaneously. On every phase leg the middle switch of balanced inverter is operated in a complimentary fashion. There are only two switching possibilities in each phase leg. The middle switch is turned OFF, top and bottom switches are turned ON so the output terminals connected to positive and negative terminal of DC bus voltage. The middle switch is turned ON, top and bottom switches are turned OFF then the output terminals.

$$v_{xg} + v_{xg} = 0, x = a, b, c \quad (17)$$

$$v_{cm0} = \frac{v_{ag}+v_{bg}+v_{cg}+v_{a'g}+v_{b'g}+v_{c'g}}{6} = 0 \quad (18)$$

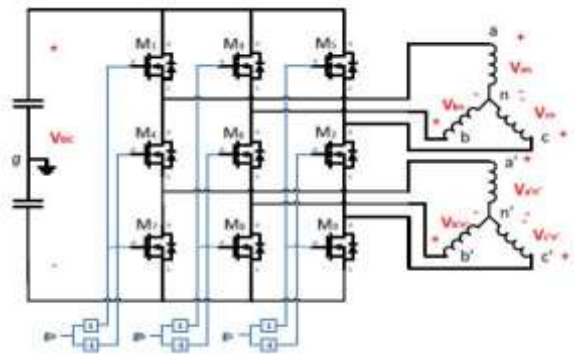

Fig.6 shows the balanced inverter topology for CMV reduction [6]

2.3(b) Eight switch inverter:

Instead of the control strategies a new eight switch topology is proposed. In this topology the occurrence of zero state is used to overcome the issue of common mode voltage. Peak value of common mode voltage occurs during zero states. Zero state voltage occurs in traditional inverters when the three phase output are connected to the same DC voltage terminal. Extra switches (S_x, S_y) are added in series to DC source and they are turned OFF when zero states occur which disconnects the DC source. But the input terminals of inverter are disconnected and ground potential is created due to machine parasitic capacitance. Since the inverter input terminals are disconnected, their might be a chance for appearance of varying voltage instead of 0V. So to maintain almost constant CMV and zero states uncertainty anti parallel Zener diodes are placed across the extra switches.

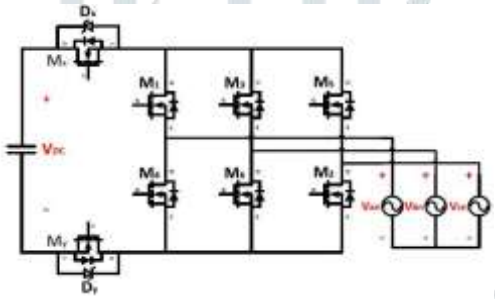

Fig.7 shows schematic diagram of eight switch inverter [7]

2.3(c) Four Phase converter:

Inverter shown in Fig.8 has even number of legs to reduce output voltage to zero. Below in eq (19) condition should be satisfied to reduce common mode voltage.

$$V_1 + V_2 + V_3 + V_4 = 0 \quad (19)$$

The extra phase leg introduced in inverter that reduces effect of CMV by modifying the control strategy.

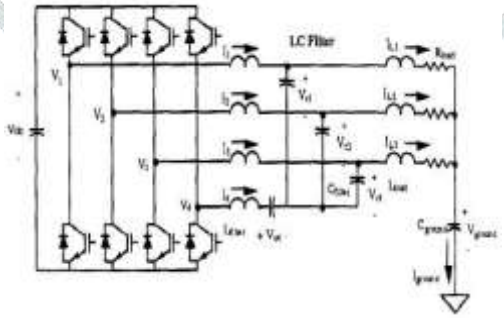

Fig.8 Shows the CMV reduction with four phase inverter [8]

Table 1 Comparing traditional PWM with RCMV control strategies [3]

	Linearity modulation range	Switching times per T_s	Simultaneous switching	DC voltage utilization ratio	CMV fluctuations	Maximum value of CMV
SVPWM	0-0.91	6	N	1	6	$\pm\frac{V_{DC}}{2}$
RSPWM	0-0.60	8	Y	0.67	0	$\pm\frac{V_{DC}}{6}$
NSPWM	0.61-0.91	4	N	1	4	$\pm\frac{V_{DC}}{6}$

AZSPWM1	0-0.91	6	N	1	6	$\pm\frac{V_{DC}}{6}$
AZSPWM3	0-0.91	6	Y	1	2	$\pm\frac{V_{DC}}{6}$
SPWM	0-0.785	6	N	0.866	6	$\pm\frac{V_{DC}}{2}$
CPPM	0-0.785	6	N	0.866	6	$\pm\frac{V_{DC}}{6}$
CPS PWM	0-0.785	6	N	0.866	6	$\pm\frac{V_{DC}}{2}$ *or* $\pm\frac{V_{DC}}{6}$

III. Conclusion:

Different RCMV control strategies which are carrier and space vector based techniques for two-level voltage source inverter are discussed. Some topologies that reduce CMV are also discussed. In topologies eight switch inverter is the best topology because in balanced inverter topology the winding configuration of motor has to be changed so it is disadvantageous. This paper mainly focused on techniques that avoid zero state like AZSPWM, NSPWM, RSPWM, and CPPM. In comparison with performance of different PWM techniques among them is high performance PWM (HPPWM) better method because of its high linearity modulation range, low THD, less CMV fluctuations. CMV has good scope of research as the power devices switching frequency is increasing.

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