Implementation of 4-Bit Carry Skip Adder Using Reversible Logic with Transistor 180-nm Technology

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Abstract: ***The high speed computation and complex computing application requirements are growing phenomenally in current compute intensive world. Due to growing demands power consumption, chip size issues and heat dissipation are the most challenging for logic design with existing technologies. So the designs of low power and high speed logic circuits are creating tremendous interest in current scenario. Reversible computing is developing as an elective that offers high calculation speed, high bundling thickness, low heat dissipation and low power utilization and so on.Utilizing the reversible logic gates using MOSFETs, a 4-bit carry skip adder has been intended for 1.8V task utilizing TSG gate and fredkin gate. The carry skip adder performs four arithmetic and four logical tasks. MOSFET transistors have been promising in acknowledging expanded usefulness on a chip. The sources of input signals, computes the weighted whole of all information signals and after that controls the ON and OFF conditions of the transistor.The results are observed from the Cadence Virtuso ADE.***

Keywords: MOSFET, TSG, Reversible gates,Adders.

I.INTRODUCTION

The current paper contains a carry skip adder structure which has higher speed and lower energy utilization using reversible logic gates by transistor 180nms technology.

In this we are implementing TSG gates and the Fredkin(F) gate by using 4-bit carry skip adder instead of having of using the full adder in order to overcome the disadvantages.A 4 * 4 one through reversible gate called TS gate "TSG" is proposed. It can be checked from the Truth Table based the input and output corresponding Boolean function can be implemented from the universal gate called NOR gate.Thus, the proposed gate can be utilized to actualize any Boolean function. The reversible TSG requires five reversible Fredkin gate and produces five garbage yields.The three FGs amidst are utilized to play out the AND operation. The block propagate signal P will be generated. The single FG in the left half of plays out the AND-OR operation to make the carry skip adder skip and produce the carry out signal Count. In the proposed carry Skip adder,the FG propagates the block's carry input to the following block if the block value. Then it undergoes mutation section where checking for errors and replaces or changes with new value. After going hamming scan module then finally fitness function is calculated. From there we get best sequence .we take best value for this signal P is one; when p=0, AND-OR it skips the logic and doesnot perform the operation efficiently.AND gate will require N-1 FGs of N inputs.2N total gates are required for proposed N bit carry save adder.In this paper is discussed as follows: II. Proposed 4* 4 Reversible Gate with full adder and its components are discussed in section II, Gray scale image in section III, Results and Discussion in section IV and Conclusion in section V.

II.PROPOSED 4* 4 REVERSIBLE GATE

In this paper, a 4 * 4 one through reversible gate called TS gate "TSG" is proposed. The proposed reversible TSG gate is shown in Fig. 1. The corresponding truth table of the gate is shown in Table I. It can be verified from the Truth Table that the input pattern corresponding to a particular output pattern can be uniquely determined. The proposed TSG gate can implement all Boolean functions.

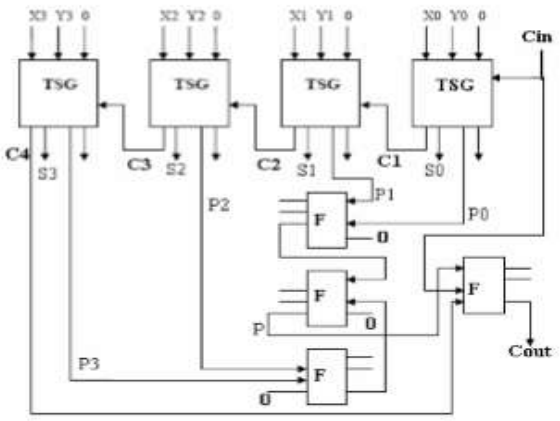


Fig.1.Skip Adder Block Using Proposed TSG and Fredkin (F) gates

The Individual Components of TSG are shown in fig.1.They are (i)TSG Gate,(ii)Fredkin Gate,(iii) Carry Skip Adder.The TSG Gate was shown in fig.2.

The conventional skip block in Fig. 1. uses the AND-OR gate combination. Fig. 9 shows the block diagram of the carry skip adder block constructed with TSG gates and Fredkin gates (FG). The three FGs in the middle of Fig. 1 are used to perform the AND4 operation. This will generate the block propagate signal P. The single FG in the left side of Fig.1the AND-OR function to create the carry skip logic and generate the block carry out signal Cout. In the proposed carry Skip adder, the FG propagates the block's carry input to the next block if the block propagate signal P is one; otherwise, the most significant full adder carry C4 is propagated to the next block. The traditional carry skip AND-OR logic in Fig.1.and the carry skip logic fig 4, do not have the equivalent truth Tables but it must be noted that the Fredkin carry skip logic more faithfully adheres to the spirit of carry skip addition by propagating the correct value of Cin to Cout. The FG carry skip logic can lead to improve carry propagation, when the block carry propagate signal P is one. When P is one, the block carry input Cin must propagate to the next block, independent of the result of the carry C4 created by the full adders within the block. When P=0, the traditional AND-OR carry skip logic in Fig.1 must account for sending C4 , it does not perform its carry skip operation efficiently. The Fredkin carry skip logic in Fig1 passes Cin to Cout whenever

P=1, regardless of C4. The savings in time can be quite significant as block sizes increases. The proposed N bit carry skip adder requires N TSG gates for implementation of ripple carry adder. Further, the N input AND gate will require N-1 FGs. Thus the total gates required in proposed N bit carry save adder is 2N.

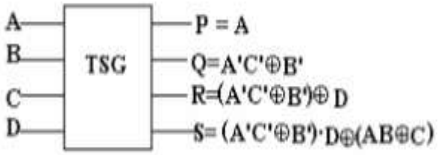


Fig.2 TSG Gate

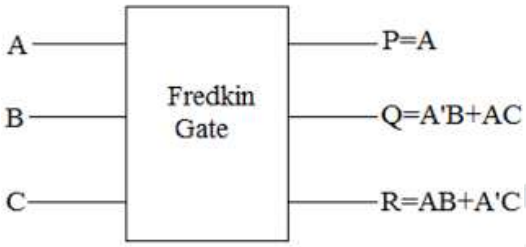


Fig.3.Fredkin Gate

TABLE I. TRUTH TABLE OF THE PROPOSED TSG GATE

A	B	C	D		P	Q	R	S
0	0	0	0		0	0	0	0
0	0	0	1		0	0	1	0
0	0	1	0		0	1	1	1
0	0	1	1		0	1	0	0
0	1	0	0		0	1	1	0
0	1	0	1		0	1	0	1
0	1	1	0		0	0	0	1
0	1	1	1		0	0	1	1
1	0	0	0		1	1	1	0
1	0	0	1		1	1	0	1
1	0	1	0		1	1	1	1
1	0	1	1		1	1	0	0
1	1	0	0		1	0	0	1
1	1	0	1		1	0	1	1
1	1	1	0		1	0	0	0
1	1	1	1		1	0	1	0

III. APPLICATIONS OF THE PROPOSED TSG GATE

To illustrate the application of the proposed TSG gate, two different types of adders – ripple carry and carry skip adders are designed. It has been proved that the adders circuit drawn using the proposed gate are the most optimized one compared to their existing counterparts in literature.

Carry Skip Adder :

In the carry skip adder, delay is reduced due to the carry computation. In the full adder operation, if either input is a logical one, the cell will propagate the carry input to its carry output. Hence, the ith full adder carry input Ci, will propagate to its carry output, Ci+1, when Pi= Xi Yi. In addition, the multiple full adders, making a block can generate a "block" propagate signal P to detour the incoming carry around to the block's carry output signal. Fig. 4 shows a four bit carry skip adder block. It is quickly determined by each block, that whether the block's carry input is propagated to its carry output. If the block propagate P is one, the block carry input Cin is propagated as the block carry output Cout. An AND gate is used to generate a block propagate signal P. Fig. 8 shows the proposed carry skip compatible Full adder constructed with TSG gate.

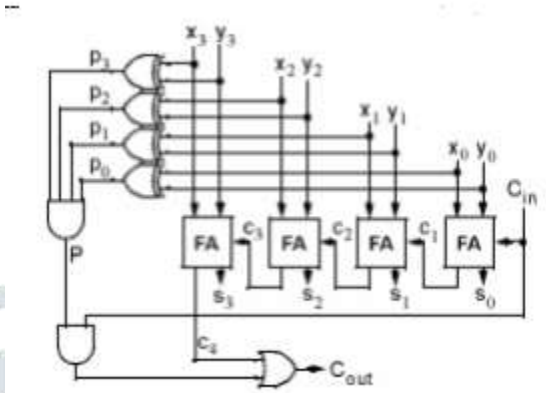


Fig .4.Four Bit Carry Skip Adder Block

IV Results and Discussion:

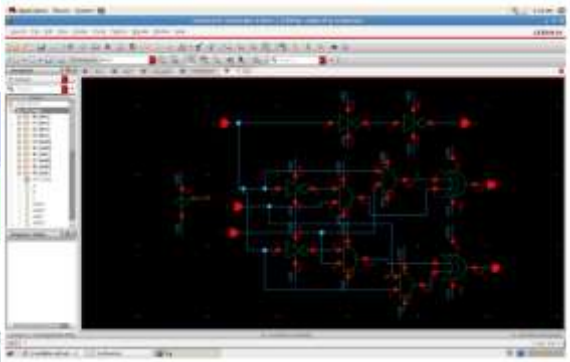


Fig.5.Simulation result of fredkin gate

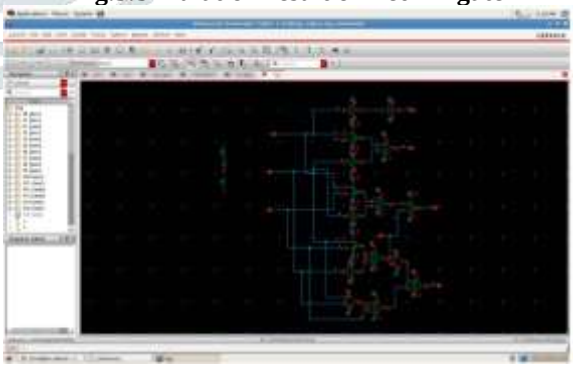


Fig.6.Simulation results of TSG

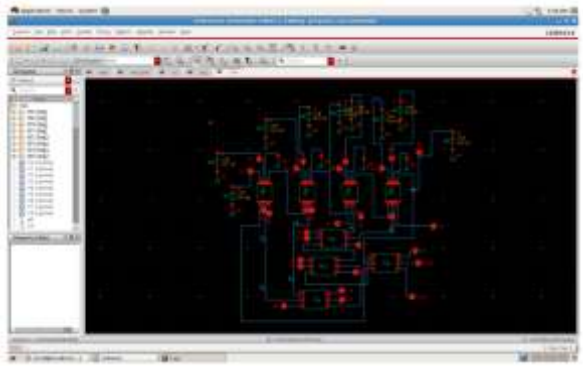
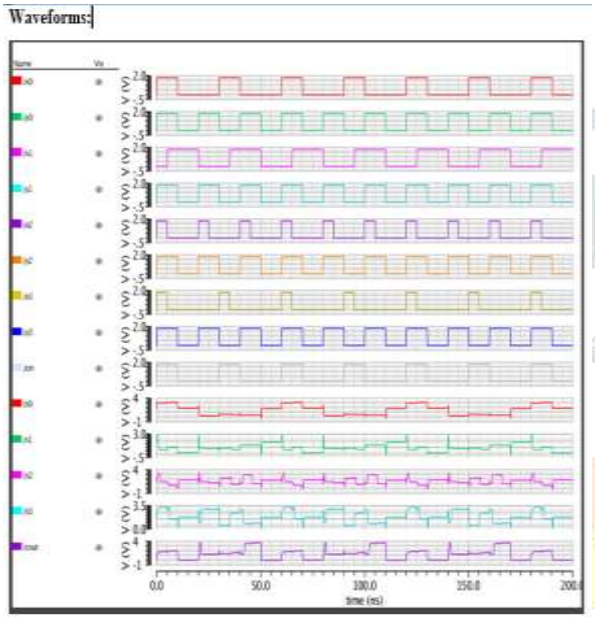


Fig.7.Carry Skip Adder using TSG gate and Fredkin gate.

WaveForms:



The focus of this paper is the proposal of new reversible 4*4 TSG gate. The proposed TSG gate is being used to design optimized architectures of ripple carry and carry skip adders. It is proved that the adder architectures using the proposed TSG gate are better than the existing counterparts in literature, in terms of number of reversible gates and garbage outputs. All the proposed architectures are analyzed in terms technology independent implementations. The technology independent analysis is necessary since quantum or optical logic implementations are not available. There are a number of significant applications of reversible logics such as low power CMOS, quantum computing, nanotechnology, and optical computing and the proposed TSG gate and efficient adder architectures are one of the contributions to reversible logic. The proposed circuit can be used to design large reversible systems. In a nutshell, the advent of reversible logic will significantly contribute in reducing the power consumption. Thus, the paper provides the initial threshold to build more complex systems which can which can execute more complicated operations.

IV CONCLUSION

The paper covers the adder architecture using proposed TSG gate are better existing counterparts in literature in terms of number of reversible gates and garbage outputs.All the proposed architecture are analysed in terms of technology independent implementations.The proposed circuit can be design large reversible circuits.Thereversivle circuits designed and proposed here form the basis of the ALU of a primitive quatam CPU.

This paper implementation is useful for designing a large number of complexity to simplicity form using reversible gates.

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