Leakage Current Minimization by Improved H6 Topology for grid-tied PV system

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Abstract : **The fundamental protest of this paper is to limit the leakage currents of grid tied PV system by the improved H6 topology. These leakage currents are diminished by the lessening of high recurrence voltage transients in the terminal and normal mode voltages. By utilizing PWM method, the high recurrence voltage transients can be decreased. An incremental conductance technique is utilized to track the most extreme power point from P-V graph of PV system. Correlation of existing CMLI and enhanced H6 topology is clarified in this paper. The conduction and switching losses are lessened, so THD of the system is decreased in this topology. This topology is developed in MATLAB/SIMULINK software.**

IndexTerms - **leakage current, high recurrence transients, cascaded multi-level inverter, common mode voltage**

1. Introduction

The fast increment in the interest for power and the current change in the ecological conditions, for example, a dangerous atmospheric deviation prompted a requirement for another source of power that is less expensive and feasible with less carbon outflows. Solar power has offered promising outcomes in the mission of finding the arrangement to the issue. The solar power is specifically changed over into electrical power by solar cells. The outcome of PV array is encouraged for boosting up PV output voltage by the boost converter. Here a MPPT method is utilized to track the MPP of P-V bend of PV framework. The outcome of PV is changed over from DC to AC by the multi-level inverters (MLI) and afterward which is provided to control network (grid) [1-5]. There are three kinds of MLIs which are diode clamped, flying capacitor clamped and cascaded multi-level inverters. The diode and flying capacitor clamped MLIs has a drawback; the most extreme outcome voltage in output is half of the input voltage.

Multi-Level Inverter (MLI) topologies are picking up significance because of their favorable circumstances, for example, high proficiency, low switch tally, low weight and diminished size. In writing overview, numerous topologies of MLIs [6-7] are proposed for the minimization of spillage current for their application in the transformer less PV frameworks (PV system). These topologies for the most part utilized two strategies for minimization of leakage current [8]. One technique depends on keeping up the common mode voltage (CMV) steady, while the other strategy depends on the minimization of the high-recurrence advances in the terminal and normal mode voltages.

One efficient method by Y. Tang *et al.* [2] has proposed a topology for a grid-tied PV framework. The transformer less inverter topology, which is prepared to do at the same time unraveling leakage current and fluctuating power issues in grid-tied photovoltaic (PV) frameworks. Without adding any extra parts to the framework, the leakage current caused by the PV-to-ground parasitic capacitance can be avoided by presenting a common mode (CM) directing way to the inverter. By appropriately infusing CM voltages to the yield channel capacitors, the fluctuating power force can be decoupled from the dc-connect. High Conduction losses and large space requirement are disadvantages of this paper. T. K. S. Freddy *et al.* [18] have proposed a topology for minimization of leakage current. As of late, lessened common mode voltage pulse width regulation (LCMV-PWM) techniques have been proposed to diminish the leakage current in three-stage transformer less photovoltaic (PV) frameworks. Be that as it may, the vast majority of these examination works just spotlight on leakage current end and ignore the general execution of the PV frameworks on issues, for example, cost, voltage linearity, dc-interface current swells and THD. In this paper, a three-stage transformer less inverter, adjusted from the single-stage H5 topology is researched.

H. F. Xiao *et al.* [11] have proposed another productive three-level MLI for the minimisation of leakage current by keeping up CMV at stable. The given topology has low conduction and exchanging misfortunes (switching losses). In any case, this setup experiences the drawback of a high number of gadget checks. M. Islam *et al.* [10] have proposed another intriguing transformer less PV MLI topology to diminish the leakage current by keeping up CMV consistent. This MLI topology utilizes six switches for the age of three levels in the inverter yield voltage. This topology can infuse receptive power into utility matrix with low symphonies contortion. This circuit design brings about high exchanging and conduction misfortunes. Besides, this MLI topology can't be stretched out to in excess of three levels in the yield voltage. L. Zhang *et al.* [9] have proposed a topology by keeping up a steady normal mode voltage (CMV). In this paper, two fundamental exchanging cells, the P-NPCC, and the N-NPCC have been proposed for the matrix attached inverter topology age to fabricate NPC topologies. The given MLI arrangement has a confused activity amid every half-cycle of the key segment of the matrix voltage. The given MLI design comprises of eight switches for the age of three levels in the yield voltage. This topology lessens the exchanging misfortunes however has the downside of high conduction misfortunes amid both turn-ON and zero voltage states. The innate asymmetry in every half-cycle causes a DC counterbalance in the MLI yield voltage. Moreover, the necessity of an extra number of switches for more than three-level activity restrains its application.

Another effective method by G. Buticchi *et al.* [13] have acquainted another vital technique with limit the leakage current by the disposal of high-recurrence voltage advances in the CMV. The creators have proposed a nine-level lattice (grid) tied PV MLI topology. This MLI topology comprises of eleven switches and four diodes. In this MLI, four switches in the low voltage connect are worked with high exchanging recurrence (switching frequency), while the rest of the switches in the high voltage connect are worked with the low exchanging recurrence. For an appropriate task of this setup, the adjust of flying capacitor voltage V_{fc} is vital. Besides, the PV terminals in this MLI topology can't be grounded.

2. Conventional Cascaded multi-level inverter:

The schematic circuit outline of the conventional five-level CMLI for PV framework is appeared in Fig. 1. This design comprises of two converters (Conv-1 and Conv-2). Conv-1 is a half-bridge inverter involving two switches S_{x1} and S_{x2}. The Conv-2 involves an exceptionally proficient and solid inverter design [15] with six changes (S_{x3} to S_{x8}). Among the six switches, four changes (S_{x3} to S_{x6}) in Conv-2 constitute a H-connect circuit. The staying two switches S_{x7} and S_{x8} in Conv-2 are bi-directional switches. The voltage levels of V_{PV} and $V_{PV}/2$ are generated by using the switches of Conv-1.The voltage V_{PV} is connected at the terminal r concerning the terminal o, when the switch S_{x1} is conducted. Likewise, the terminal r achieves the voltage $V_{PV}/2$ when switch S_{x2} is turned ON. The switches S_{x1} and S_{x2} are integral in nature. The created voltage levels at the terminal r of Conv-1 are given as a contribution to the Conv-2. The positive, negative and zero levels of comparing input (voltage between the terminals r also, o) over the load are created by Conv-2. The bi-directional switches S_{x7} and S_{x8} give the free-wheeling way amid zero voltage state. The yield (output) of the five-level CMLI is associated with the grid through a LCL filter as appeared in Fig. 1 [16-18].

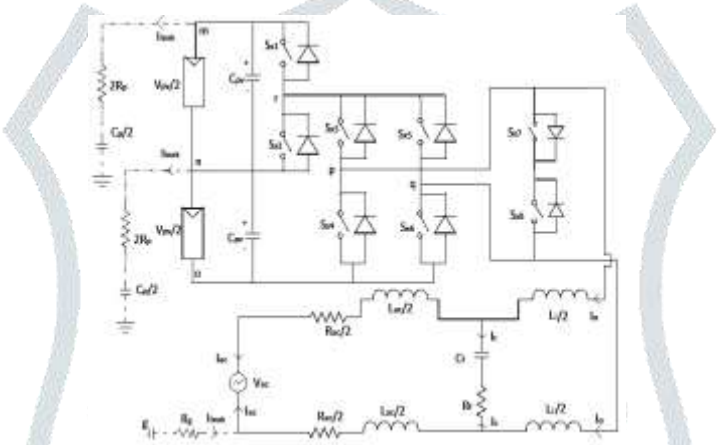

Fig. 1 Conventional five-level CMLI

Conventional five-level CMLI comprise of lattice (grid) side inductance L_{ac}, inverter side inductance L_i and capacitance C_f. The opposition R_f in the shunt branch of the channel is utilized as a damping resistor. The opposition R_{ac} alludes to the network side opposition, and the opposition R_g demonstrates opposition in the ground way. The variable V_{ac} alludes to instantaneous lattice voltage. The factors R_p and C_p allude to the parasitic opposition and capacitance in the PV framework individually appeared with spotted lines in Fig. 1. The factors i_o, i_c and i_{ac} signify the yield current of five-level CMLI, current moving through shunt branch of the channel and the present streaming into the framework individually. The leakage current spilling out of the PV panel into the ground through parasitic capacitance is represented as i_{leak}. The equations (1) and (2) shows the V_{po} and V_{qo} voltages of CMLI. By considering the average of V_{po} and V_{qo} voltages from equations (1) and (2), the common mode voltage V_{cm} can be obtained. By maintaining constant CMV at common mode terminals, the leakage currents are going to be reduced.

$$V_{po} = [s_1 s_3 + 0.5 s_2 s_3 - \frac{1}{(s_3 + s_4)} + \frac{1}{(s_3 + s_4)(s_1 + s_2)}]V_{pv} \quad (1)$$

$$V_{qo} = [s_1 s_5 + 0.5 s_2 s_5 - \frac{1}{(s_5 + s_6)} + \frac{1}{(s_5 + s_6)(s_1 + s_2)}]V_{pv} \quad (2)$$

The common mode voltage of conventional CMLI is

$$V_{cm} = [(s_1 + 0.5 s_2)(s_3 + s_5) + [\frac{1}{(s_3 + s_4)} + \frac{1}{(s_5 + s_6)}][\frac{1}{(s_1 + s_2)} - 1]]\frac{V_{pv}}{2} \quad (3)$$

Table. 1 Switching sequence of conventional CMLI

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{pq}
1	0	1	0	0	1	1	0	V_{pv}
0	1	1	0	0	1	1	0	$V_{pv}/2$
0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	1	$-V_{pv}/2$

1	0	0	1	1	0	0	1	$-V_{pv}$

The switching states of conventional CMLI topology is appeared in Table I. When switch Sx1 is turned ON together with other inverter switches (S_{x3}, S_{x6}) or (S_{x4}, S_{x5}) individually, the inverter output voltage achieves the voltage levels $+V_{PV}$ or $-V_{PV}$. In the same way, when switch S_{x2} is turned ON with a similar exchanging mixes the output voltage achieves voltage levels are $+V_{PV}/2$ or $-V_{PV}/2$. The most essential component to be seen amid zero voltage state or free-wheeling stage is the detachment or disengagement between PV source and the network (grid). By switching OFF all the switches of H-connect inverter, the separation between the PV source and the framework can be easily attained. The freewheeling path for the inductor current amid the switch OFF time of an switching cycle is provided by the bi-directional switches S_{x7} and S_{x8}. This activity helps in limiting the leakage current coursing through the parasitic capacitance.

3. Improved H6 Topology:

3.1 Operation of Improved H6 Topology:

The schematic circuit outline of the five-level enhanced H6 topology appeared in Fig. 2. This topology utilizes six switches for the generation of five levels in output (yield) voltage. Among six switches two switches S_1 and S_2 are integral switches. Anyway to limit the leakage current, the complimentary switching is utilized for the two sets of switches (S_3, S_6) and (S_4, S_5). The switches S_1 and S_2 are utilized to produce the voltage level of V_{pv} and $V_{pv}/2$. At the point when switch S_1 is turned ON, the voltage V_{pv} is connected at the terminal r concerning terminal o. Additionally, the terminal r accomplishes voltage $V_{pv}/2$ when switch S_2 is turned ON. This converter produces the positive, negative and zero level of comparing input voltage over the load.

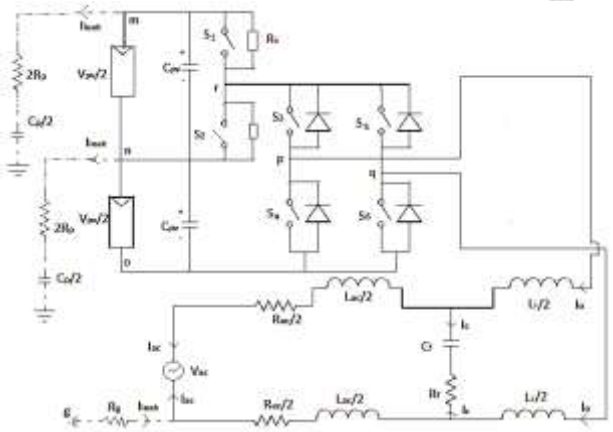

Fig. 2 Circuit diagram of improved H6 topology

It comprises of lattice (grid) side inductance L_{ac}, inverter side inductance L_i and capacitance C_f. The opposition R_f in the shunt branch of the channel is utilized as a damping resistor. The opposition R_{ac} alludes to the network side opposition, and the opposition R_g demonstrates opposition in the ground way. The variable V_{ac} alludes to instantaneous lattice voltage. The factors R_p, R_s and C_p allude to the parasitic opposition, snubber resistance and capacitance in the PV framework individually appeared with spotted lines in Fig. 2. The factors i_o, i_c and i_{ac} signify the yield current of five-level improved H6 topology, current moving through shunt branch of the channel and the present streaming into the framework individually. The leakage current spilling out of the PV panel into the ground through parasitic capacitance is represented as i_{leak}.

Table. 2 Switching states of improved H6 topology

S_1	S_2	S_3	S_4	S_5	S_6	V_{pq}
1	0	1	0	0	1	V_{pv}
0	1	1	0	0	1	$V_{pv}/2$
1	0	0	0	0	0	0
0	1	0	1	1	0	$-V_{pv}/2$
1	0	0	1	1	0	$-V_{pv}$

The output of the five levels H6 topology is associated with the grid. This enhanced H6 topology utilizes two Insulated Gate Bi-polar Transistor (IGBT) switches (S1 and S2) with anti parallel snubber resistance and four MOSFET switches (S3, S4, S5 and S6). Here the snubber resistances are used to avoid the short circuit at input side during the switches S_1 and S_2 conducted. The IGBT switches have high power exchange ability and work at low switching recurrence (frequency), which diminishes the switching losses and it has a low on state power dissipation. MOSFET's can be works at high exchanging recurrence [17 and 20] for minimizing high frequency transients. The main advantage of a MOSFET is that it requires almost no input current to control the load current, when compared with bipolar transistors. This enhanced H6 topology can be effectively fell to accomplish in excess of five levels in the yield voltage.

The inverter yield voltage V_{pq} at various voltage levels with the corresponding switching conditions of all switches are appeared in Table. 2. The inverter yield voltage V_{pq} achieves the voltage levels $+V_{pv}$ or $-V_{pv}$ when switch S_1 is turned ON alongside other inverter switches (S_3, S_6) or (S_4, S_5) individually. Likewise, the voltage levels $+V_{pv}/2$ or $-V_{pv}/2$ are acquired at V_{pq} when switch S_2 is turned ON with a similar exchanging blends. The most critical element to be seen amid zero voltage state or free-wheeling stage is the segregation or disengagement between PV source and the grid. The isolation between the PV source and the grid can be accomplished by turning OFF every one of the switches of the inverter [7]. As there is no direct connection between the two sources, the PV terminal points (nodes m, n and o) float and have undefined voltages. The float or undefined value restricts the terminal voltages from becoming zero. Thus, high-frequency voltage transitions at the PV terminals are avoided. In other words, the possibility of the flow of leakage current can be minimized. Also, in the other intermediate states like switching between $V_{PV}/2$ to V_{PV} or vice-versa, again the same principle can be used. The above action further helps in the minimization of the leakage current in the PV system.

3.2 Pulse Width Modulation Technique:

The operation of the proposed PWM technique is explained by considering the given five-level CMLI. The high-frequency transitions in the parasitic capacitance of five-level improved H6 topology are minimized using the proposed PWM technique. The suggested action can be achieved by switching from V_{PV} to 0 states or vice-versa instead of the switching from V_{PV} to $V_{PV}/2$ state or vice-versa. Additionally, during the zero voltage state of the switching cycle, the PV array is isolated from the grid. The isolation of the PV array and the grid during zero voltage state is similar to the inverter configuration reported in [15]. In this topology the switching pulses are directly generated by using the pulse generators and logic gates.

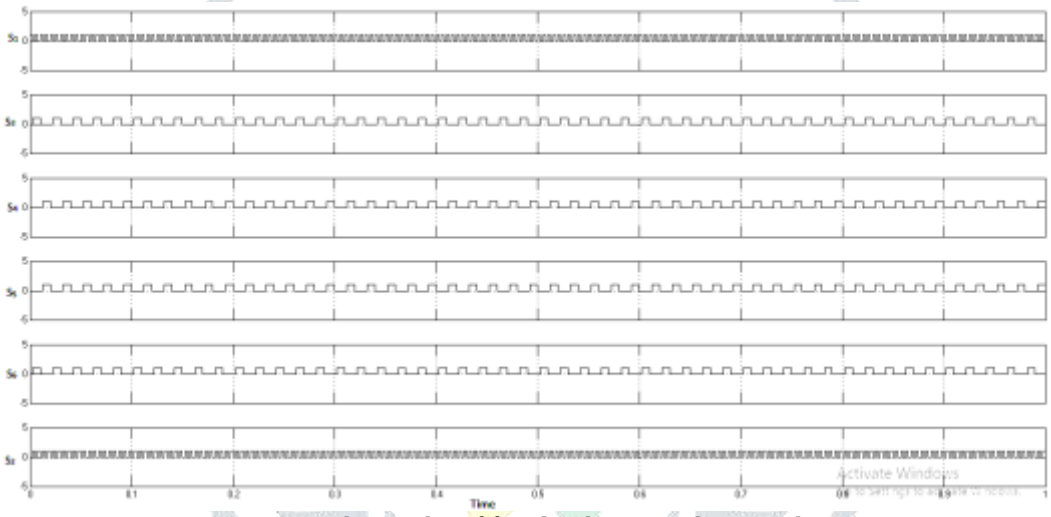

Fig. 3 Switching pulse of five-level improved H6 topology

Fig. 3 shows the switching pulses for the switches of five-level improved H6 topology. Here the switches S_1 and S_2 are complimentary switches and supplies V_{pv} and $V_{pv}/2$ input voltages to the multi-level inverter. The switching pairs (S_3,S_6) and (S_4,S_5) are also complimentary pairs. The leakage currents can be minimized by reducing high frequency transitions. These transitions can be reduced by using given PWM switching sequence. And high frequency transients are reduced by operating the MOSFET switches at high switching frequencies.

3.3 Integration of MPPT for improved H6 topology:

Photovoltaic systems normally use a maximum power point tracking (MPPT) technique to continuously deliver the highest possible power to the load when variations in the isolation and temperature occur, Photovoltaic (PV) generation is becoming increasingly important as a renewable source since it offers many advantages such as incurring no fuel costs, not being polluting, requiring little maintenance, and emitting no noise, among others. The well-known Incremental Conductance algorithm [20] is employed for the two PV sources individually to track Maximum Power Point (MPP). Thus, each MPPT algorithm tracks the MPP for respective PV sources. To track the MPP, the required information of (i) the average values of the two PV source voltages (V_{PV1} and V_{PV2} for the PV sources PV_1 and PV_2 respectively) and (ii) the currents (I_{PV1} and I_{PV2} for the PV sources PV_1 and PV_2 respectively) are sensed and then given to their respective MPPT algorithms. The disadvantage of the Perturb and Observe (P & O) method to track the peak power under fast varying atmospheric condition is overcome by IC method. The IC can determine that the MPPT has reached the MPP and stop perturbing the operating point. If this condition is not met, the direction in which the MPPT operating point must be perturbed can be calculated using the relationship between dI/dV and –I/V. This relationship is derived from the fact that dP/dV is negative when the MPPT is to the right of the MPP and positive when it is to the left of the MPP [14]. This algorithm has advantages over P&O in that it can determine when the MPPT has reached the MPP, where P&O oscillates around the MPP. Also, incremental conductance can track rapidly increasing and decreasing irradiance conditions with higher accuracy than P & O. Incremental conductance method has high response and well control for extracted power than P & O method [15].

4. Simulation results of improved H6 topology:

To support the switching function analysis given in the previous sections, the proposed five-level improved H6 topology is simulated using POWERSIM blocks in the MATLAB/SIMULINK software. Here the single diode solar panel with boost converter and grid connected improved H6 inverter models are designed in MATLAB software for getting required output voltage and minimized leakage currents. Another simulation is carried out with the proposed configuration to demonstrate the MPPT operation. The proposed five-level enhanced H6 topology is operated using Incremental Conductance (IC) MPPT algorithm to extract the maximum power from the individual PV arrays. In this topology, the IC MPPT algorithm is used for the two PV sources PV1 and PV2 which are identical (having same array configuration). Simulation is done considering a resistive load connected to the output of the inverter *via* an LC filter. The PV modules with an open circuit voltage of 20.50 V and short circuit current of 6 A at STC are chosen for the array simulation. The output voltage of each PV panel is V_{pv} = 110.01 V and output current of PV panel is i_{pv} = 5.56 A. Table III gives the value of various parameters used for simulating the five-level enhanced H6 topology.

Table. 3 Parameters considered for the simulation of improved H6 topology

parameter	P	V_{DC}	f_{sw}	V_{ac}	f_{ac}	R_f
value	4050.216W	220V	25kHz	220V	50Hz	1Ω
parameter	R_{ac}	R_g	R_s	C_f	L_i	L_{ac}
value	1Ω	0.1Ω	$1*10^5$Ω	6μF	4mH	20mH

The simulation waveforms of five-level output voltage and sinusoidal output voltages of improved H6 topology using the proposed PWM technique are shown in Fig. 4(a) & 4(b). The presence of zero voltage state in all the voltage transitions of V_{pq} can be clearly noticed from the plot. The sinusoidal waveform of grid current i_{ac} = 28 A which is shown in Fig. 4(c). The grid current is nearly sinusoidal. The Total Harmonic Distortion (THD) of grid current i_{ac} is around 1.06%. Fig. 4(d) shows the waveform for leakage current i_{leak} flowing through the parasitic capacitor. The proposed PWM technique reduces the value of leakage current as can be observed in Fig. 4(d). The spikes in the leakage current are observed when there is a sudden voltage transition in the terminal voltage. The RMS value of i_{leak} is less than 20mA which is as per the standard VDE0126-1-1[13]. The high-frequency voltage transitions in the common-mode voltage are also avoided. This further brings down the size, weight and cost of the EMI filter to be used in the grid-connected system [22].

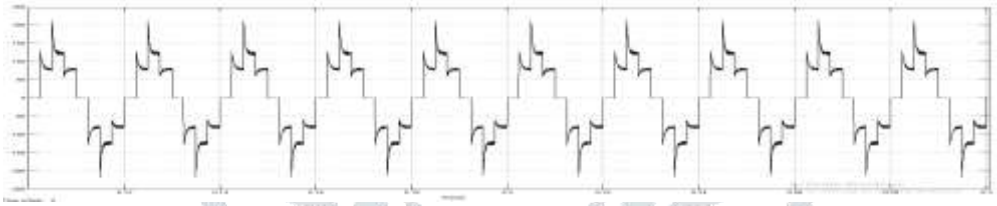

Fig. 4(a) Five-level output voltage of improved H6 topology

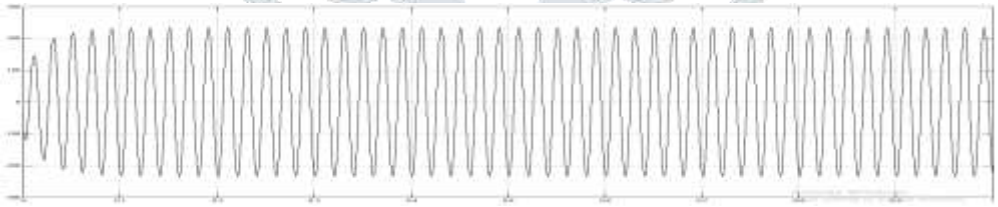

Fig. 4(b) Sinusoidal output voltage of improved H6 topology

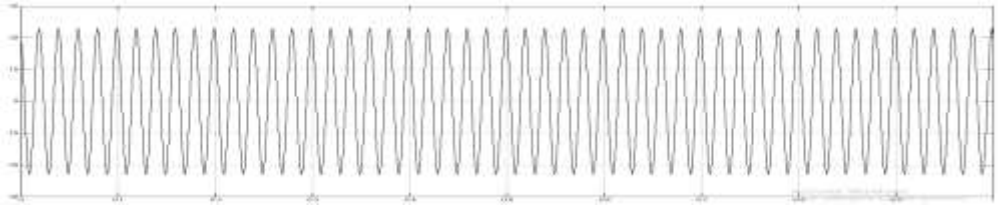

Fig. 4(c) Sinusoidal output current of improved H6 topology

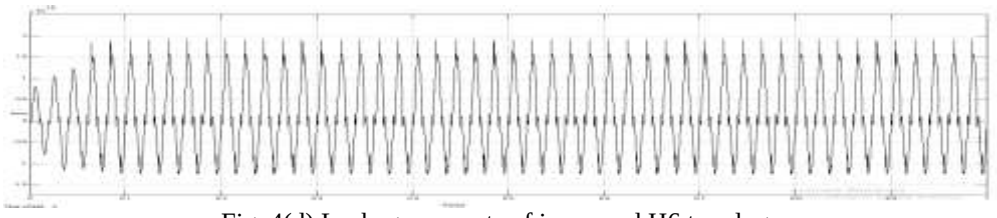

Fig. 4(d) Leakage currents of improved H6 topology

5. Comparison of Conventional CMLI and Improved H6 Topology:

Table. 4 Comparison of Conventional CMLI and Improved H6 topology

S. No.	Description	Conventional CMLI topology	Improved H6 topology
1	Number of switches used in the topology	8	6
2	Number of switches conducting during positive and negative half cycles	4	3
3	Number of switches conducting during zero voltage state	2	1
4	Switching and Conduction losses	low	low
5	Number of switches operating at high switching frequency	2	2
6	Number of switches operating at low switching frequency	3	4
7	Leakage current	5.6*10^-15 A	1.8*10^-15 A
8	Total harmonic distortion (THD)	2.16%	1.06%
9	Number of levels in output voltage	5	5

The proposed five-level improved H6 topology is compared with the existing CMLI topology which can be shown in table IV. The inverter configuration based CMLI and improved H6 topologies are designed to minimize the leakage currents for five-level transformer less PV system. The improved H6 topology will gives better performance and better results than the CMLI topology. The improved H6 topology uses less number of switches than CMLI topology for gaining the same five-level output voltage of CMLI. The switching and conduction losses of improved H6 topology is less because of this topology operates at lower switch count, lower switching frequency than the CMLI topology. Only one switch will be conducted at zero voltage in improved H6 topology. In CMLI topology two switches will be conducted at zero voltage state. Less number of switches conducted during the operation of improved H6 topology than CMLI, so the conduction losses will be reduced. The leakage currents can be minimized by maintaining constant common mode voltage and by reducing the high frequency voltage transitions at terminal and common mode voltage. By using PWM techniques, the high frequency voltage transitions can be minimized for the minimization of leakage currents. The leakage currents are less in improved H6 topology than the CMLI topology.

6. Conclusion:

Compared to CMLI, an improved five-level H6 topology with low switch count for the minimization of leakage current in a transformer less PV system is given better performance. The improved H6 topology with the designed pulse width modulation (PWM) technique reduces the high-frequency voltage transitions in the terminal and common-mode voltages. By avoiding the high-frequency voltage transitions achieves the minimization of the leakage current. This topology also has reduced conduction and switching losses. The improved H6 topology can be easily cascaded. Compared to CMLI, the leakage currents are less in five-level improved H6 topology. The outputs of the PV system are given to the inverter topology which is converted into sinusoidal and then the sinusoidal output voltages are given to the power grid. The IC MPPT algorithm is also integrated with the five-level improved H6 topology to extract the maximum power from the PV panels. The H6 topology is compared with the existing CMLI topology which is shown in table IV.

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