Design and Evaluation of Standalone Photovoltaic System Fed Asymmetric Multilevel Inverter

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Abstract- This paper presents a comparative study of solar fed single phase symmetric and asymmetric multilevel inverters. The solar fed symmetric and asymmetric multilevel inverters is triggered by multi carrier sinusoidal pulse width modulation (SPWM) technique. The SPWM technique include Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy, and Alternate Phase Disposition (APOD) strategy. Performance like %Total Harmonic Distortion (%THD), fundamental RMS voltage (Vrms) and Crest Factor (CF) are evaluated and the comparison results are presented. Simulation were performed using MATLAB/SIMULINK. It is observed that APOD PWM strategy provides output with lower distortions and higher fundamental RMS voltage.

Index Terms **-** Photovoltaic System, Boost Converter, Battery Management System, Symmetric Multilevel Inverters, Asymmetric Multilevel Inverters, Multicarrier Sinusoidal Pulse Width Modulation Technique, Total Harmonic Distortion.

I. INTRODUCTION

Renewable energy sources especially solar electric energy demand have become indispensable in the recent years because of low maintenance, cost, low noise, cleanliness, no moving parts and it is also a safe resource. Solar energy is converted into electrical energy by means of photovoltaic cells. A photovoltaic array converts sunlight into electricity [1]-[2]. The photovoltaic modules may fed to small loads such as lightning systems and DC-motors but energy obtained from the PV module acts as low voltage DC source and has relatively low efficiency [3]. In order to improve the efficiency and converting low voltage DC source into usable AC source, the power electronics converters are used to transform DC into DC and DC into AC [4]-[5].

Photovoltaic systems growth is mostly in standalone and grid connected applications. The basic components which are connected to photovoltaic systems are boost converter (DC-to-DC), batteries and inverter (DC-to-AC) for standalone applications. Inverters play a major role to convert the DC voltage into sinusoidal form [6]-[7]. Nowadays a multilevel inverter concept was introduced for increasing the number of levels in output voltage which leads to reduction of the harmonics without using passive filters. When higher number of levels is increased in output voltage, the harmonics will reduce dramatically. Therefore, MLIs are used for high voltage and high power applications [8]-[9]. Based on the configuration, MLIs can be classified into three major types. They are Diode Clamped Multilevel Inverter (DCMLI), Flying Capacitor Multilevel Inverter (FCMLI) and Cascaded H-Bridge Multilevel Inverter (CHBMLI). The operation of each configuration with their pros and cons has been explained detail in [10]. The DCMLI and FCMLI has required higher number of clamping diodes and clamping capacitors so that the design package is difficult. Based on the number of power semiconductor switches, the investment cost and size of inverter configuration become very high [11]-[12]. Due to these drawbacks, reduction of the component count without affecting the generation of voltage levels came into picture. Out of different structures of MLI's, Cascaded H-Bridge (CHB) MLI is more suitable converter for DC power source utilization [13]-[14]. The extension of the symmetric cascaded multilevel inverter topology is to increase the number of levels which involves more number of switches will leads to increase the complexity of the system with more number of gate driver circuits. Asymmetric multilevel inverters shows wider attention for reducing switching complexity. The multi carrier sine pulse width modulation (SPWM) strategy with Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy, and Alternate Phase Opposition Disposition (APOD) strategy has been analyzed as a control strategy for reduced switch count multilevel inverter [15]. The motivation of the solar fed asymmetric multilevel inverter with multi carrier SPWM technique is to reduce the lower order output harmonics and reduce the harmonic filtration circuit [16]. In other way, they enhance the quality of the produced electricity by making the wave form approaching the well behaved sine wave to feed to load and at the same time decreases the switching losses in which the switching frequency is low [17]-[18].

II. PV SYSTEM

The solid state device in solar panel is solar cell. Group of solar cell can be packed into modules, strings and arrays. PV module consists of a number of solar cells associated in series and parallel disposition [4]-[5]. The open circuit voltage of a silicon solar cell is 0.6V [4]. The power that one module can produce is not adequate to meet the load demand. Hence, the modules are connected in series and parallel to meet the power demand.

Single diode model of a solar cell has current source in parallel with an inverted diode along with a series and a parallel resistance. The series resistance is due to the path of flow of electrons from n-p junction and parallel resistance is due to the leakage current. Output current of PV-cell (I_{pv}) is given by

$$I_{PV} = N_P \times I_{ph} - N_P \times I_S \left[\exp\left(\frac{q \times \left(V_{PV} + I_{PV} R_{S)}\right)}{N_S \times A \times k \times T_C} \right) - 1 \right] \quad (1)$$

Table 1 PV panel specifications

Parameter	Value
Rated power (P_{max})	255W
Voltage at maximum power (V_{mp})	30.6V
current at maximum power (I_{mp})	8.33A
Open circuit voltage (V_{OC})	37.6V
Short circuit current (I_{SC})	8.84A
No. of solar cells in series (N_S)	60
No. of solar cells in parallel (N_P)	1

III. BOOST CONVERTER

The boost converter is a step-up DC-DC switching converter. With the help of boost converter, the low input-voltage level from the solar can be boosted up to a useful high output voltage level. While designing the conventional boost converter [11], as per the required output voltage the duty cycle is calculated by equation (6),

$$D = 1 - \frac{V_0}{V_{in}} \quad (2)$$

Table 2 Boost converter specifications

PARAMETERS OF BOOST CONVERTERS	CONVERTER-1	CONVERTER-2
Input voltage (V_{in})	30V	30V
Output voltage (V_{out})	100V	200V
Switching frequency (f_S)	40KHz	40KHz
Duty cycle (D)	0.7%	0.85%
Inductor current ripple (ΔI /I)	<=10%	<=10%
Input voltage ripple $(\Delta V_{in} / V_{in})$	<=1%	<=1%
output voltage ripple $(\Delta V_{out} / V_{out})$	<=1%	<=1%

IV. BATTERY MANAGEMENT SYSTEM

The battery in a photovoltaic system is charged regularly (often daily). The battery must be adequately charged during high sunshine hours to enable the full power delivery to the load at light fall. Generally, in photovoltaic applications the storage battery has the highest life time cost in the system; it has a profound effect on the reliability and performance of the system. Currently the most commonly used storage technology for photovoltaic applications is the lead acid battery. The advantages of the lead acid battery are its low cost and great availability. The problem is that photovoltaic panels are not an ideal source for charging batteries. With the lead acid battery the charging regime may have a significant impact on its service life.

V. SOLAR FED SYMMETRIC AND ASYMMETRIC MULTI-LEVEL INVERTER

5.1 Solar fed 7-level symmetric multilevel inverter

The DC sources of symmetric multilevel inverter configuration are equal in magnitude which is called symmetric multilevel inverter. The number of DC sources, number of switches and possible output voltage level are calculated using the following formulas,

Number of DC sources = K (3)

Number of switches (S) = 2K + 6 (4)

Number of levels (L) = 2K + 1 (5)

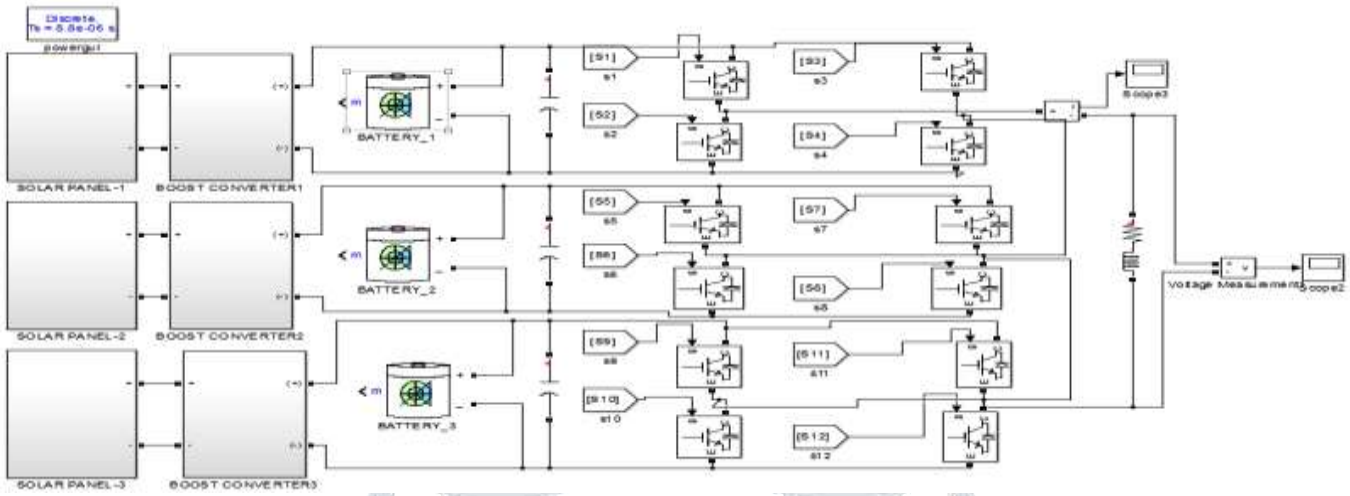

Figure 1 Solar fed 7-Level symmetric multilevel inverter

Figure 1 shows a circuit configuration of solar fed 7-level symmetric multilevel inverter with RL-load. The DC sources of this configuration are equal in magnitude. So, $Vdc_1 = Vdc_2 = Vdc_3 = 100$ V. Each H-bridge can produce voltage outputs in three levels +Vdc, 0, and –Vdc by four different combinations of switches, S1, S2, S3, and S4. In order to obtain +Vdc, switches S1 and S4 are turned ON whereas for obtaining –Vdc, we can turn ON switches S2 and S3. If we turn ON, S1 and S2 or S3 and S4, the output voltage is 0. Switching pulse waveform and switching states for 7-Level symmetric multilevel inverter is shown in **Figure 2** and **Table 3**. The AC output of each of every full-bridge inverter is connected in series so that the voltage waveform generated will be the summation of all the inverter output voltages.

Table 3 Switching states for 7-level symmetric multilevel inverter

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
3Vdc	1	0	0	1	1	0	0	1	1	0	0	1
2Vdc	1	0	0	1	0	1	0	1	1	0	0	1
Vdc	1	0	0	1	0	1	0	1	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0
-Vdc	0	1	1	0	1	0	1	0	1	0	1	0
-2Vdc	0	1	1	0	1	0	1	0	0	1	1	0
3Vdc	0	1	1	0	0	1	1	0	0	1	1	0

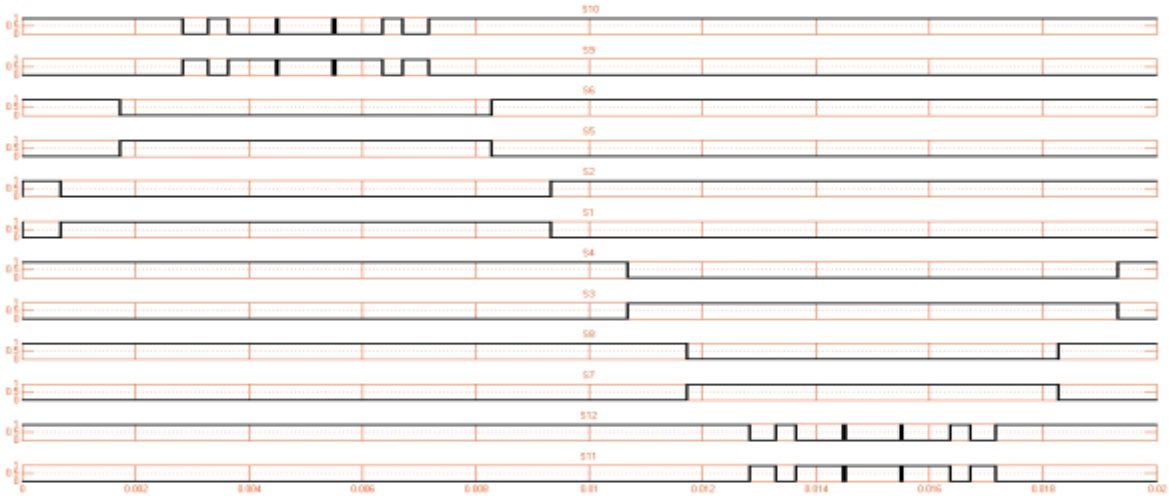

Figure 2 Switching pulse pattern for 7-Level symmetric multilevel inverter

5.2 Solar fed 7-level asymmetric multilevel inverter

The DC sources of asymmetric multilevel inverter configuration are not equal in magnitude which is called asymmetric multilevel inverter DC voltage ratio of binary and ternary are the most popular.The number of DC sources, number of switches and possible output voltage level are calculated using the following formulas,

$$\text{Number of DC sources} = N \quad (6)$$

$$\text{Number of switches (S)} = 4N \quad (7)$$

$$\text{Number of levels (L)} = 2^{N+1} - 1 \quad (8)$$

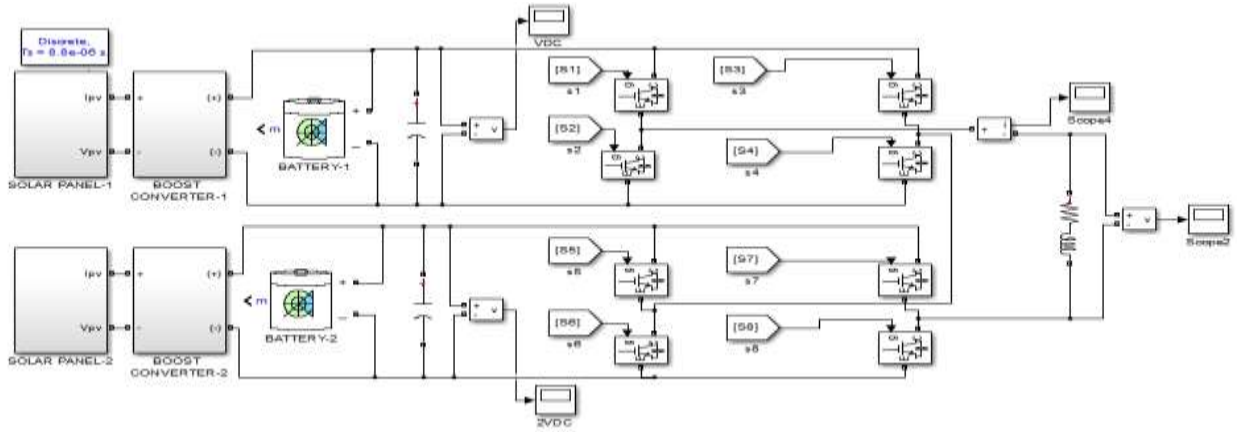

Figure 3 Solar fed 7-level asymmetric multilevel inverter.

Figure 3 shows a circuit configuration of solar fed 7-level asymmetric multilevel inverter with RL-load employing binary DC input source. So, Vdc = 100V, 2Vdc = 200V. It looks like a solar fed 7-level symmetric multilevel inverter except input DC sources. By using Vdc and 2Vdc, it can synthesize seven output levels; -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc. The lower inverter generates a fundamental output voltage with three levels, and then the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Switching pulse waveform and switching states for 7-Level asymmetric multilevel inverter is shown in **Figure 4** and **Table 4**. Here, the final output voltage levels becomes the sum of each terminal voltage.

Table 4 Switching states for 7-level asymmetric multilevel inverter.

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8
3Vdc	1	0	0	1	1	0	0	1
2Vdc	1	0	0	1	0	1	0	1
Vdc	1	0	0	1	0	1	0	1
0	0	0	0	0	0	0	0	0
-Vdc	0	1	1	0	1	0	1	0
-2Vdc	0	1	1	0	1	0	1	0
3Vdc	0	1	1	0	0	1	1	0

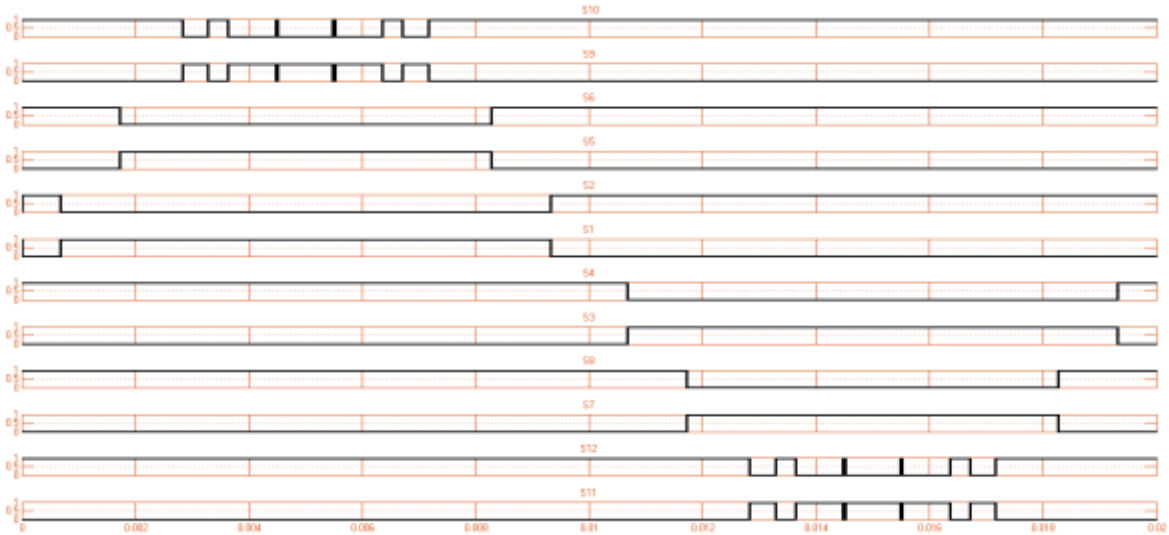

Figure 4 Switching pulse pattern for 7-Level asymmetric multilevel inverter.

In asymmetric multilevel inverter, the number of output-voltage levels can be dramatically increased without increasing the switching devices and DC-sources ratio of binary or in trinary ratio. The advantages of asymmetric topology are:

- ✓ Reduced number of DC sources.
- ✓ High conversion efficiency.
- ✓ Flexibility to enhance output levels.
- ✓ Better utilization of PV module.
- ✓ Reduction in circuit complexity and cost.
- ✓ Filtering circuit can be mitigated.

5.3 Multi carrier SPWM technique.

For this a multi carrier sine pulse width modulation technique is implemented, with a reference of sine wave and a triangular carrier is used to generate firing pulses for a 7-level symmetric and asymmetric multilevel inverters. For an n-level inverter using (n-1) carriers with the same frequency (fc) and same peak-to-peak amplitude (Ac) are used. The reference waveform has amplitude (Am) and frequency (fm) and it is placed at the zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on otherwise, the device switches off [6]. Hence, Amplitude Modulation Index

$$m_a = \frac{A_r}{A_c} \tag{9}$$

Frequency Modulation Index

$$m_f = \frac{f_c}{f_r} \tag{10}$$

Where

A_r= Peak amplitude of reference control signals.

A_c= Peak amplitude of the Triangular carrier wave.

f_c = frequency of the carrier wave.

f_r = reference sinusoidal signal frequency.

m_a-Determines the magnitude of output voltage.

f_r-controls the frequency of output voltage.

f_c-determines switching frequency of power semiconductor devices. Which means there exist 20 cycles of triangular waves for each cycle of sine wave.

There are many carrier arrangements to implement PWM strategy. In this work the following disposition of carrier strategies were carried out.

A. Phase disposition (PD) PWM strategy.

B. Phase opposition disposition (POD) PWM strategy.

C. Alternate phase opposition disposition (APOD) PWM strategy.

A. Phase disposition PWM strategy-In case of PDPWM strategy, all the carrier waveforms are in phase. The carrier arrangement is shown in **Figure 5.**

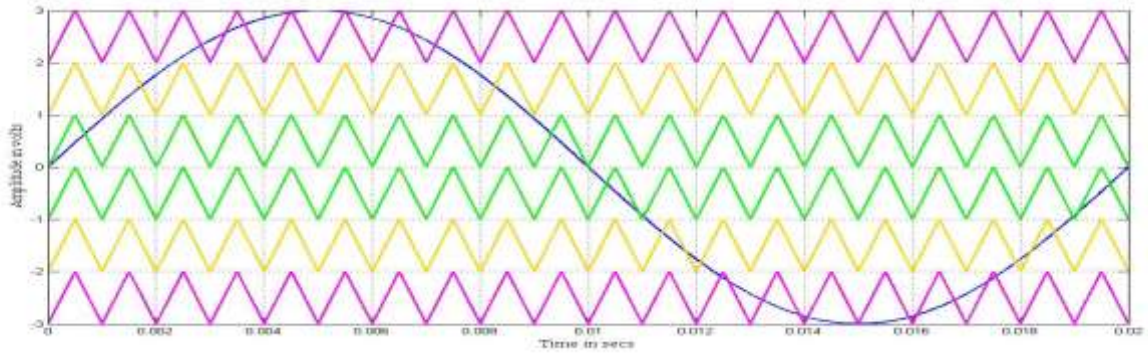

Figure 5 Multicarrier arrangement with sinusoidal reference for PDPWM strategy

B. Phase Opposition Disposition PWM strategy-In case of PODPWM strategy, the carrier waveforms above the zero reference are in phase. The carrier waveforms below the zero reference are also in phase but are180º phase shifted. The carrier arrangement is shown in **Figure 6**.

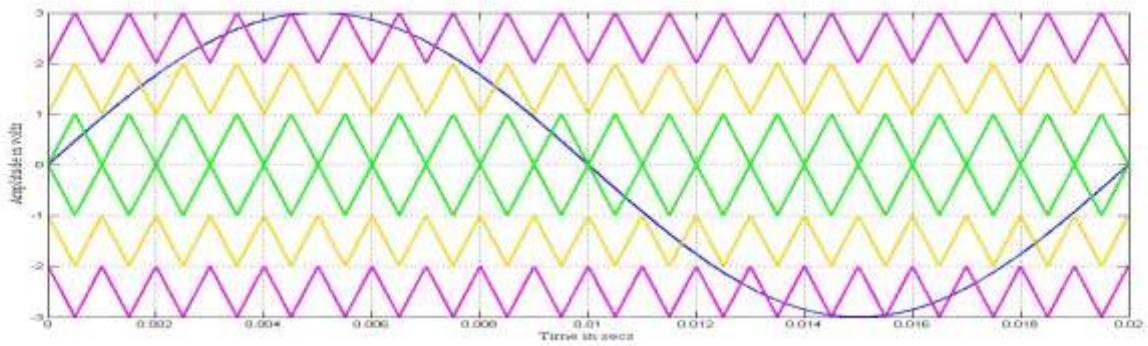

Figure 6 Multicarrier arrangement with sinusoidal reference for PODPWM strategy

C. Alternate phase opposition disposition PWM strategy-In case of APOD PWM, every carrier waveform is in out of phase with its neighbouring carrier by 180°. The **Figure 7** shows the carrier arrangement for APOD strategy [4].

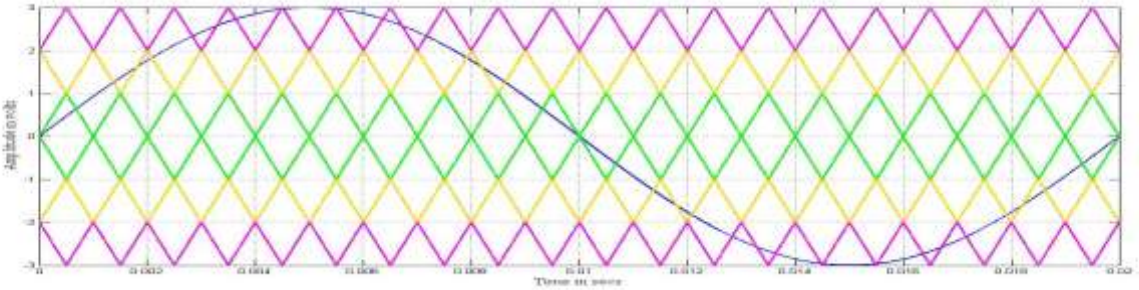

Figure 7 Multicarrier arrangement with sinusoidal reference for APODPWM strategy

VI. SIMULATION RESULTS

The single phase solar fed symmetric and asymmetric multilevel inverters is modeled in MATLAB/SIMULINK using power system block set. **Figure (8-10)** respectively shows the simulation, PV and IV graphs of 255W solar panel. **Figure (11-12)** respectively shows the output voltage and FFT plot for solar fed 7-Level symmetric multilevel inverter with APOD PWM strategy. **Figure (13-14)** respectively shows the output current and FFT plot for solar fed 7-Level symmetric multilevel inverter with APOD PWM strategy. **Figure (15-16)** respectively shows the output voltage and FFT plot for solar fed 7-Level asymmetric multilevel inverter with APOD PWM strategy. **Figure (17-18)** respectively shows the output current and FFT plot for solar fed 7-Level asymmetric multilevel inverter with APOD PWM strategy **Table 3** shows %Total Harmonic Distortion (%THD), fundamental RMS voltage (Vrms) and Crest Factor (CF) of output voltage. It is observed from the **Table 3**,

a) The single phase solar fed asymmetric topology can generate a large number of levels (odd and even) without increasing the number of switches and DC voltage sources.

b) APOD PWM strategy gives the lower THD-(9.75%), CF-(1.41447) with solar fed 7-level asymmetric multilevel inverter.

c) APOD PWM strategy gives higher fundamental RMS voltage (301V) with switching devices (8) and DC-sources (2).

The following parameter values are used for simulation: Vdc =300V, RL (load) = 50 ohms, fc=1000 Hz and fm=50Hz.

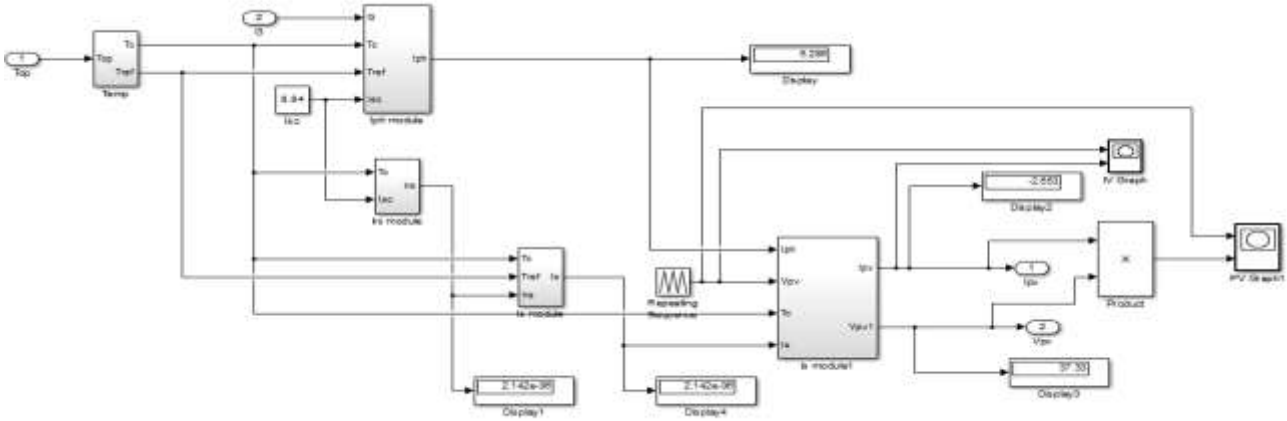

Figure 8 Simulation of 255W solar panel in MATLAB

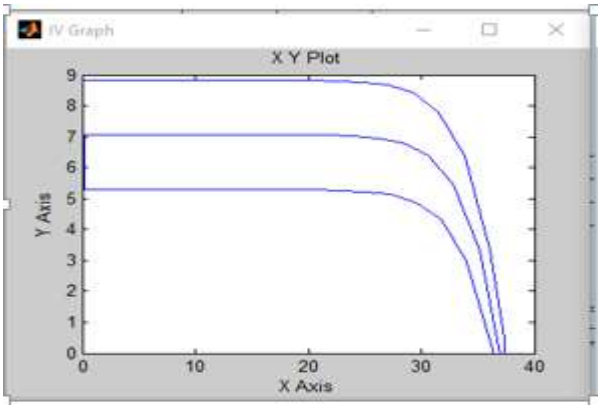

Figure 9 IV graph for 255W solar panel.

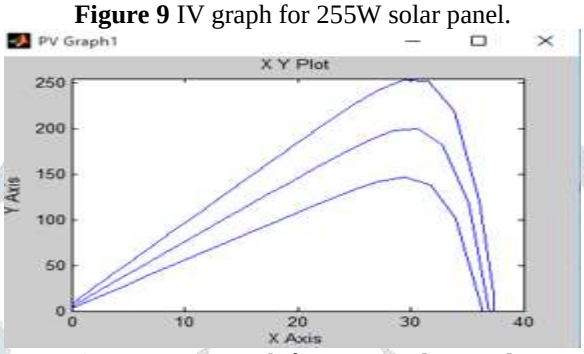

Figure 10 PV graph for 255W solar panel.

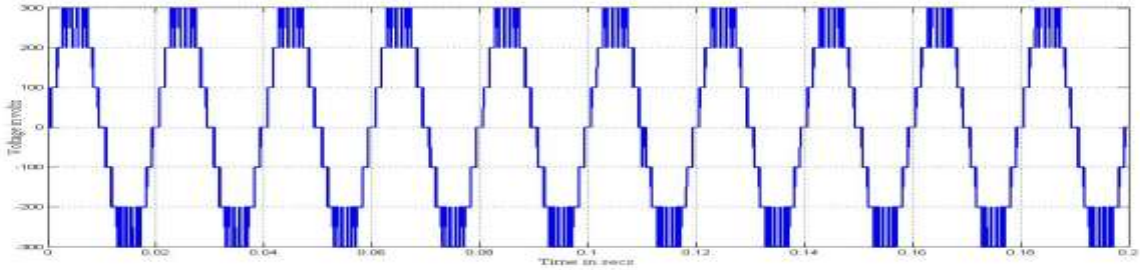

Figure 11 Solar fed 7-Level symmetric multilevel inverter output voltage waveform with APOD PWM strategy

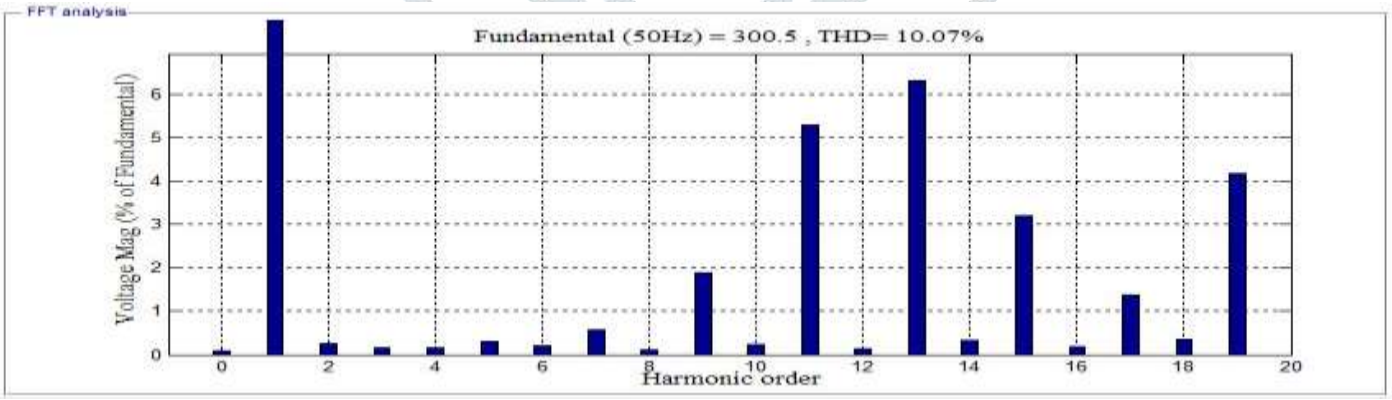

Figure 12 FFT plot for output voltage of solar fed 7-Level symmetric multilevel inverter with APOD PWM strategy.

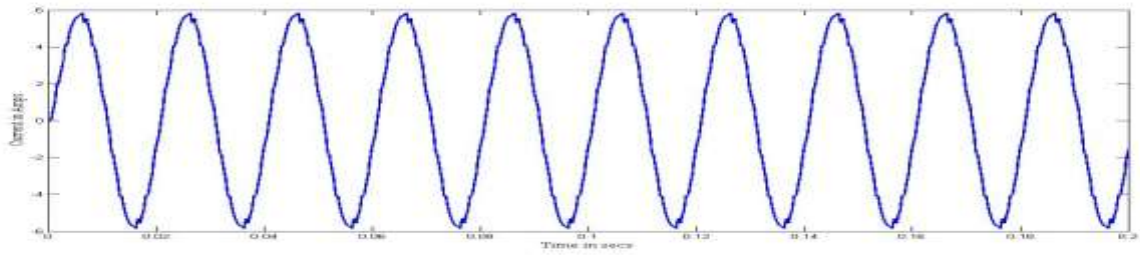

Figure 13 Solar fed 7-Level symmetric multilevel inverter output current waveform with APOD PWM strategy

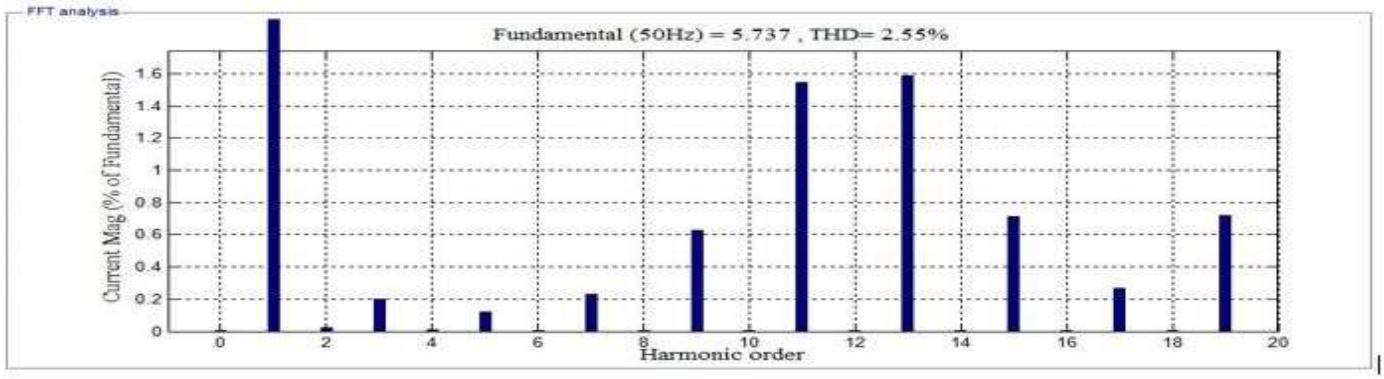

Figure 14 FFT plot for output current of solar fed 7-Level symmetric multilevel inverter with APOD PWM strategy.

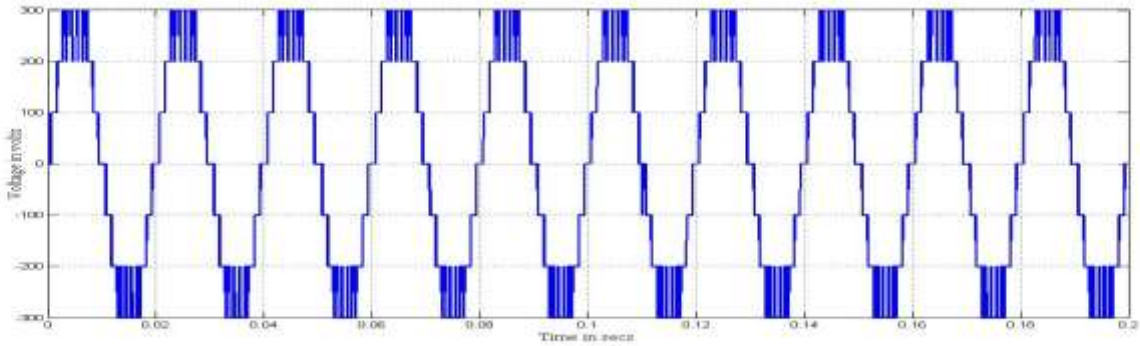

Figure 15 Solar fed 7-Level asymmetric multilevel inverter output voltage waveform with APOD PWM strategy

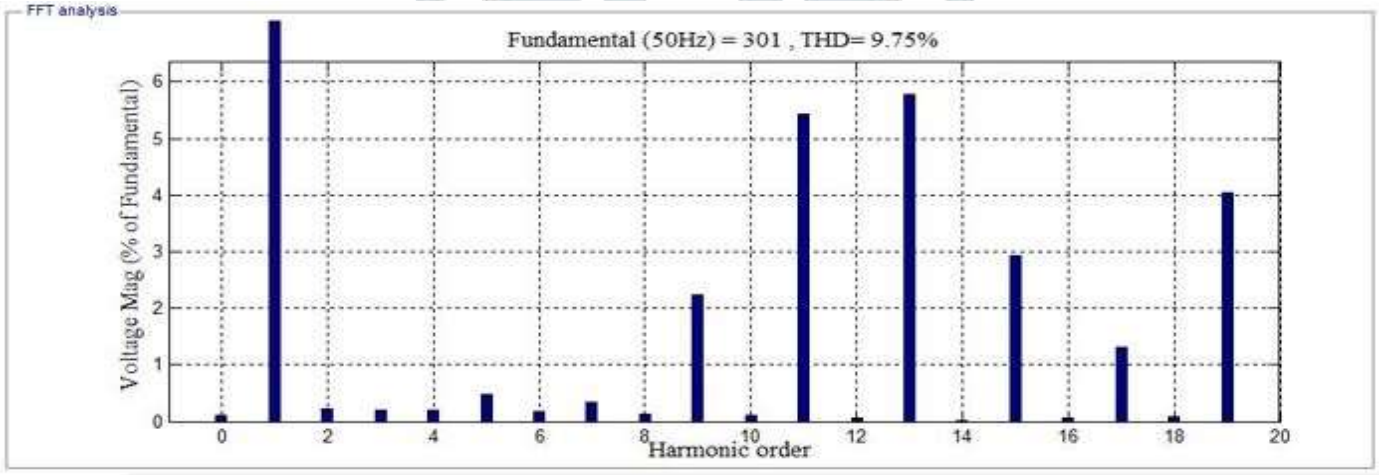

Figure 16 FFT plot for output voltage of solar fed 7-Level asymmetric multilevel inverter with APOD PWM strategy.

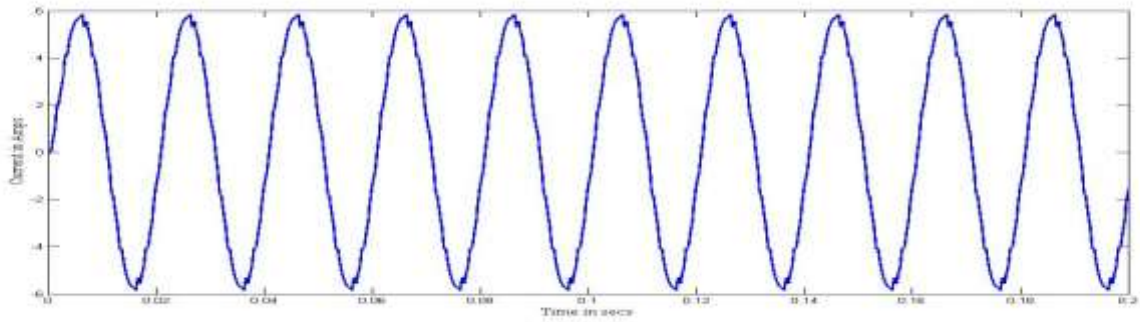

Figure 17 Solar fed 7-Level asymmetric multilevel inverter output current waveform with APOD PWM strategy

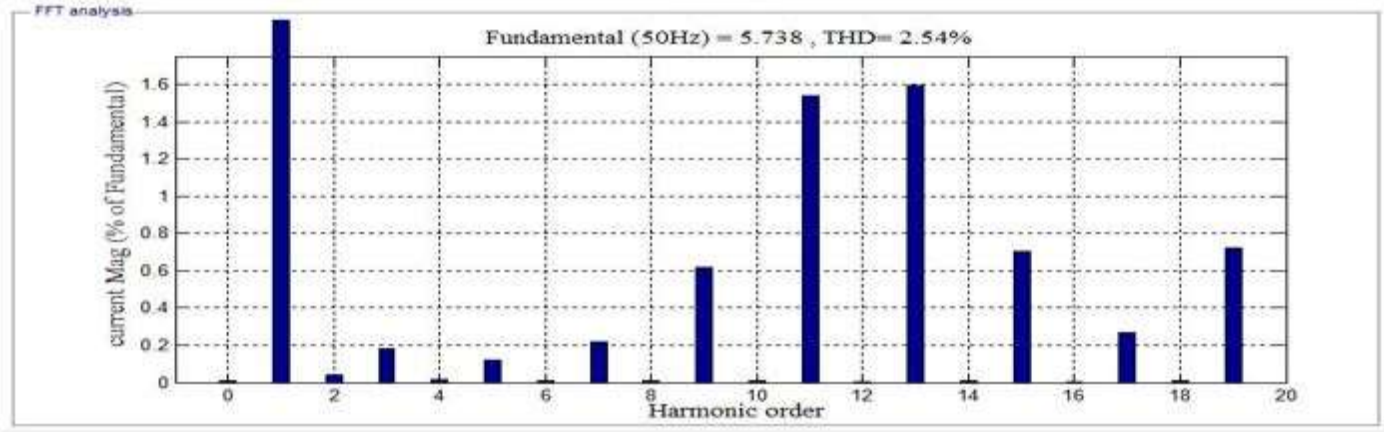

Figure 18 FFT plot for output current of solar fed 7-Level asymmetric multilevel inverter with APOD PWM strategy.

Table 3 Comparison of existing and proposed solar fed multilevel inverters

PARAMETER	**SOLAR FED SYMMETRIC MULTILEVEL INVERTER**			**SOLAR FED ASYMMETRIC MULTILEVEL INVERTER**		
No. of levels	7			**7**		
No. of switches	12			**8**		
	PD	**POD**	**APOD**	**PD**	**POD**	**APOD**
Fundamental and RMS voltage	299.7V (211.9V)	299.5V (211.8V)	300.5V (212.5V)	300.5V (212.5V)	300.4V (212.4V)	**301V (212.8V)**
Crest factor (CF)	1.41434	1.41406	1.41411	1.41411	1.41431	**1.41447**
Voltage Total Harmonic Distortions	12.88%	10.43%	10.07%	12.70%	10.37%	**9.75%**
Current Total Harmonic Distortion	3.48%	2.75%	2.55%	3.43%	2.76%	**2.54%**

VII. CONCLUSION

In this paper, a standalone solar fed symmetric and asymmetric (binary-DC source) 7-level multilevel inverter have been presented. The solar fed 7-level asymmetric multilevel inverter gives higher output voltage with lower harmonics when compared to solar fed 7-level symmetric multilevel inverter as is evident from **Table 3.** The performance factors like %THD, Vrms and CF have been evaluated and presented. APOD PWM strategy with solar fed 7-level asymmetric multilevel inverter gives lower THD, higher fundamental RMS voltage (Vrms) and Crest Factor (CF) with less switching devices compare to solar fed 7-level symmetric multilevel inverter.

VIII. ACKNOWLEDGMENT

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