BLDC Motor Fed Seventeen-Level Inverter Formed by Cascading Flying Capacitor and Floating Capacitor H-Bridges

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Abstract

In his paper presents a multilevel inverter for generating 17 voltage levels utilizing a three-level flying capacitor inverter and fell H-connect modules with coasting capacitors has been proposed. Different angles of the proposed inverter like capacitor voltage adjusting have been exhibited in the present paper. The security of the capacitor adjusting calculation has been confirmed both amid homeless people and enduring state operation. Every one of the capacitors in this circuit can be adjusted promptly by utilizing one of the post voltage mixes. Another preferred standpoint of this topology is its capacity to produce every one of the voltages from a single dc-link control supply which empowers consecutive operation of converter.

I. INTRODUCTION

WITH the approach of multilevel inverters, the execution of medium and high-voltage drives have changed radically. As the quantity of voltage levels expands, the output voltage is nearer to sine wave with decreased symphonious content, enhancing the execution of the drive significantly as exhibited. One of the pioneering works in the field of multilevel inverters is the unbiased point clipped inverter.

Then again, the utilization of various disconnected dc sources utilizing H-bridges for plasma adjustment creating different voltage levels was exhibited. The work exhibited examines the issues with the plan of falling numerous rectifiers what's more, proposes an answer for adjusting the capacitors. The work exhibited produces different voltage levels by switching the load current through capacitors. Here, the voltage throughthe capacitors

can be kept up at wanted an incentive by evolving the bearing of load current through the capacitor by picking the excess states for a similar post voltage. Here, the drifting capacitor H-bridge is utilized to create different output voltages. The voltages of the capacitors are kept up at their planned values by switching through repetitive states for a similar voltage level. The works introduced in address parts of utilizing fell H-bridges and propose different effective control calculations. Secluded multilevel converters which are extremely prevalent in HVDC applications are another type of multilevel converters which can be utilized for engine drive applications as displayed. The idea of falling flying capacitor inverter with impartial point cinched inverter is exhibited. Comparable idea has been made accessible economically as ABB ACS 2000. The idea of expanding the quantity of levels utilizing flying capacitor inverter with cross connected capacitors has been introduced. An intriguing design to create 17 voltage levels utilizing various capacitors is exhibited. However the capacitor voltages can't be adjusted immediately. They can be adjusted just at the basic frequency. A single-phase seventeen-level inverter series is exhibited in utilizes huge number of power supplies and has a coasting stack. This is more reasonable for STATCOM applications. An alluring calculation for working seventeen level inverter has been displayed.

In the present paper, we propose another 17-level inverter framed by falling three-level flying capacitor inverter with coasting capacitor H-spans which utilizes a solitary dc supply and determines all the required voltage levels from it. The execution of the proposed series is tentatively confirmed both for steady state operation and amid homeless people and the outcomes are exhibited.

II. POWER CIRCUIT TOPOLOGY

The proposed converter is a crossover multilevel topology utilizing a three-level flying capacitor inverter and falling it with three coasting capacitor H-Bridges. The three-phase control schematic is appeared in Figure 1. The voltages of capacitors AC1, BC1, and CC1 are kept up at Vdc/2. Capacitors AC2, BC2, what's more, CC2 are kept up at voltage level of Vdc/4. Additionally capacitors AC3, BC3, and CC3 are kept up at voltage level of Vdc/8 and capacitorsAC4, BC4, and CC4 are kept up at voltage level of Vdc/16. Each fell H-extension can either include or subtract its voltage to the voltage produced by its past phase. Notwithstanding that, the CHBs can likewise be avoided. The subsequent inverter post voltage is the number-crunching total of voltages of each series.

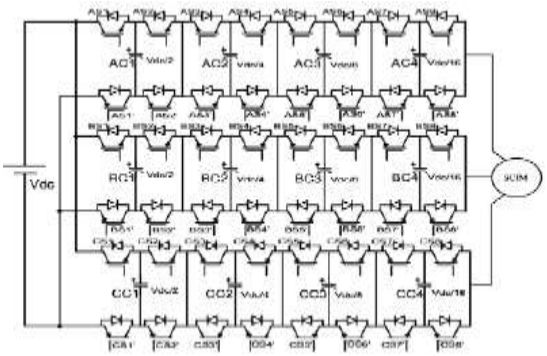


Figure 1: Three-phase power schematic of the proposed seventeen-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

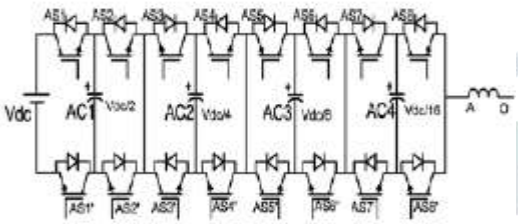


Figure 2: One phase of the proposed 17-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

The schematic chart for one period of the proposed converter is appeared in Fig. 2. The switch sets (AS1, AS1'), (AS2, AS2'), (AS3, AS3'), (AS4, AS4'), (AS5, AS5'), (AS6, AS6'), (AS7, AS7'), and (AS8, AS8') are switched in integral mold with suitable dead time. Every switch combine has two

particular rationale states, in particular top device is ON (indicated by 1) or the base device is ON (signified by 0). In this way, there are 256 (28) particular switching mixes conceivable. Every voltage level can be created utilizing at least one switching states (shaft voltage redundancies). By switching through the excess switching mixes (for a similar shaft voltage), the current through capacitors can be switched and their voltages can be controlled to their endorsed values. This technique for adjusting the capacitor voltages at all loadcurrents and power considers quickly has been watched for 17 shaft voltage levels. They are 0, Vdc/16, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. Notwithstanding, by switching through all the conceivable post voltage switchingcurves, 31 unmistakable post voltage levels can be created utilizing the proposed topology. In the extra 14 levels, the voltages of capacitors can be adjusted just in an essential cycle.

There are 82 switching mixes (see Table I) that can be utilized to create the previously mentioned 17 post voltage levels where momentary capacitor voltage adjusting is conceivable. The impact of 82 switching mixes on each capacitor's charge state (charge or release) for positive bearing of current (i.e., when the shaft is sourcing present as set apart in Figure 3) is appeared in Table I. For negative bearing of current, the impact of the switching state on the capacitor is turned around. For instance, at the point when the controller requests a shaft voltage of Vdc/16, there are five distinctive excess changing curves to create it. Every switching mix differently affects the state of charge of the capacitors. At the point when the switching state (0, 0, 0, 0, 0, 0, 0, 1) (see Table I) is connected, the capacitor C4 releases at the point when the post is sourcing present as [see Figure 3(a)]. To adjust the capacitor C4 and to take its voltage back to the recommended esteem (Vdc/16), one of the other four switching curves is connected Figure 3(b)–3(e). It can be watched that when switching state (0, 0, 0, 0, 0, 1, 1, 0) is connected, the course of current in the capacitor C4 is turned around [see Figure 3(b)] and the capacitor C4 charges. However in this procedure, the capacitor C3 is released. In the event that the capacitor C3 needs charging, switching state excess of (0, 0, 0, 1, 1, 0, 1, 0) is connected [see Figure 3(c)] which releases C2. To charge C2 one of the switching redundancy appeared in Figure 3(d) and 3(e) is connected in light of the state of charge of capacitor C1. In the case of switching state (0, 1, 1, 0, 1, 0, 1, 0) is connected, the capacitor C1 is released and this state charges the various capacitors as appeared in Figure 3(d). At last, when switching condition of (1, 0, 1, 0, 1, 0, 1, 0) is connected, all the four capacitors are charged for positive heading of present as appeared in Figure 3(e). By switching through the excess post voltage curves, it can be watched that the every one of the capacitors' voltages can be kept up at their recommended values while creating post voltage of Vdc/16 for positive bearing of current. Assuming all the capacitors require releasing, the capacitor C4 is released initially and the rest of the capacitors can be released amid ensuing switching cycles when C4 should be charged. For negative heading of current, the impact of the capacitor voltages is the inverse. The whole procedure of capacitor voltage adjusting for post voltage of Vdc/16 that has been clarified is shown in Figure 4. Here, the capacitor voltage variety with application of different repetitive states for post voltage of Vdc/16 has been appeared for positive heading of current. For other post voltages specifically, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc, a comparative technique can be utilized to adjust all the capacitor voltages. The switchingfrequency of any CHB module is at most the PWM switchingfrequency the converter. This is because of the synchronization of utilization of the switching state with each PWMtransition (the switching state is locked till the following PWM move). In addition in this conspire, just the capacitors that add to the output shaft voltages are switched.

III. SPACE VECTOR CONTROL REGION

Each pole of the three-phase inverter can generate one of the 17 discrete pole voltage levels namely 0, Vdc/16, Vdc/8,3Vdc/16, Vdc/4, 5Vdc/16, 3Vdc/8, 7Vdc/16, Vdc/2, 9Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, also, Vdc. For the proposed three-phase inverter, there is an aggregate of 4913 (173) shaft voltage curves.

Every post voltage mix produces a voltage space vector V SV as given in the accompanying condition:

$$V_{SV} = V_{AN} + V_{BN}\angle 120^\circ + V_{CN}\angle 240^\circ \qquad (1)$$

WhereV_{AN} , V_{BN} and V_{CN} are the three-phase voltages. These 4193 post voltage curves when set apart on a space vector plane spread crosswise over 817 particular space vector areas. Each of the 817 space vector areas can have more than one shaft voltage curve (phase voltage repetition) with various basic mode voltages. Likewise, every shaft voltage can have at least one repetitive switching mix (post voltage repetition which can be utilized to adjust the capacitor voltages of that specific phase) as depicted in the past segment. The outline of the space vector polygon framed by these 817 areas is appeared in Figure 5. There 16 concentric hexagons that frame the space vector control area of the proposed seventeen-level inverter. The space vectors on the external hexagon don't have any phase voltage redundancies. The areas on the second biggest hexagon have twofold excess also, can be created with two series of post voltages with various normal mode voltages. For the littler internal hexagons, the number of shaft voltage mixes for producing the space vector areas increments. There are 16 redundantpole voltage mixes each with an alternate regular mode voltage for every space vector area on the internal generally hexagon. In this manner, the zero state at the middle has a sum of seventeen shaft voltage mixes all of which create zero differential mode voltage.

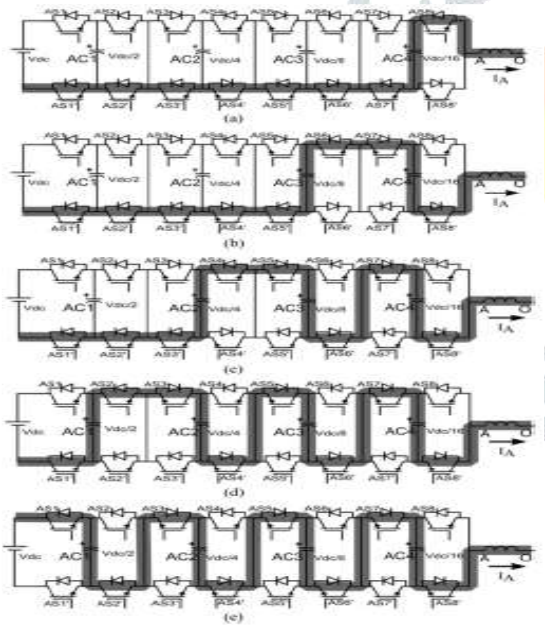


Figure 3: Switching Redundancies for pole voltage of Vdc/16. (a) Current pathfor switching state (0, 0, 0, 0, 0, 0, 0, 1). (b) Current path for switching state (0, 0, 0, 0, 0, 1, 1, 0). (c) Current path for switching state (0, 0, 0, 1, 1, 0, 1, 0). (d) Current path for switching state (0, 1, 1, 0, 1, 0, 1, 0). (e) Current path for switching state (1, 0, 1, 0, 1, 0, 1, 0).

IV. IMPLEMENTATION

The piece chart of the controller to create the switching signals for the inverter is introduced in Fig. 6. The control calculation can be anything like V/f or vector control or some other calculation which requests a specific series of reference voltage levels for the three phases. These voltage levels are sent to level-moved bearer based space vector PWM generation calculation actualized in DSP as depicted , the output of which is (bolstered to FPGA) an seriesof level information and the PWM flag for every phase. This information is nourished to a level synthesizer which produces the quick level in view of the PWM flag and

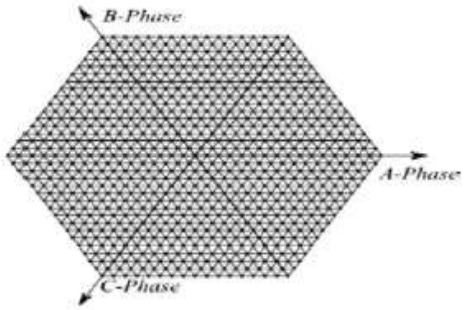


Figure 4: Space vector polygon formed with the proposed five-level inverter.

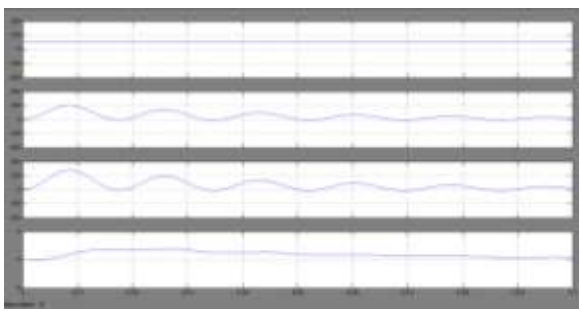
The level information. The immediate level information is nourished to aswitching state generator which creates a suitable switching state in light of the requested level, the condition of capacitor voltages and current. This is accomplished by actualizing This switching state is nourished to a dead time generation circuit which creates the gating signals for the top and base devices which have correlative operation with reasonable dead time. The dead time generation circuit is likewise actualized in FPGA in this manner avoiding any need for outside equipment and giving reliable dead band.

Extension topic

In this project we used seventeen level inverter to fed SCIM (Squirrel cage induction motor). But The SCIM has some drawbacks like operated in lagging power factor, efficiency is low and required maintenance. Therefore we overcome these problems we go for another motor drive like BLDC motor (Brush less DC motor). The BLDC motor has some features like power factor is high, efficiency is high and there is no brushes there is no requirement of maintenance of brushes therefore cost of motor reduces and no need for regular maintenance. The BLDC motor also small in size and also operated for AC and DC supply.

Because of this reasons we go for BLDC motor in place of SCIM. In extension we fed BLDC motor with seventeen level inverter and check the performance of the BLDC motor.

Proposed Simulation Results



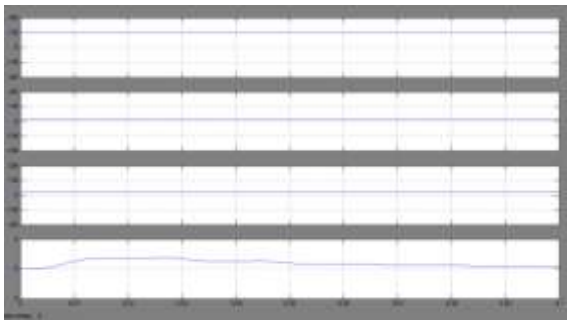


Figure 5: Pole, Phase, capacitor voltages along with current for 10-Hz operation of converter. VAC1 (50 V/div),VAO: Pole voltage (100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (100 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: (20 mS/div).

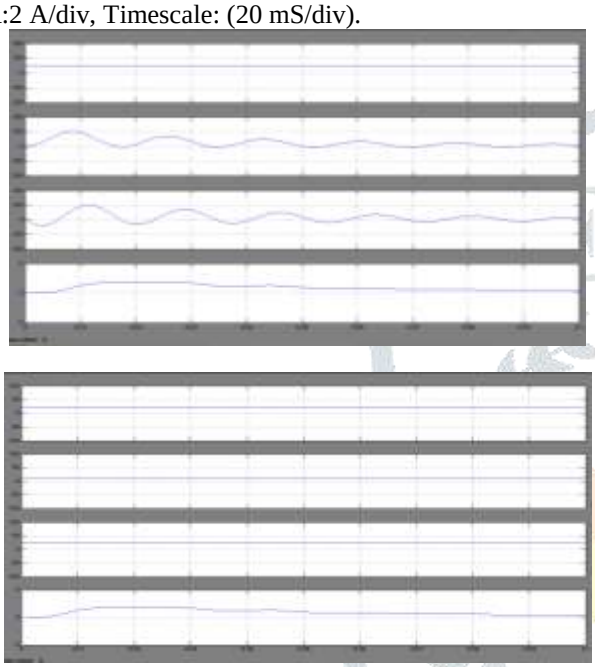
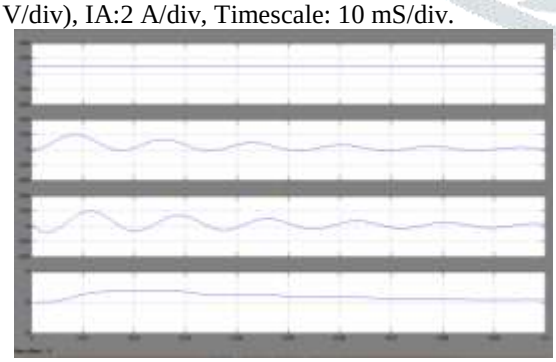


Figure 6: Pole, Phase, capacitor voltages along with current for 20-Hz operation of the converter. VAC1: (50 V/div),VAO: Pole voltage(100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (20 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.



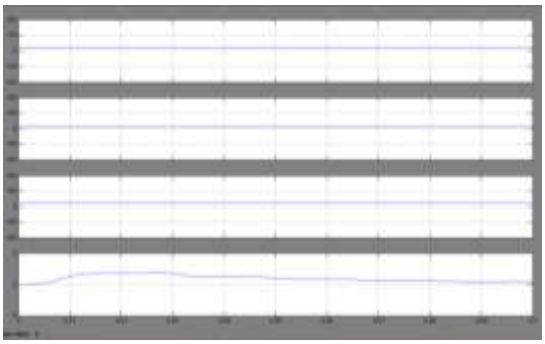


Figure 7: Pole, Phase, capacitor voltages along with current for 30-Hz operation of the converter. VAC1 :(50 V/div),VAO: Pole voltage(100 V/div),VAN: Phase Voltage (100 V/div), VAC4: (20 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.

Figure 8: Pole, Phase, capacitor voltages along with current for 40-Hz operation of the converter. VAC1:(50 V/div),VAO: Pole voltage(100 V/div),VAN: Phase Voltage (100 V/div), VAC4: (10 V/div),VAC3: (10 V/div),VAC2: (100 V/div), IA:2 A/div, Timescale: 5 mS/div.

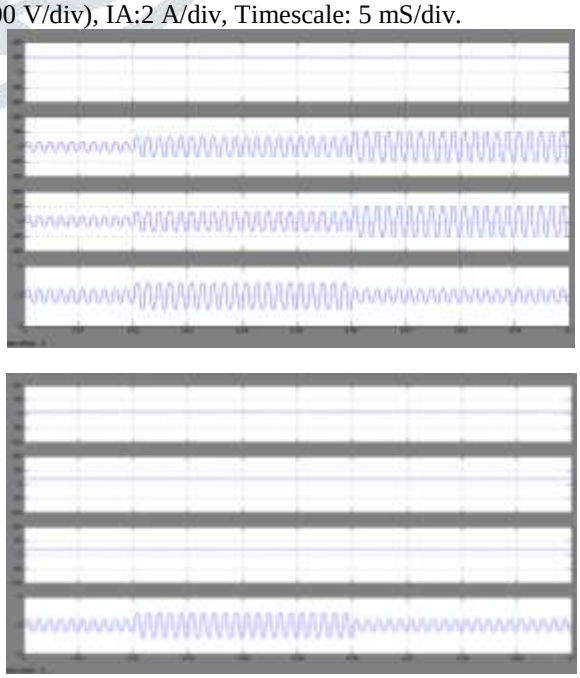


Figure 9: Pole, Phase, capacitor voltages along with current during sudden acceleration. VAC1:Cap AC1 voltage(100 V/div), VAO: Pole Voltage(100 V/div), VAN: Phase Voltage(100 V/div),VAC4:Cap AC4 voltage(10 V/div), VAC3:Cap AC3 voltage (20 V/div), VAC2:Cap AC2 voltage (20 V/div),IA: Phase current (2 A/div) Timescale: 500 mS/div.

Extension Simulation Results

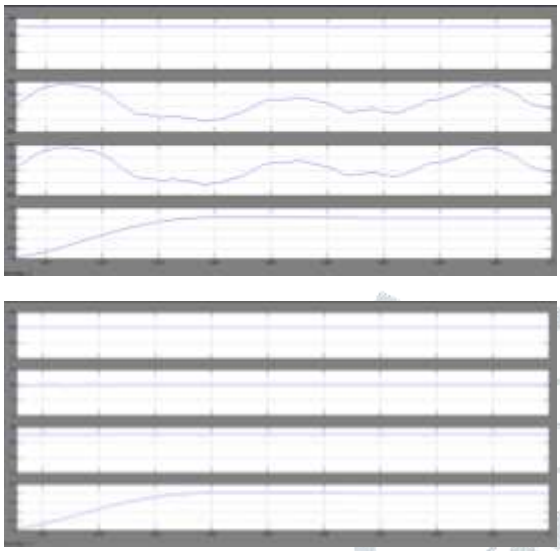


Figure 10: Pole, Phase, capacitor voltages along with current for 10-Hz operation of converter. VAC1 (50 V/div),VAO: Pole voltage (100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (100 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: (20 mS/div).

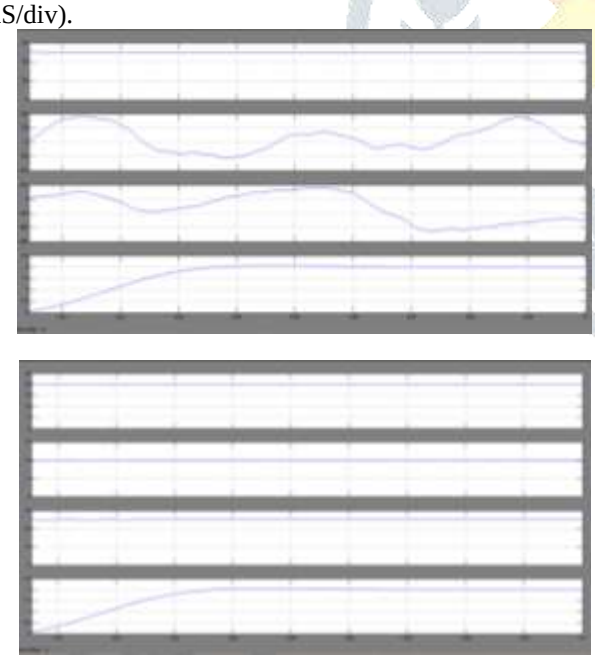


Figure 11: Pole, Phase, capacitor voltages along with current for 20-Hz operation of the converter. VAC1: (50 V/div),VAO: Pole voltage(100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (20 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.

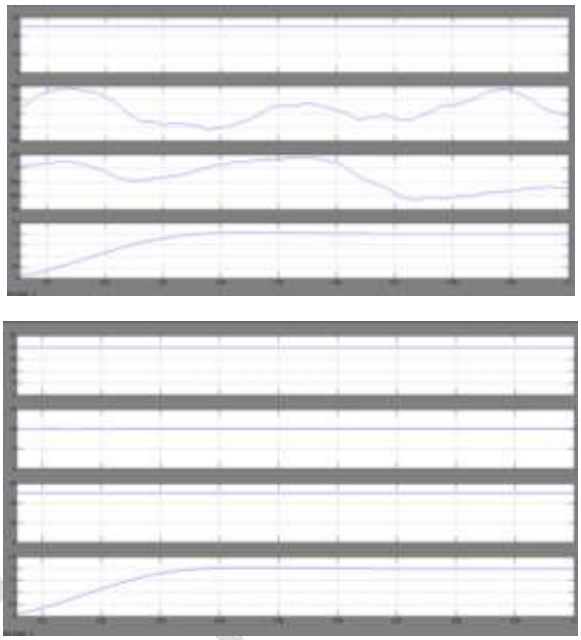


Figure 12: Pole, Phase, capacitor voltages along with current for 30-Hz operation of the converter. VAC1 :(50 V/div), VAO: Pole voltage (100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (20 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.

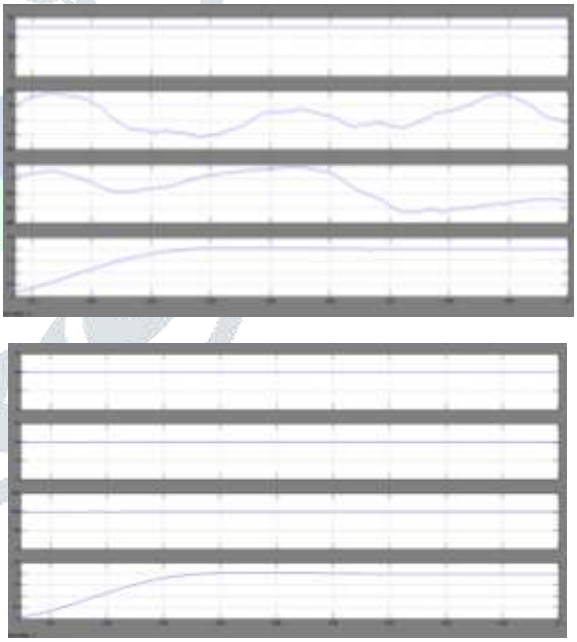
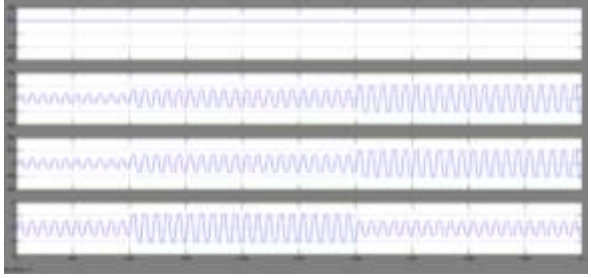


Figure 13: Pole, Phase, capacitor voltages along with current for 40-Hz operation of the converter. VAC1:(50 V/div),VAO: Pole voltage(100 V/div),VAN: Phase Voltage (100 V/div), VAC4: (10 V/div),VAC3: (10 V/div),VAC2: (100 V/div), IA:2 A/div, Timescale: 5 mS/div.



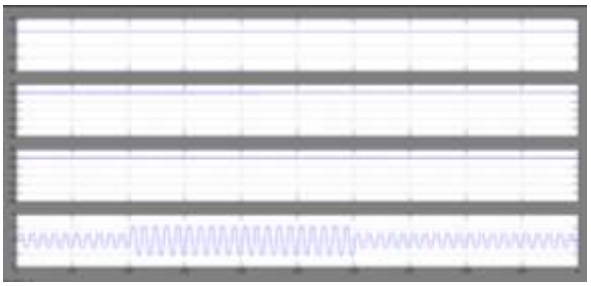


Figure 14: Pole, Phase, capacitor voltages along with current during sudden acceleration. VAC1:Cap AC1 voltage(100 V/div), VAO: Pole Voltage(100 V/div), VAN: Phase Voltage(100 V/div),VAC4:Cap AC4 voltage(10 V/div), VAC3:Cap AC3 voltage (20 V/div), VAC2:Cap AC2 voltage (20 V/div),IA: Phase current (2 A/div) Timescale: 500 mS/div.

CONCLUSION

Another 17-level inverter design shaped by falling a three-level flying capacitor and three gliding capacitor Hbridges has been proposed interestingly. The voltages of each of the capacitors are controlled promptly in few switching cycles at all loads and power components getting elite output voltages and currents. The proposed series utilizes a single dc connection and determines the other voltage levels from it. This empowers consecutive converter operation where power can be attracted and provided to the lattice at endorsed control consider. Too, the proposed 17-level inverter has enhanced dependability. On the off chance that of disappointment of one of the H-bridges, the inverter can even now be worked with decreased number of levels providing full energy to the stack. This element empowers it to be utilized as a part of basic applications like marine drive and footing where unwavering quality is of most height concern. Another preferred standpoint of the proposed design is particularity and symmetry in structure which empowers the inverter to be stretched out to more number of phases like five-phase furthermore, six-phaseseries with a similar control plot.

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