

A HIGHLY RELIABLE And EFFICIENT QUASI SINGLE STAGE BUCK-BOOST INVERTER.

[1] Rohini, [2]Manish G Rathi.

[1] M.tech student, [2]Professor

[1] Dept of Power Electronics, PDA engineering College, Kalburgi, Karnataka,India.

ABSTRACT

This paper proposes a novel high efficiency quasi single-stage single-phase buck-boost inverter. The proposed inverter can solve current shoot-through problem and eliminate PWM dead-time, which leads to greatly enhanced system reliability. It allows bidirectional power flow and can use MOSFET as switching device without body diode conducting. The reverse recovery issues and related loss of the MOSFET body diode can be eliminated. Also, the proposed inverter can be operated with simple PWM control and can be designed at higher switching frequency to reduce the volume of passive components.

KEY WORDS

Buck-boost, dual-buck, efficiency, inverter, MOSFET, reliability, switching cell, single-stage, Z-source.

INTRODUCTION

For dc to ac power conversion, there are two converters: voltage source inverter (VSI) and current source inverter (CSI)[1-3] [5]. The VSI has only buck (or step-down) function and is vulnerable to shoot-through (or arm short) problem caused by electromagnetic interference (EMI) noise. Similarly, the CSI has only boost (step-up) function and is vulnerable to open-circuit (or arm open) problem caused by EMI. In order to avoid the shoot-through problem, a finite dead-time in gate signals is required for the VSI. Likewise, a finite overlap-time is required for the CSI to prevent the open-circuit problem. The dead-time or overlap-time causes output waveform distortion. Output voltages of renewable energy sources change in a wide range. To regulate an inverter output voltage in systems having wide input dc voltage variation, a buck-boost power conditioning system is preferred.

Inverter: Which converts the DC voltage into AC voltage .There are two types .They are

1. Voltage source inverter (VSI).
- 2.. Current source inverter (CSI).

Voltage source inverter (VSI): in many industrial application, to control the output voltage of inverters is often necessary to cope with the variations of dc input voltage, to regulate voltage of inverters and to satisfy the constant volts and frequency control requirement. There are various techniques to vary the inverter gain. The efficient method of controlling the gain is to incorporate PWM control within the inverter. In the voltage source inverter (VSI) the input voltage is maintained constant and output voltage not dependent on the load. VSI requires feedback diodes and the control circuit is complicated. Current source inverter (CSI): The input behaves as a current source. The output current is maintained constant irrespective of load on the inverter and the output voltage is forced to change. Buck-Boost converter: A Buck Boost converter can be obtained by the cascade connection of the two basics converters the step-down converter and step- up converter. This allows the output voltage to be higher or lower than the input voltage, based on the duty ratio D . The cascade connection of the step-down and step-up converters can be combined into the single Buck-Boost converter.

I. CIRCUIT DIAGRAM

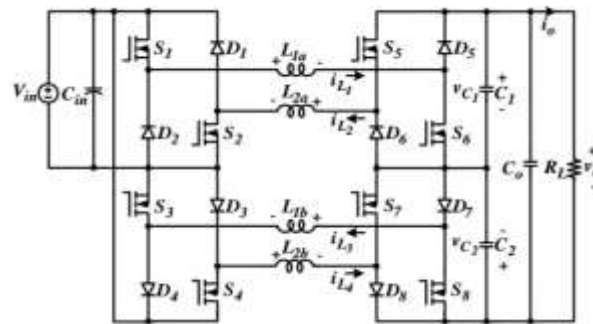


Fig.1. Proposed Buck-Boost inverter.

Fig. 1 shows the circuit topology of the proposed quasi single-stage BBI. It is a combination of the dual-buck and switching cell (SC) structures. The dc input of the proposed inverter takes the dual-buck structure and the ac output takes the SC ac-ac structure. Similar to the qzsi and the dual-buck inverter, the proposed inverter is very resistant to EMI noise's. The proposed inverter can be designed with MOSFET, therefore, high frequency and high efficiency operation can be realized. As shown in Fig. 1, each switching device is connected in series with an external diode, therefore no shoot-through current is possible in the proposed inverter. The inductors L_{1a} , L_{1b} , L_{2a} , L_{2b} split the phase legs and serve as buck, boost and current limiting inductors. The two capacitors C_1 and C_2 in the output are added to provide a safe path for inductor currents when dead-time occurs in the gate signals. They also serve as both output filter capacitor and lossless snubbers reducing the voltage spikes caused by the stray inductances in the circuit layout.

A. Buck Operation

PWM strategy during the buck operation is depicted Fig. 3 The switches S_6, S_7 are always OFF and S_5, S_8 are ON, that is, $D=0$. The diodes D_6, D_7 are reverse biased and D_5, D_8 are forward biased. The equivalent circuit during the buck operation is shown in Fig.2. During the buck operation, the proposed inverter reduces to the dual-buck inverter with only one extra MOSFET and diode conducting the main current at a time. The inductor L_{1a} and L_{1b} conduct the main current during the positive half-cycle of output current with the direction shown in Fig. 4 , and L_{2a} and L_{2b} conduct current during the negative half-cycle of output current. During the buck operation, the proposed inverter has two consecutive modes as discussed below. In the following mode analysis, all the inductors are assumed to have an equal inductance, $L/2$. Fig.3 shows the operation when the output current is positive and the same analysis can be made for the negative half-cycle of current.

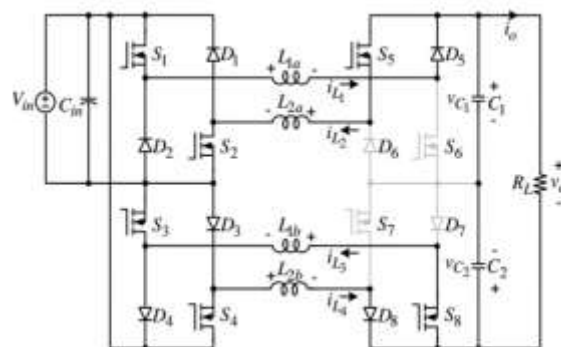


Fig.2. Equivalent circuit of the proposed inverter during Buck operation

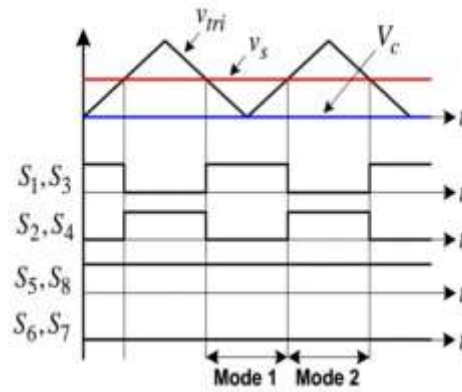


Fig.3. PWM strategy during buck operation.

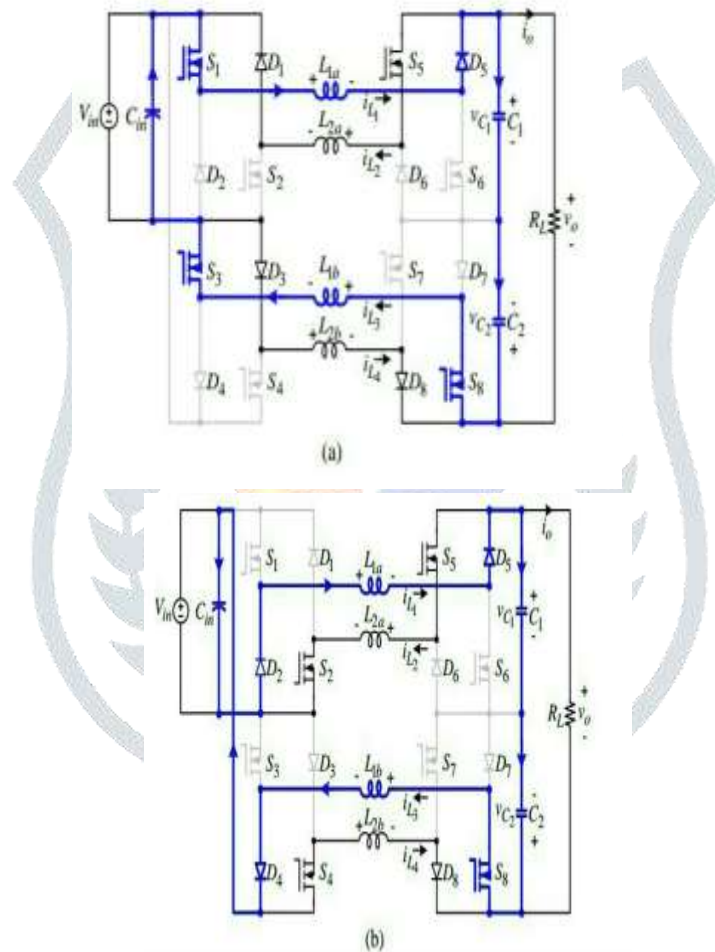


Fig.4 buck operation of the proposed inverter, (a)Mode1 (b)Mode2 .

Mode1

As shown in Fig.4 (a), the switches S1,S3 are turned-on and S2,S4 are turned-off, thus the diodes D2, D4 are reverse biased. The current relation is given as follows:

$$\frac{diL1}{dt} = \frac{(Vin-v0)}{L} \quad (1)$$

Mode2

As shown in Fig. 4(b), the switches S1, S3 are OFF and S2, S4 are ON, and the diodes D2, D4 are forward biased due to freewheeling action. The current relation is given as follows

$$\frac{diL1}{dt} = \frac{-Vin-v0}{L} \quad (2)$$

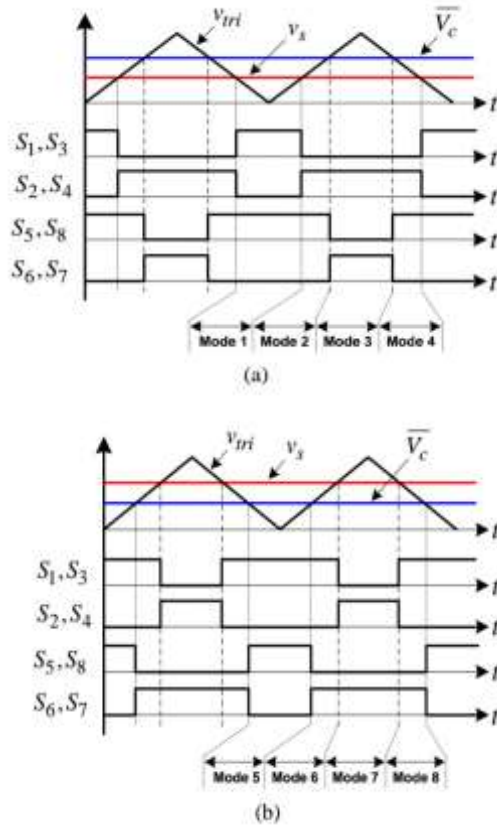


Fig.5 PWM strategy during boost operation. (a) $V_{in} > v_0$ (or $V_c > v_s$). (b) $V_{in} < v_0$ (or $V_c < v_s$).

B.Boost operation

During the Boost operation, M is set to 1, and D is varied to regulate v_0 . The switching states are shown in Fig. 5. In Fig. 5 V_c is defined as $(1-D)$ and it is the dc control signal that determines the duty cycle of switches S_5, S_8 that is, $(1-D)$. Fig. 5(a) shows the switching signals when $V_c > v_s$ (or when the instantaneous output voltage is lower than V_{in}). Fig 5(b) shows the switching signals for $v_s > V_c$. In this paper, the voltages before and after inductors are designated as dc-bridge and ac-bridge voltages, respectively. The dc-bridge voltage is varied between 0 and v_0 . The inductors L_{1a} and L_{1b} , and (L_{2a} and L_{2b}) are in series, therefore the voltage across L_{1a} or L_{1b} becomes $V_{in}/2, -V_{in}/2, (V_{in}-v_0)/2$, and $(-V_{in}-v_0)/2$. Similarly, during the negative half cycle, the voltage across L_{2a} or L_{2b} become $V_{in}/2, -V_{in}/2, (-V_{in}+v_0)/2$. Modes 1-4 for $V_{in} > v_0$ are shown in Fig. 5(a), and modes 5-8 for $V_{in} < v_0$ are shown in Fig 5(b)

Mode1&5: These modes are the same as mode 1 of the buck operation shown in Fig 6(a).

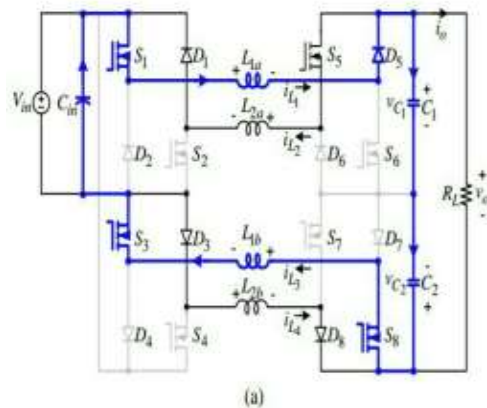


Fig. 6(a) Boost operation of the proposed inverter. Mode 1&5.

2) Mode 2&4 These modes are the same as mode 2 of the buck operation shown in Fig. 6(b).

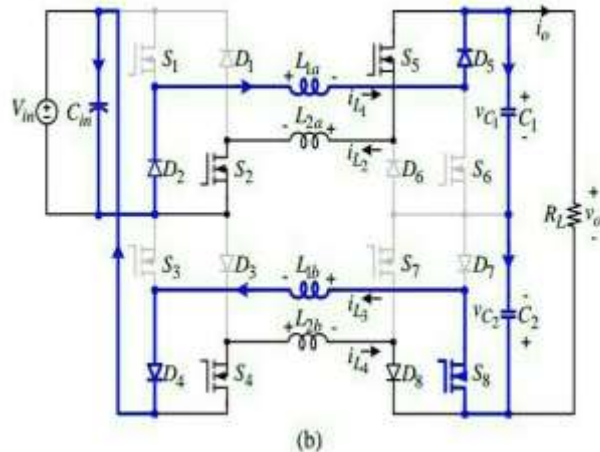


Fig. 6(b) Boost operation of the proposed inverter. Mode 2&4

3) Mode 3&7 In mode 3 and 7, as shown in Fig. 7(a), the switches S1, S3, S5, and S8 are OFF and the switches S2, S4, S6, and S7 are ON. The inductor current decreases with a slope as:

$$\frac{di_{L1}}{dt} = -\frac{V_{in}}{L} \quad (3)$$

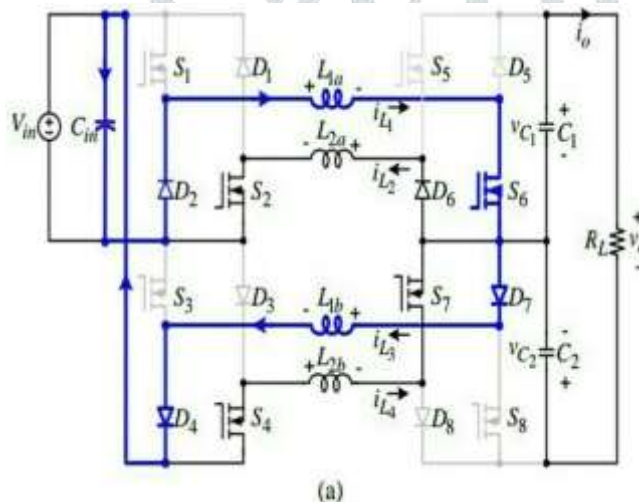


Fig. 7(a) Boost operation of the proposed inverter. Mode 3&7.

4) Mode 6&8 In mode 6 and 8, as shown in Fig. 7(b), the switches S1, S3, S6, and S7 are ON, and S2, S4, S5, and S8 are OFF. The inductor current rises with a slope as.

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L} \quad (4)$$

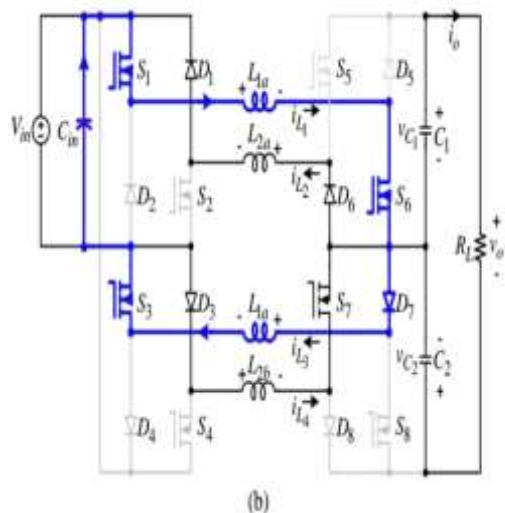


Fig. 7(b) Boost operation of the proposed inverter. (b) Mode6&8.

RESULTS ANALYSIS

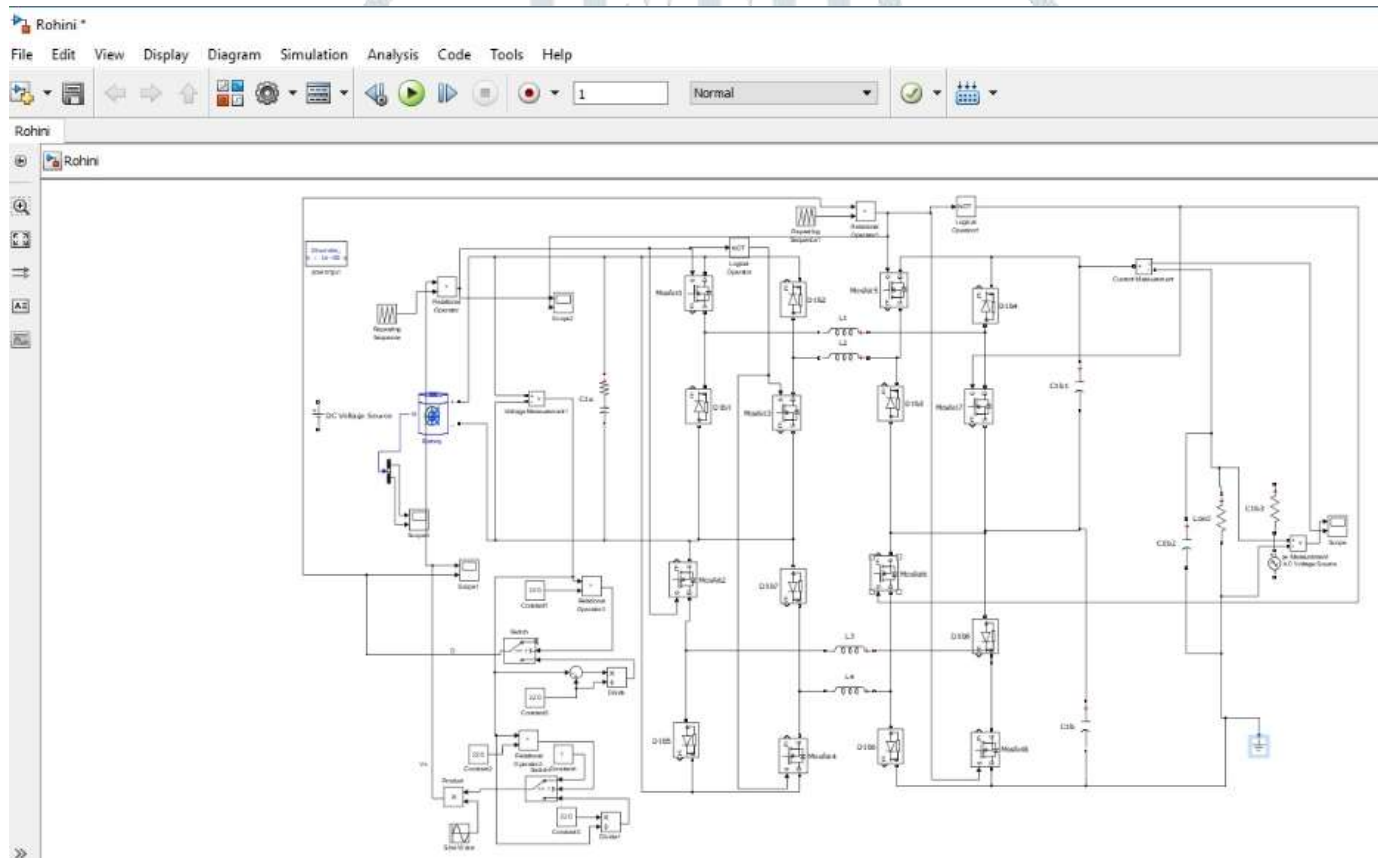


Fig 9: Simulation circuit.

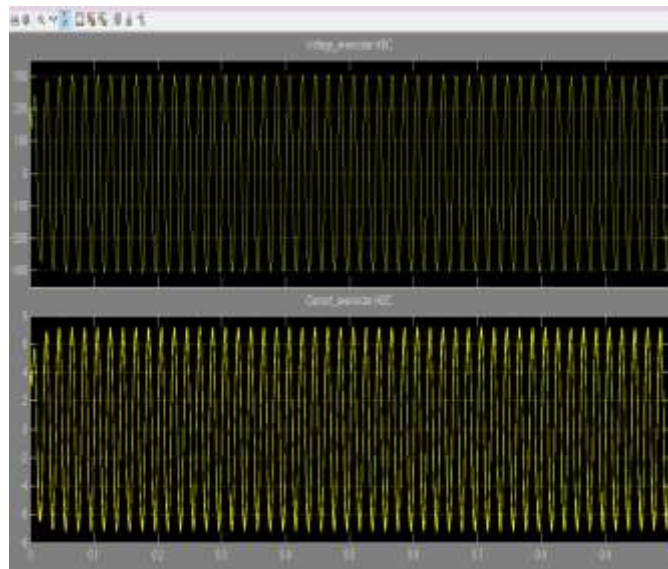


Fig9: INPUT is ($V_{in}=250$) BOOST OUTPUT

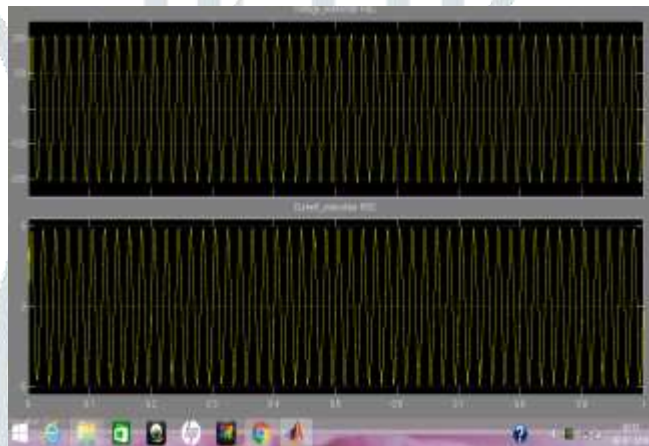


Fig10: INPUT is ($V_{in}=250$) BUCK OUTPUT

CONCLUSION

In this paper, a highly reliable and efficient quasi single-stage single-phase bidirectional buck-boost inverter is proposed. The proposed inverter takes the dual-buck structure at the input dc side and the switching cell structure at the ac output side. It is immune from both short-circuit and open-circuit problems. Therefore, PWM dead-times can be eliminated in the proposed inverter, which results in high quality output voltage waveforms. Moreover, it utilizes high speed power MOSFETs along with externally selected fast recovery diodes, which decrease the switching and conduction losses. Thus, high frequency and high efficiency operation is realized. The operation principle and circuit analysis of the proposed topology are presented in detail.

REFERENCES

- [1] R. R. Errabelli, and P. Mutschler, "Fault-tolerant voltage source inverter for permanent magnet drives," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 500-508, Feb. 2012.
- [2] B. Sahan, S. V. Araujo, C. Noding, and P. Zacharias, "Comparative evaluation of three-phase current source inverters for grid interfacing of distributed and renewable energy systems," IEEE Trans. Power Electron., vol. 26, no. 8, pp. 2304-2318, Aug. 2011.

- [3] S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1928-1940, Sep. 2007.
- [4] S. Rajakaruna and L. Jayawickrama, "Steady-state analysis and designing impedance network of Z-source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 3245-3253, Jul. 2010. [6] J. C. Rosas-Caro, F. Z. Peng, and H. Cha, "Z-source-converter-based energy-recycling zero-voltage electronic load," *IEEE Trans. Ind. Electron.*, vol. 56, no. 12, pp. 4894-4902, Dec. 2009.
- [5] Q. Tran, T. Chun, and J. Ahn, "Algorithms for controlling both the DC boost and AC output voltage of Z-source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2745-2750, Oct. 2007.
- [6] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184-191, Jan. 2011.
- [7] W. Yu, J. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated AC-module application," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253-1260, Apr. 2011.
- [8] P. Sun, C. Liu, J.-S. Lai, and C.-L. Chen, "Grid-tie control of cascade dual-buck inverter with wide-range power flow capability for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1839-1849, Apr. 2012.
- [9] Z. Zhao, M. Xu, Q. Chen, J. Lai, and Y. Cho, "Derivation, Analysis, and Implementation of a Boost-Buck converter-Based High-Efficiency PV Inverter", *IEEE Trans. Power Electron.*, vol.27, No.3, pp.1304-1313, March 2012.
- [10] W. Wu, J. Ji, and F. Blaabjerg, "Aalborg Inverter — A new type of "Buck in Buck, Boost in Boost" Grid-tied Inverter", *IEEE Trans. on Power Electron.*, vol.30, no.9, pp. 4784 - 4793, Sept. 2015.
- [11] R. R. Errabelli, and P. Mutschler, "Fault-tolerant voltage source inverter for permanent magnet drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 500-508, Feb. 2012.
- [12] Ashraf Ali Khan, Honnyong Cha, Hafiz Ahmed, Juyong Kim, and Jinate Cho "A Highly Reliable and High Efficiency Quasi Single-Stage Buck-Boost Inverter.