IMPLEMENTATION OF CASCADED HIGH STEP-UP DC-DC CONVERTER USING THREE-WINDING COUPLED INDUCTOR AND DIODE CAPACITOR TECHNIQUE

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***Abstract* –A cascaded high step up DC-DC converter realized with a tightly coupled three-winding coupled inductor is introduced in this paper. The capacitors are charged in parallel and discharged in series by the coupled inductor. Thus, the proposed converter can achieve high step-up voltage gain with appropriate duty ratio. The voltage stresses on the main switch can be reduced by a passive clamp circuit. Therefore, low resistance $R_{DS(ON)}$ for main switch can be adopted to reduce conduction loss. Compared with existing high step up converters, the proposed converter features that the smaller the turn's ratio is, the larger the conversion gain. So, the name couple inductor reverse is given to represent reverse coupled inductor principle of operation. In addition, diode-capacitor circuit is introduced to not only recycle leakage energy to output, but also further increase the voltage conversion gain. The metal-oxide-semiconductor field-effect transistor (MOSFET) was used for the switching device. The major goal was to improve efficiency. The results of simulations are presented to evaluate the behavior and feasibility of the proposed topology. The operation of proposed system has been found satisfactory.**

***Index Terms* - Cascaded high step-up DC-DC converter, coupled inductor-reverse, Metal-oxide-semiconductor field-effect transistor (MOSFET), Switching losses, reduced turns ratio.**

I.INTRODUCTION

Renewable energy is increasingly becoming a hot research topic, the high step-up converter is also widely employed as an interface in many industry applications, such as fuel cell system, photovoltaic system, electric vehicles, and so on .In general, conventional boost converter can satisfy the requirement in such applications [1]. To achieve a high conversion ratio without operating at large duty cycle, some papers have focused on coupled inductor technique. Typical isolated flyback converter is often adopted for achieving high voltage gain by adjusting the turns ratio [4]. But, the leakage inductance may cause high voltage spikes on the switch and induce energy losses. In order to improve the problems, passive snubber circuit or active clamp circuit can be applied. However, some typical drawbacks exist: The voltage stress of main switch is equal to the output voltage; hence, a high voltage rating switch with high on-resistance should be used, generating high conduction losses [7]. In addition, an extremely high duty ratio will induce large conduction losses on power devices and serious diode reverse recovery problem. Based on the above drawbacks, the conventional boost converter is not suitable for realizing high step-up voltage gain together with high efficiency. Many other techniques have been researched to achieve a high conversion ratio and avoid operating at extreme duty ratio such as switched capacitor technique [7], voltage lift technique [10] and so on. More components, however, are needed for extremely large conversion ratio, resulting in higher cost and complex circuit.

In the proposed strategy, a coupled inductor with a lower voltage rated switch is used for raising the voltage gain (whether the switch is turned on or turned off) [6]. The capacitors are charged in parallel and discharged in series by the coupled inductor, stacking on the output capacitor. Thus, the converter can achieve high step-up voltage gain with appropriate duty cycle [7]. Besides, the voltage spike on the main switch can be clamped. Therefore, low on-state resistance $R_{DS(ON)}$ of the main switch can be adopted to reduce the conduction loss[8]. But, this makes both cost and circuit high and complex. However, under the condition of large voltage conversion gain, the turns ratio must be very high. Using a coupled inductor with a large turn ratio also introduces several problems [12]. For example, the leakage inductance and parasitic capacitance formed by secondary winding of the coupled inductor may cause voltage and current spikes and increase loss and noise that will dramatically degrade the system performance [9]. In this paper, a novel cascaded high step-up dc-dc converter with three-winding coupled inductor and diode-capacitor structures are proposed.

The features of the proposed converter are as follows [1]:

1) The smaller the turn's ratio is, the higher voltage conversion gain.

2) Leakage inductance energy can be recycled to the output,
3) The cascaded structure makes voltage conversion gain higher.

II. BASIC OPERATING PRINCIPLE:

Fig.1 shows the equivalent circuit of the coupled inductor. and Fig. 2 shows circuit structure of the proposed converter, which consists of three-winding coupled inductor, that is modeled as an ideal transformer with a turns ratio (N_2: N_1: N_3), a magnetizing inductance L_M , and leakage inductances L_{k1} , L_{k2} , and L_{k3}, a power switch S, an input inductor L_{in} , a three-winding coupled inductor, diodes D_1 , D_2 , D_3 , D_4 , and D_o , a storage energy capacitor C_1, a clamped capacitor C_c, a multiplier capacitor C_2 , and an output capacitor C_o . Equivalent circuit of the proposed converter is shown in Fig. 2(b).

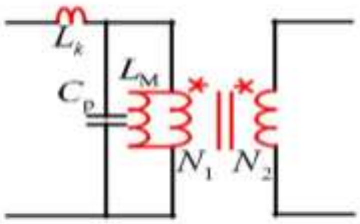

Fig.1.Equivalent circuit of the coupled inductor.

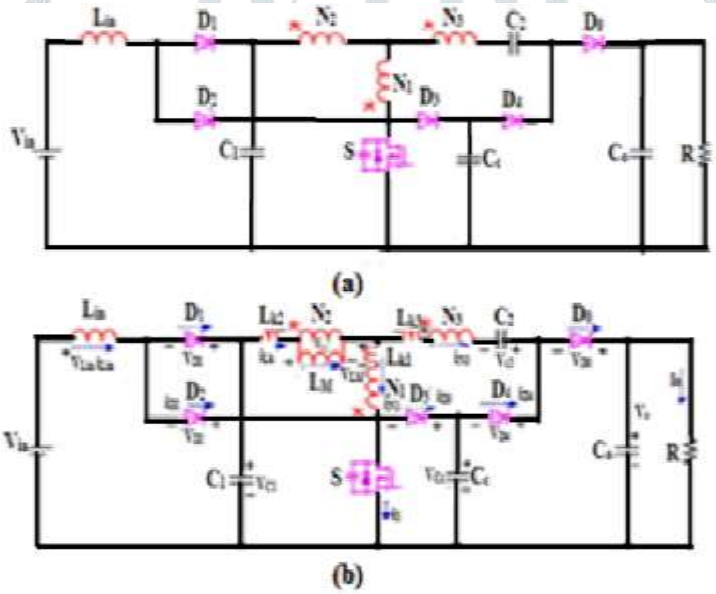

Fig.2 Circuit configuration of the proposed converter.

Fig. 8 shows theoretical waveforms of the proposed converter during one whole switching period. The five operating modes are described as follows.

1) Mode I [t_0, t_1]: During this mode, the switch S is turned ON and starts to conduct. The diodes D_1 and D_o are forward biased and D_2, D_3, and D_4 are reverse biased. The current-flow path is shown in Fig. 3. The input voltage V_{in}, input inductor L_{in}, magnetizing inductance L_M, and multiplier capacitor C_2 are in series to provide energies to the load R and output capacitor C_o .When the current i_{Do} decreases to zero at t_1 , this mode ends.

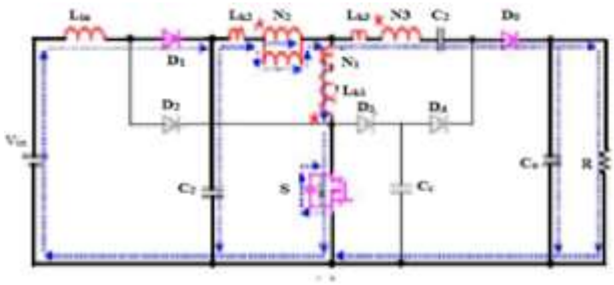

Fig.3

2) Mode II [t_1, t_2]: During this mode, the switch S is turned ON and keeps conducting. The diodes D_2 and D_4 are forward biased and D_1, D_3, and D_o are reverse biased. The input inductor L_{in} is charged by input source $V_{in.}$ The current-flow path is shown in Fig. 4. The windings of coupled inductor N_1 and N_3, C_c are in series to provide energy to the multiplier capacitor C_2. The output capacitor C_o provides energy to the load R. When the switch S is turned OFF at t_2, this mode ends.

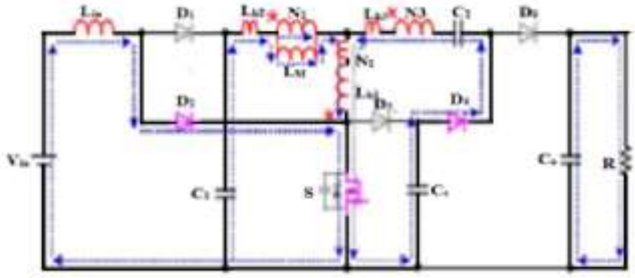

Fig.4

3) Mode III [t_2, t_3]: During this mode, the switch S is turned OFF. The diodes D_2 and D_4 are forward biased and D_1, D_3, and D_o are reverse biased. The energies of leakage inductor L_{k2} and L_{k1}, magnetizing inductance L_M and input inductor L_{in} are released to the parasitic capacitor of switch S. Fig. 5 shows the current-flow path. The output capacitor C_o provides the energy to the load R. When the voltage stress across the parasitic capacitor of switch S is equal to the voltage stress across clamped capacitor C_c at t_3, this mode ends.

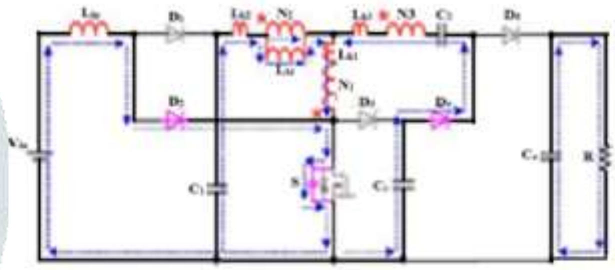

Fig.5

4) Mode IV [t_3, t_4]: During this mode, the switch S is turned OFF. The diodes D_2 and D_4 are reverse biased and D_1, D_3 and D_o are forward biased. The capacitor C_1 is charged by the input source V_{in} and input inductor L_{in} .The clamped capacity or C_c is charged by the energies of leakage inductor L_{k2}, L_{k1},and magnetizing inductance L_M . Fig. 6 shows the current-flow path. The input source V_{in}, input inductor L_{in} , magnetizing inductance L_M , and multiplier capacitor C_2 are in series to provide energies to the load R and output capacitor C_o .When the charging current i_{D3} is equal to zero at t_4 , this mode ends.

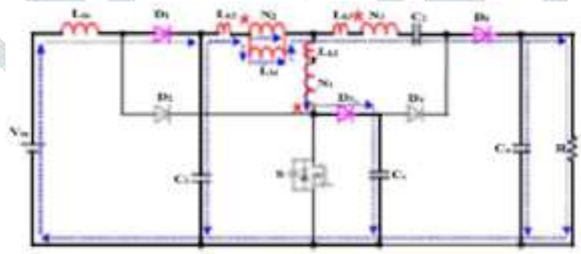

Fig.6

5) Mode V [t_4, t_5]: During this mode also the switch S is OFF. The diodes D_2, D_3, and D_4 are reverse biased and D_1 and D_o are forward biased. The capacitor C_1 is still charged by V_{in} and input inductor L_{in}. Fig. 7 shows the current-flow path. The input voltage V_{in}, input inductor L_{in} , magnetizing inductance L_M , and multiplier capacitor C_2 are in series to provide energies to the load R and output capacitor C_o . When the switch S begins to conduct at t_5, next switching period begins.

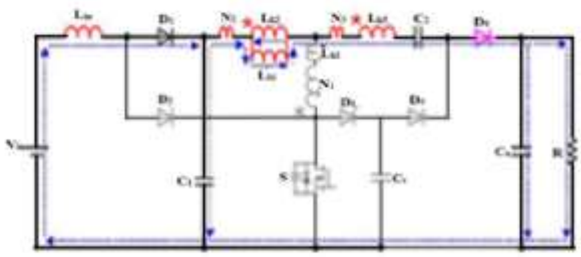

Fig. 7

Advantage:

In the proposed converter, voltage gain formula is different from other converters. The voltage gain formula combines both square feature and inverse ratio feature of the turns ratio. The two features can reduce the duty cycle, winding turns, voltage stress, and coupled inductor volume and so on when operating at the same condition.

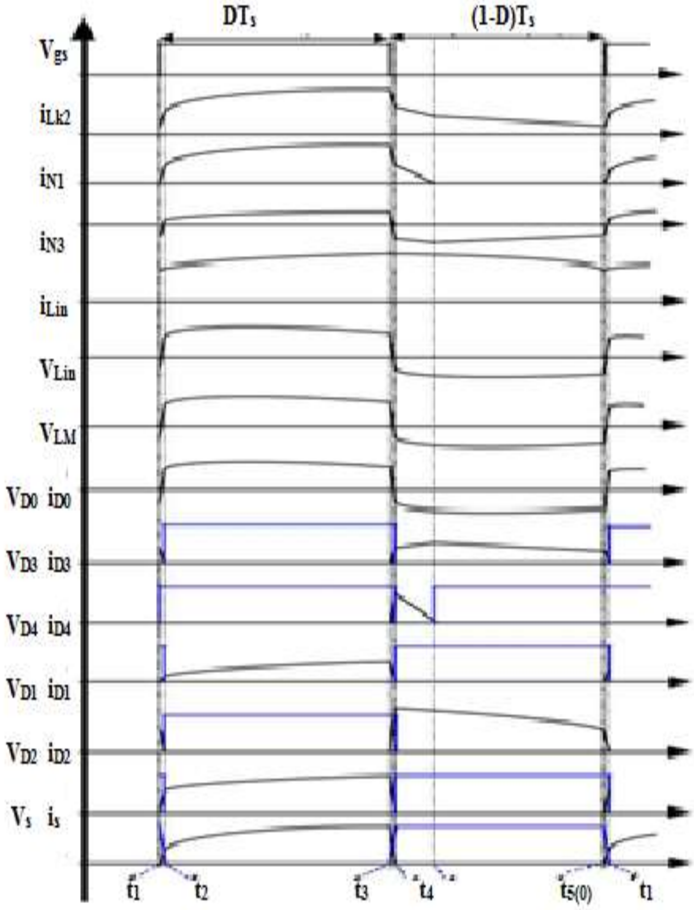

Fig. 8 Theoretical waveforms of proposed converter

III. SIMULATION MODEL AND RESULTS

Simulation was obtained for a cascaded Couple Inductor- Reverse high step up converter using MATLAB/Simulink [R2014a] for input voltage 38v with R- load. Switching sequences have been provided using a pulse generator. Results were obtained for 38v to 380v.

The scheme of the block diagram describing a cascaded couple inductor- reverse high step up dc-dc converter is shown in fig.9 and the simulation parameters for different inputs are given in Table I. Fig.10 shows the simulation results for switching pattern generator. Fig.11 shows the simulation result of a cascaded couple inductor- reverse high step up dc-dc converter. Output of 280v obtained for an input of 28v, Fig. 12 shows the simulation result of a cascaded couple inductor- reverse high step up dc-dc converter. Output of 380v obtained for an input of 38v and Fig. 13 shows the simulation result of a cascaded couple inductor- reverse high step up converter. Output of 480v obtained for an input of 48v.

Table I. Simulation Parameters

Input Voltage=28v.

Parameter	As a High Step-Up Converter
Input Voltage	28v
Resistive Load	1MΩ
Output Voltage	280v

Input Voltage=38v.

Parameter	As a High Step-Up Converter
Input Voltage	38v
Resistive Load	1MΩ
Output Voltage	380v

Input Voltage=48v.

Parameter	As a High Step-Up Converter
Input Voltage	48v
Resistive Load	1MΩ
Output Voltage	480v

Performance comparison between the proposed converter and other converters:

The comparison between the previous results published in [2], [3] are compared with the results of the simulation development. In order to compare, the turns ratio of coupled inductor is the same that is $n_2 = 1.5$ and $n_3 = 1.5$. Table II summarizes the voltage conversion gain, switch stresses, maximum diode stresses, maximum capacitor stresses, and numbers of components.

From the view of numbers of components, the numbers of components in the proposed converter are almost the same as that in [3]. The cost between them is almost equal. The numbers of components in the proposed converter are larger than that in [2]. This increases the cost of the proposed converter. Let us consider V_{in}= 38v, V_o= 380v, D=0.3, n_2=n_3=1.5 in Table II.

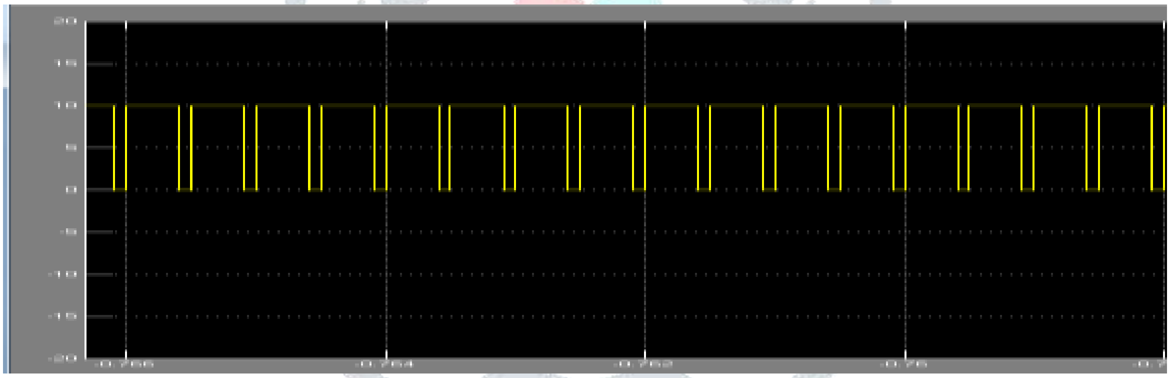

Fig.10 Simulation result for switching pattern generator.

Table III. Proposed Converter

Input Voltage	Output Voltage
28v	280v
38v	380v
48v	480v

From above TABLE III. that is proposed converter for different inputs, we can observe that by using a cascaded high step-up converter we can easily achieve output voltage 10 times more than the input voltage.

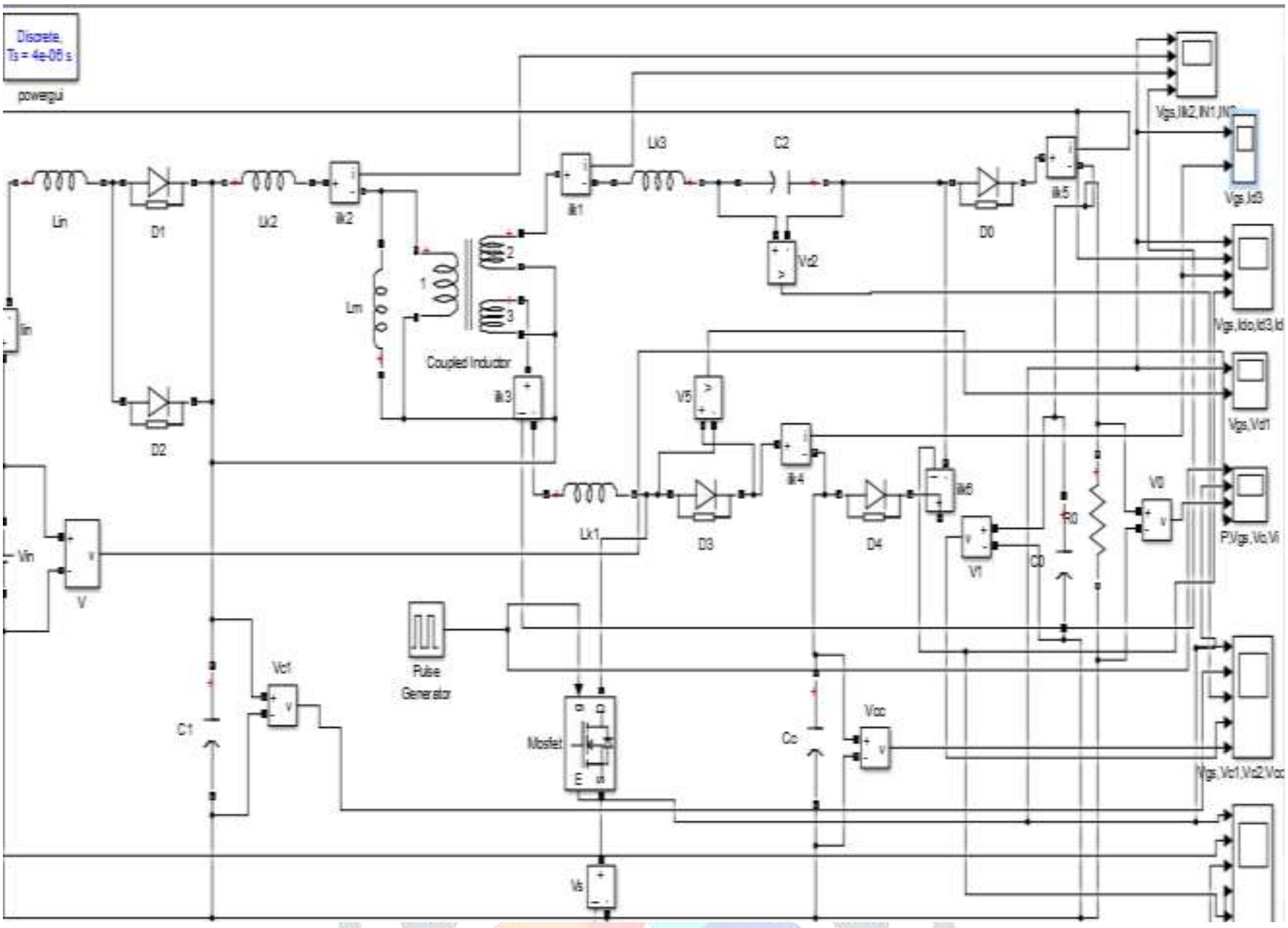

Fig.9. Simulation model of a cascaded couple inductor- reverse high step up dc-dc converter.

Pulse Generator=10V, V_{gs}, Input Voltage=28v. & Output voltage=280v.

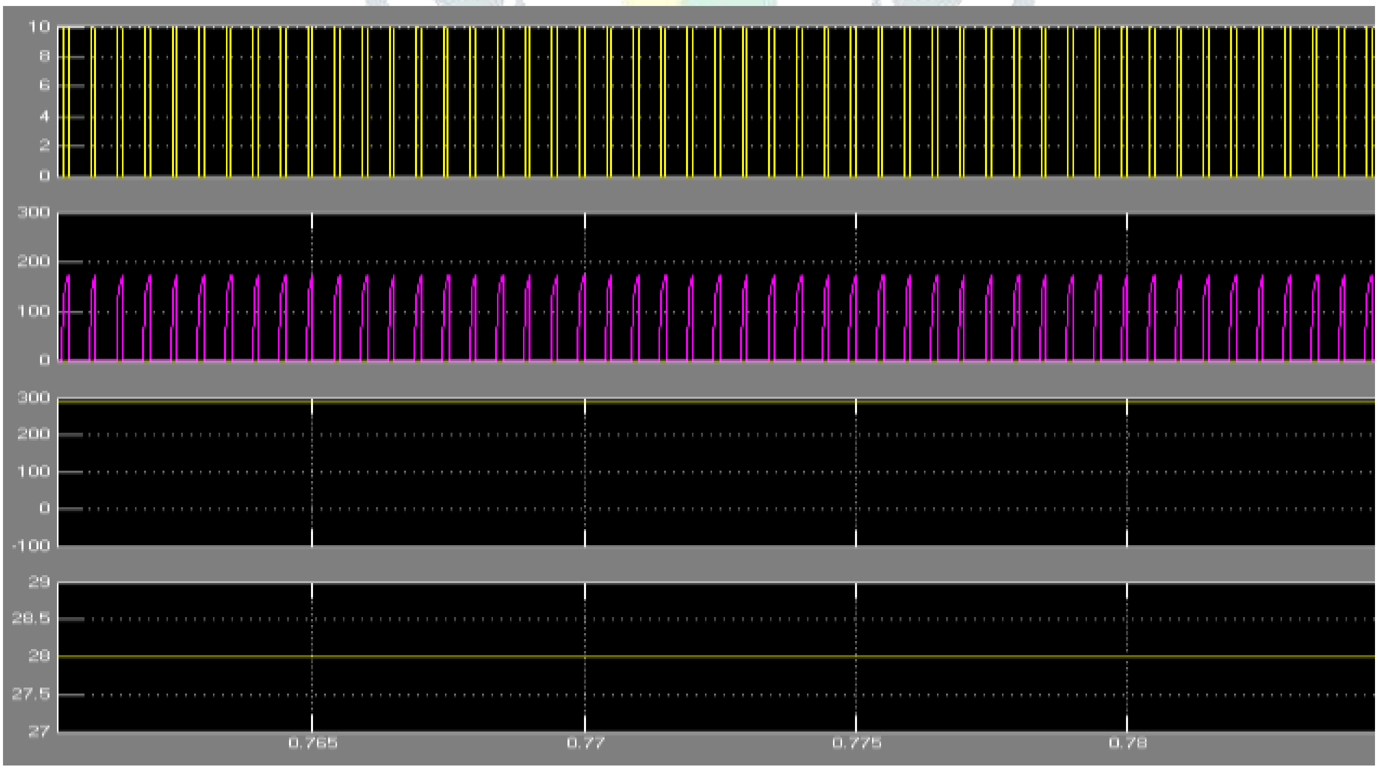

Fig.11 Simulation result of a cascaded couple inductor- reverse high step up dc-dc converter. Output of 280v obtained for an input of 28v.

Pulse Generator, Vgs, Input Voltage=38v. & Output Voltage=380v.

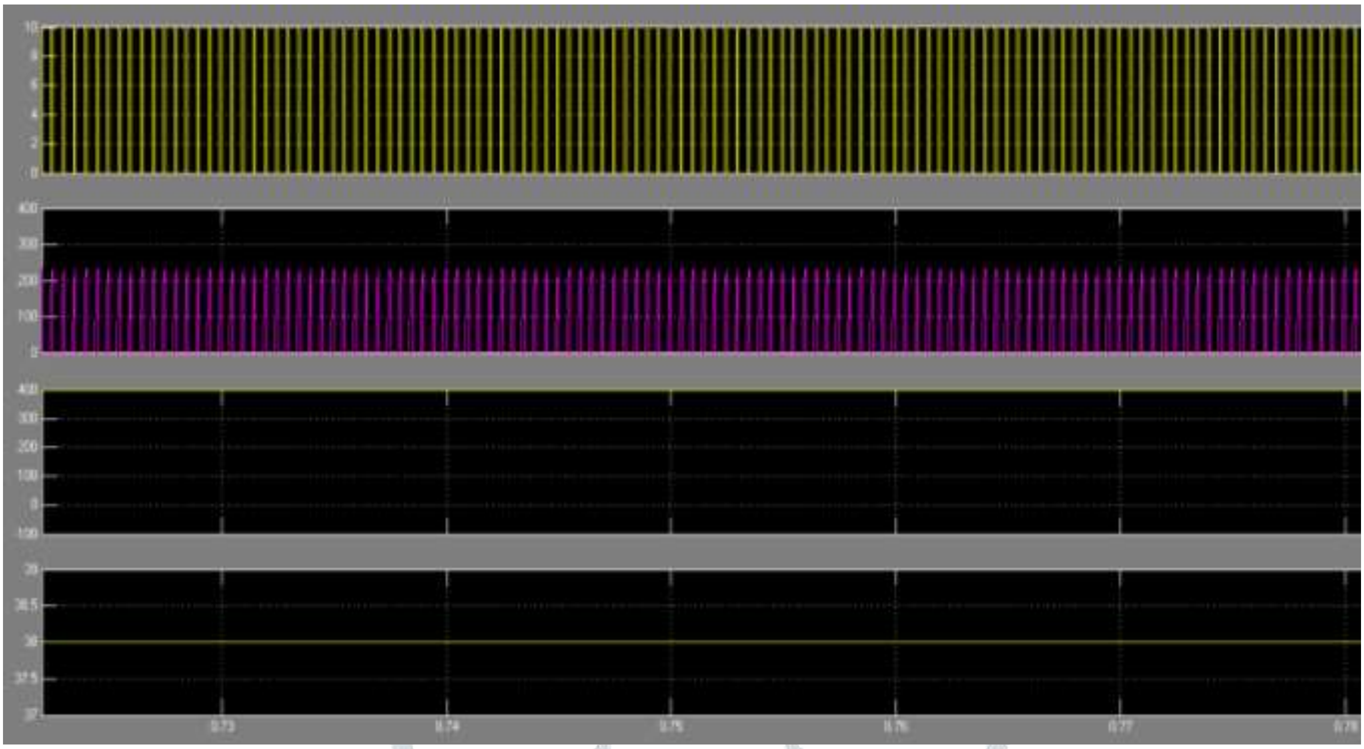

Fig.12 Simulation result of a cascaded couple inductor- reverse high step up dc-dc converter. Output of 380v obtained for an input of 38v.

Pulse Generator=10V, $V_{gs,}$ Input Voltage=48v. & Output Voltage=480v.

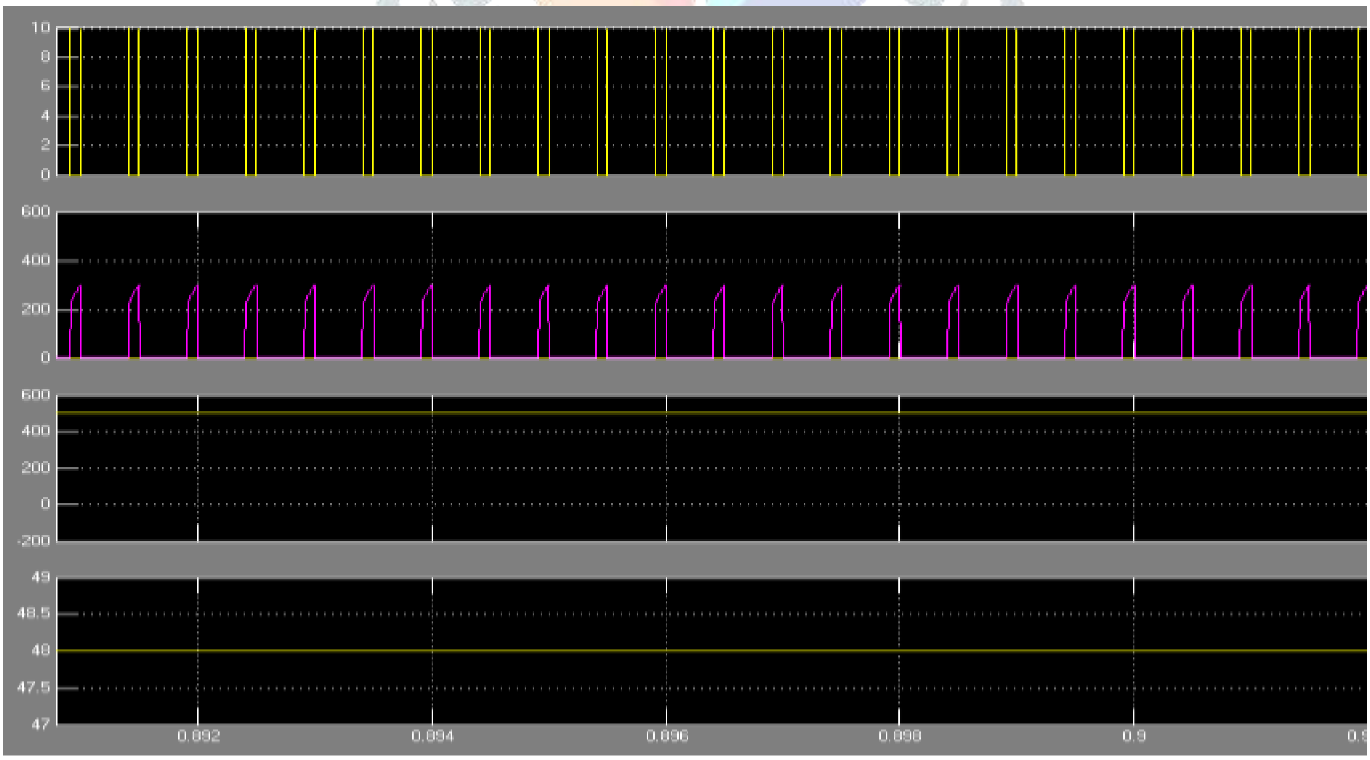

Fig.13 Simulation result of a cascaded couple inductor- reverse high step up dc-dc converter. Output of 480v obtained for an input of 48v.

Table II. Comparison Between Three Winding Coupled Inductor High Step-Up Converters [1]

Topology	Converter[2]	Converter[3]	Proposed converter
Voltage Gain	$(1+n_3)+\frac{1+Dn_2}{(1-D)}$ =4.57	$n_2+\frac{2-D+n_3}{1-D}$ =6.07	$\frac{1}{(1-D)^2}\times\frac{2n_2+n_3-1}{n_2-1}$ =14.28
Voltage stress of active switches	$\frac{V_O}{(1+n_3)(1-D)+1+Dn_2}$ =118.75	$\frac{V_O}{2-D+(1-D)n_2+n_3}$ =89.41	$\frac{(n_2-1)V_o}{2n_2-1+n_3}$ =54.85
Maximum Voltage stress of diodes	$\frac{(1+n_3)V_o}{(1+n_3)(1-D)+1+Dn_2}$ =296.87	$\frac{(1+n_2)V_o}{2-D+(1-D)n_2+n_3}$ =223.52	$\frac{(n_2+n_3)V_o}{2n_2-1+n_3}$ =325.71
Maximum Voltage stress of capacitors	$\frac{(1+n_3)(1-D)V_o}{(1+n_3)(1-D)+1+Dn_2}$ =207.81	$\frac{(1+n_2)(1-D)V_o}{2-D+(1-D)n_2+n_3}$ =156.42	$\frac{(n_2+n_3-D(n_3+1))V_o}{(n_2-1)(2n_2-1+n_3)}$ =488.57
Number of capacitors	3	4	4
Number of diodes	3	4	5

IV. CONCLUSION

In this work, modeling and simulation of a cascaded couple inductor- reverse high step up converter has been developed using MATLAB/simulink [R2014a]. Simulation results were observed to confirm the predicted performance of the proposed topology. The developed simulation results are obtained for resistive load. Because, the resistive load has been used to reduce the complexities of the circuit. Under this loading condition, the converter's performance has been tested for an input voltage 28v, 38v and 48v then we observed an output voltage as 280v, 380v and 480v. The MOSFETs are used as the main power switching device due to its high power applications and fast switching frequency for fine control.

For the high step-up applications, a novel high voltage gain converter is introduced in this work, which combines a quadratic boost converter with three-winding coupled inductor and diode– capacitor techniques. The diode–capacitor circuits not only increase the voltage conversion gain, but also recycled the leakage energy to the output. The three-winding coupled inductor-reverse makes the smaller turn's ratio available implementing the high voltage conversion gain. Due to the cascaded structure, a smaller duty cycle can produce a high conversion gain. The voltage stresses on the power switch and diodes are very low. The efficiency is improved efficiently as compared to the results published in previous papers [2], [3].

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