IMPLEMENTATION OF AREA EFFICIENT CARRY LOOK AHEAD ADDER IN GDI TECHNOLOGY

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Abstract: Adders are used in processors in the arithmetic logic units, to calculate addresses, table indices, and other similar operations. A new area efficient carry look ahead adder including full adder, propagate generate adder, logic AND gates, logic OR gates and XOR gates has been implemented to enhance the performance of arithmetic systems. In this paper, proposed 4 bit carry look ahead adder is implemented in 90 nm,130 nm and 180 nm technology at 0.9 V, 1.2 V and 1.8 V respectively using GDI (Gate Diffusion Input) technique which shows better results in comparison to previous carry look ahead adders. Power consumption and number of transistors are compared and analyzed.

Index Terms: Very large scale integration, Carry Look Ahead Adders, Area

INTRODUCTION

A carry look ahead adder (CLA) or fast adder is a type of adder used in digital logic. A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder(RCA), for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry bit have been calculated to begin calculating its own result and carry bits. The carry look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits of the adder. When two numbers are to be added and if each of them is of N bits than we can add in two ways they are serial and parallel. In serial addition, the LSBs are added first then the carry created are propagated to the next higher bits. In parallel addition, it added in parallel without waiting for carrying and different algorithms are used to compensate for the carry. [2] Today, there are an increasing number of portable applications requiring small areas low power high throughput circuitry [4].

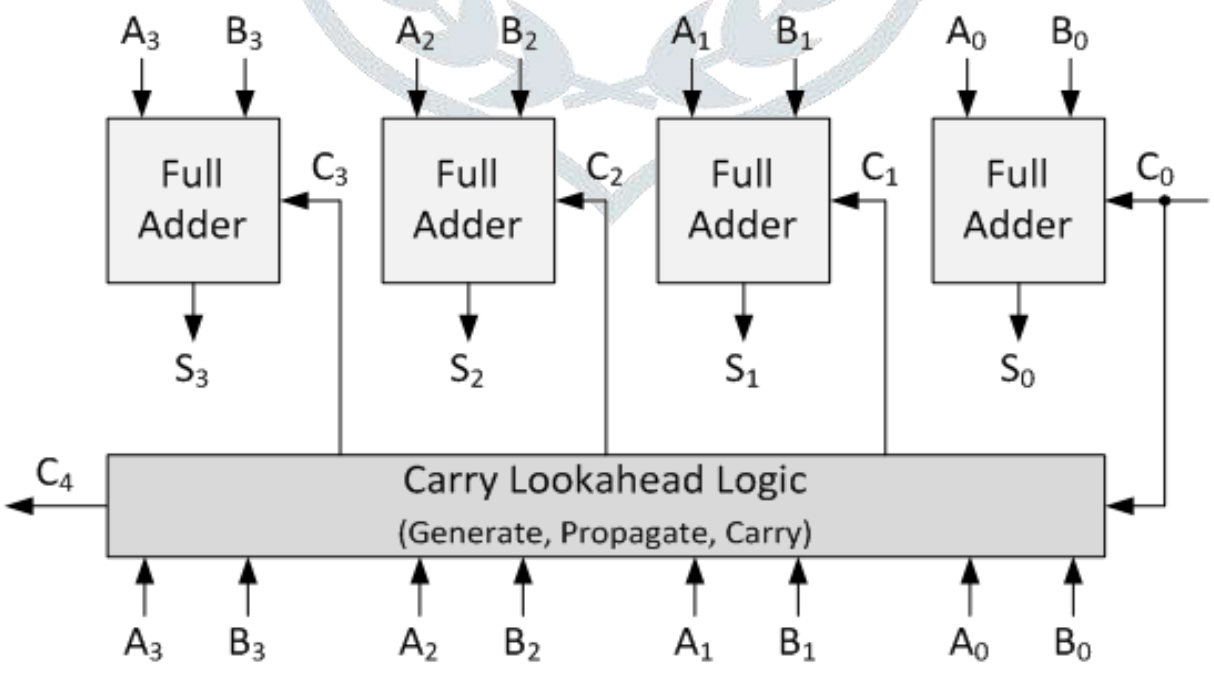

Fig. 1 Carry Look Ahead Adder Realization

Table I Truth Table of Carry Look Ahead Adder

A	B	Ci	SUM	Co	Condition
0	0	0	0	0	No Carry generate
0	0	1	1	0	
0	1	0	1	0	
0	1	1	0	1	No Carry Propagate
1	0	0	1	0	
1	0	1	0	1	
1	1	0	0	1	Carry generate
1	1	1	1	1	

The carry of the *i*th stage C may be expressed as
Ci = Gi + Pi.Ci-1
where
Gi = Ai . Bi (generate signal)
Pi = Ai xor Bi (propagate signal)

The sum Si is generated by
Si = Ai xor Bi xor C i-1 = Pi xor C i-1

For 4 bit carry look ahead adder, the four stages of carry generated signals are
C0= G0 + P0Cin
C1 = G1+ P1G0 +P1P0 Cin
C2 = G2+ P2G1 + P2P1G0 + P2P1P0 Cin
C3 = G3+ P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0 Cin [2]

II. PREVIOUS WORKS

GDI technique

The GDI (Gate Diffusion Input) method is based on the use of a simple cell as shown in Fig. 2. GDI cell contains three inputs G (the common gate input of the nMOS and pMOS transistors), P (input to the outer diffusion node of the pMOS transistor) and N (input to the outer diffusion node of the nMOS transistor).The out node (the common diffusion of both transistors) may be used as input or output port, depending on the circuit. The source of the PMOS in a GDI cell is not connected to VDD while the source of the NMOS in a GDI cell is not connected to GND. This feature gives the GDI cell two extra input pins to use which makes the GDI design more flexible in comparison to usual CMOS design. [3] In this paper half adder has been implemented using GDI technology.

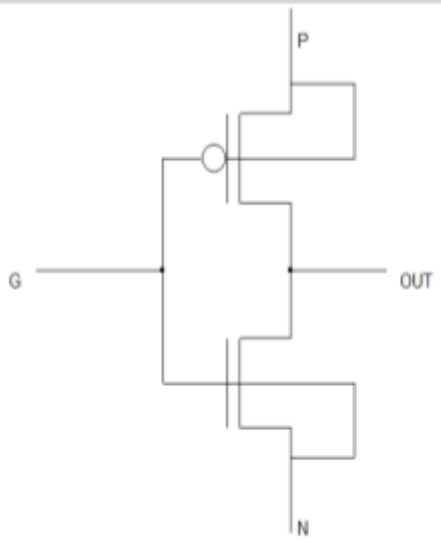

Fig. 2 GDI basic cell [3]

Table II. Various functions of GDI basic cell [8]

N	P	G	OUT	FUNCTION
0	B	A	AbarB	F1

B	1	A	Abar + B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	AbarB + AC	MUX
0	1	A	Abar	NOT
Bbar	B	A	AbarB + ABbar	XOR
B	Bbar	A	AB + AbarBbar	XNOR

PREVIOUS CARRY LOOK AHEAD ADDERS:

(1) MCLA

The MCLA full adder design is shown in Fig.3. This architecture uses the NAND gates instead of the simple AND, OR and NOT gates that are used in the normal adder circuits. [1]

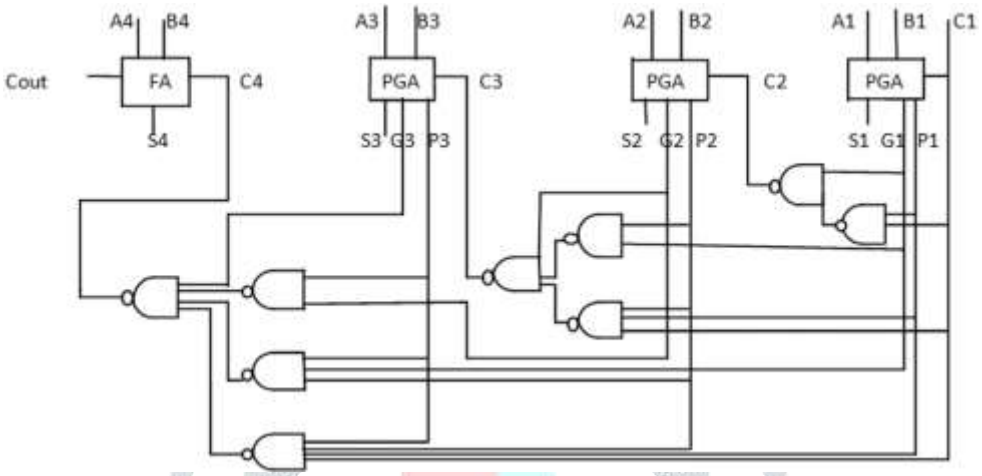

Fig.3 Architecture of MCLA [1]

(2) NCLA

The NCLA full adder design is shown in Fig.4. This architecture uses the AND gates in place of NAND gates. [1]

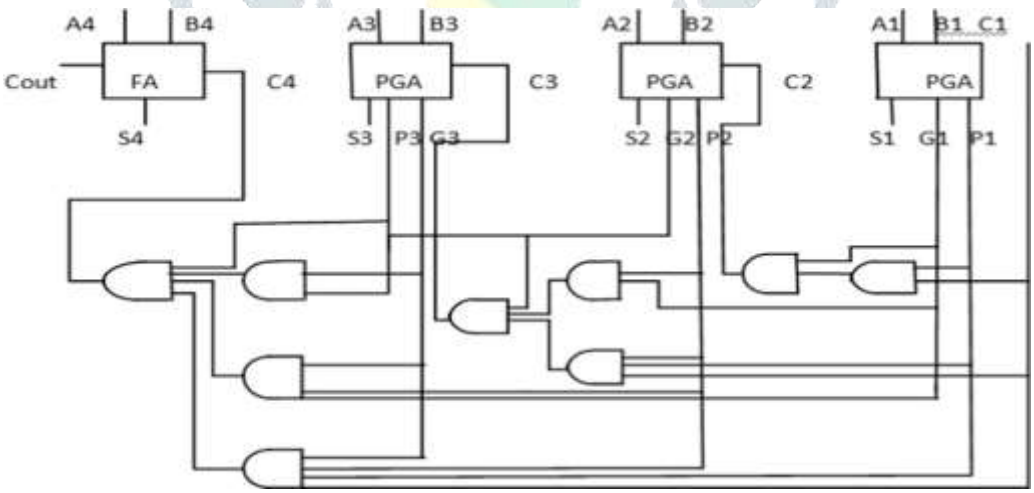

Fig.4 architecture of NCLA [1]

(3) MOCLA

The MOCLA adder architecture shown in Fig. 5 uses the combination of the multiplexer and the OR gates to implement the design. [1]

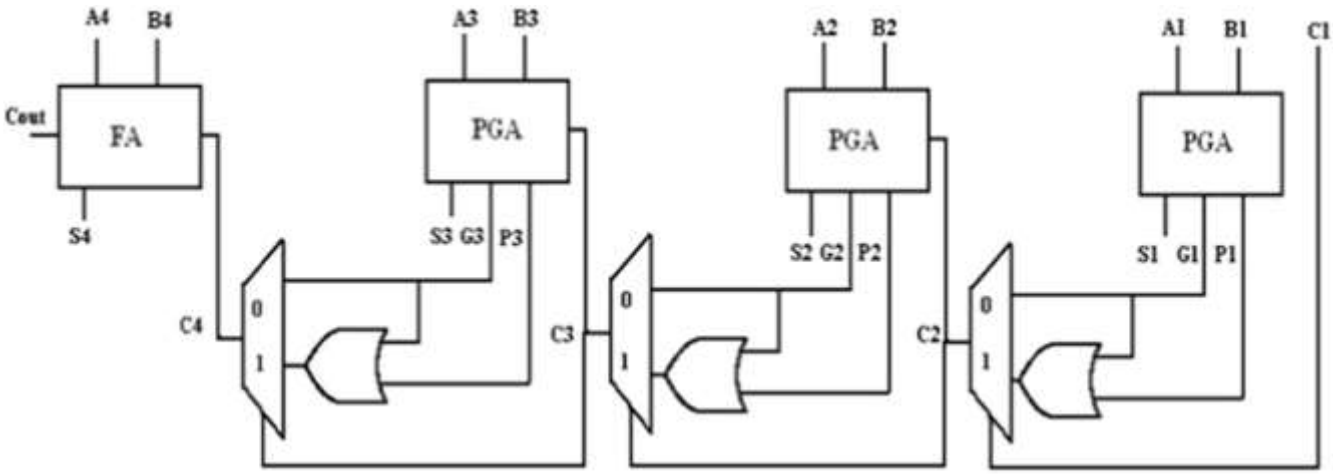

Fig.5 Architecture of MOCLA [1]

III. PROPOSED CIRCUIT

An area efficient carry look ahead adder is implemented using GDI technology which uses 44 transistors. It has been compared with MOCLA presented in paper [1] and shows better results. Proposed carry look ahead adder has been implemented in 90nm, 130 nm and 180 nm technologies at 0.9 V, 1.2 V and 1.8 V respectively. Schematics have been prepared using Tanner tool shown in Fig.6, Fig.7, Fig.8, Fig.9, Fig.10 and Fig.11. All the simulation results have been carried out using TSPICE program. Comparison of power dissipation and number of transistors has been analyzed in Table III and Table IV.

Number of transistors used in circuits defines the area. Power Dissipation is calculated which is the sum of static power, dynamic power and short circuit power dissipated [10] [11] and is calculated by using following equation

Ptotal = Pdynamic + Pshort circuit + Pstatic

Schematic and waveform of Proposed Carry look ahead adder:

Schematic of CLA (90 nm), CLA (130 nm), CLA (180 nm), FA, PGA, XOR, AND, OR gates [5] [6] [7] have been shown in Fig.6, Fig.8, Fig.10, Fig.12, Fig.13, Fig. 14, Fig. 15 and Fig. 16 respectively. Waveforms have been shown in Fig. 7, Fig. 9 and Fig. 11 respectively.

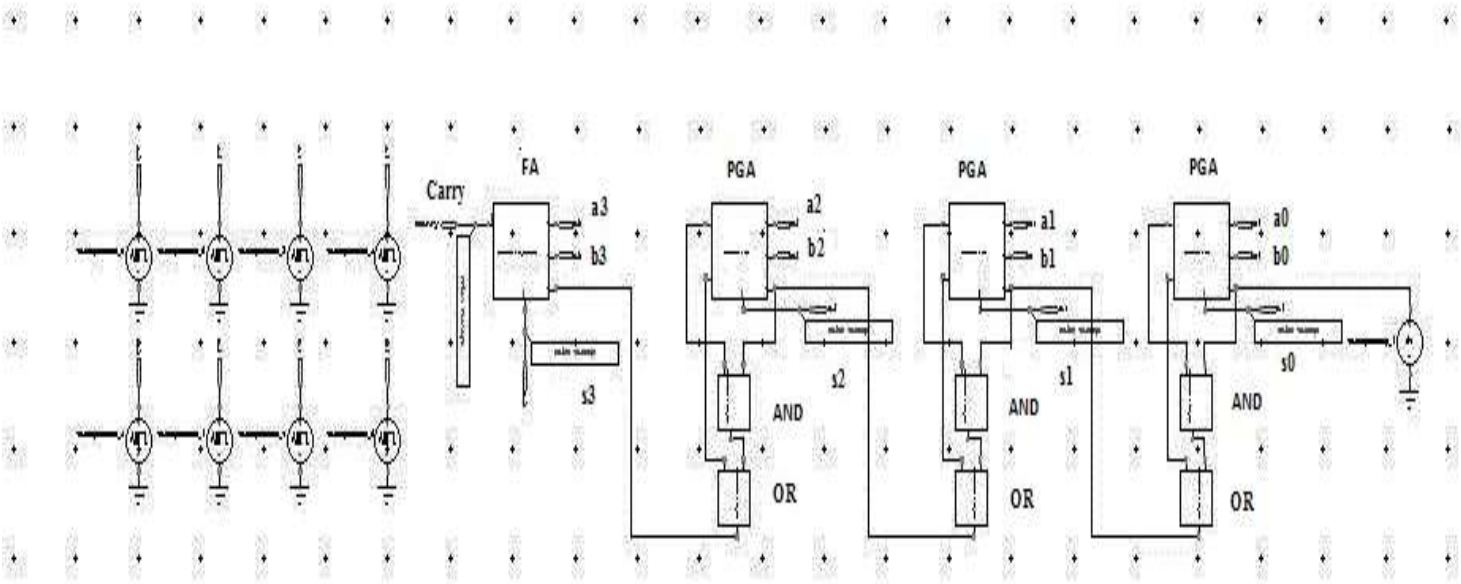

Fig. 6 Schematic of proposed 90 nm carry look ahead adder at 0.9 V

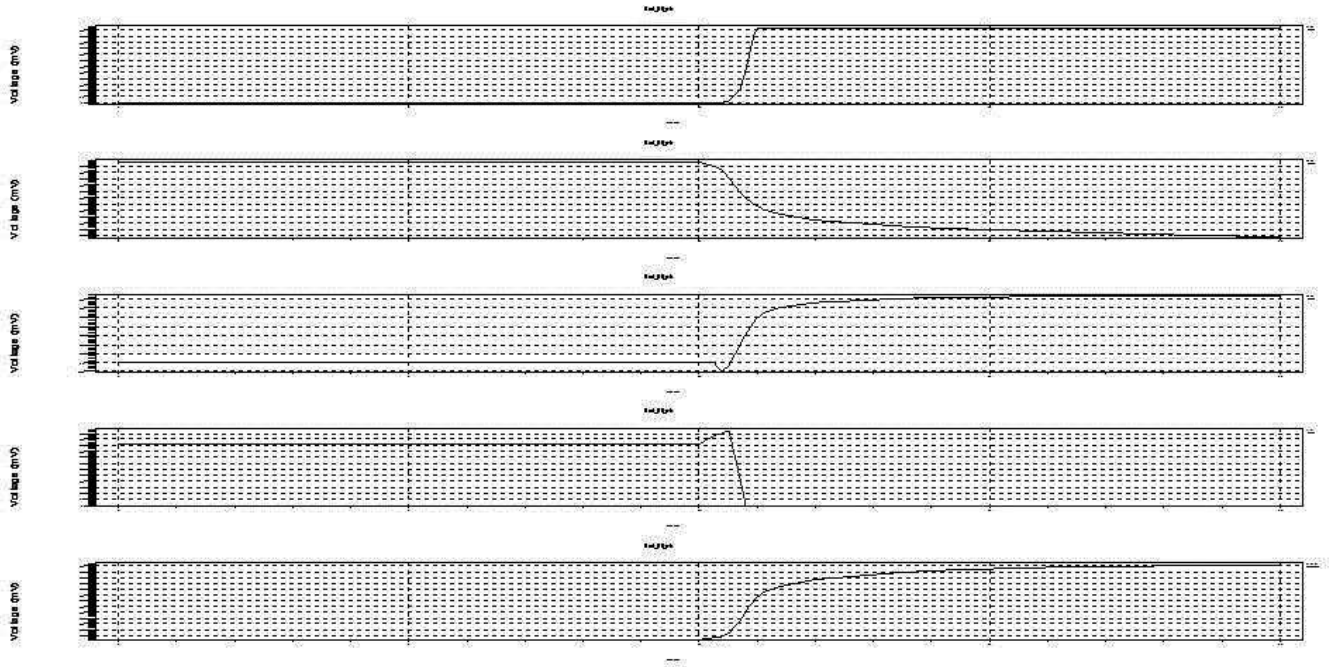

Fig. 7 Waveform of proposed 90 nm carry look ahead adder at 0.9 V

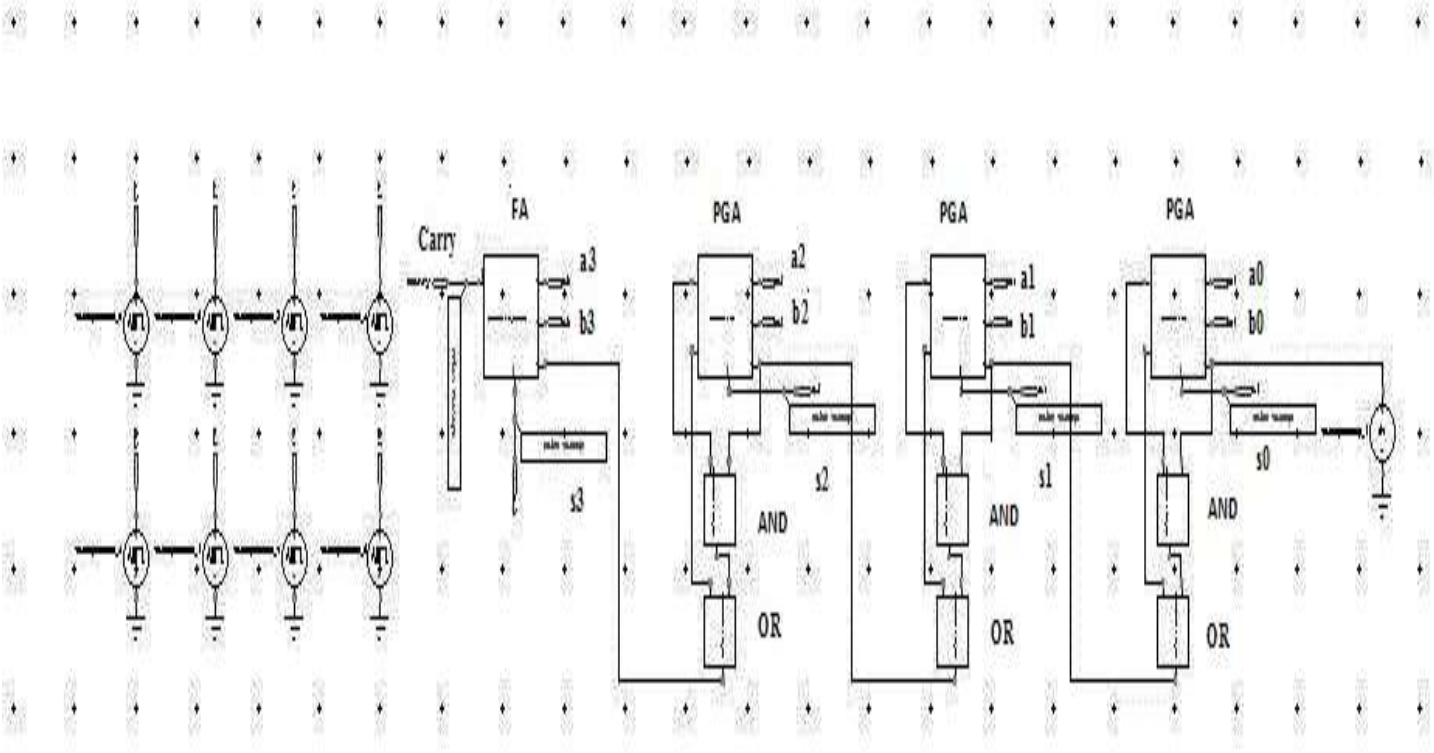

Fig. 8 Schematic of proposed 130 nm carry look ahead adder at 1.2 V

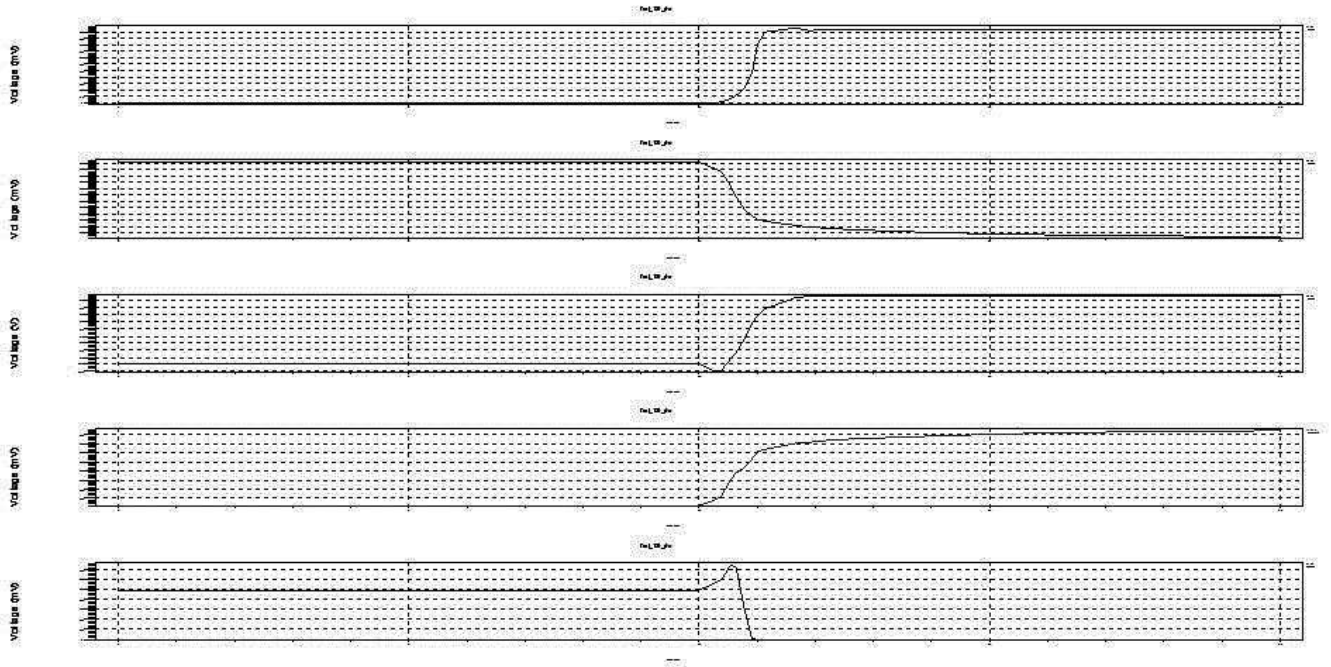

Fig. 9 Waveform of proposed 130 nm carry look ahead adder at 1.2 V

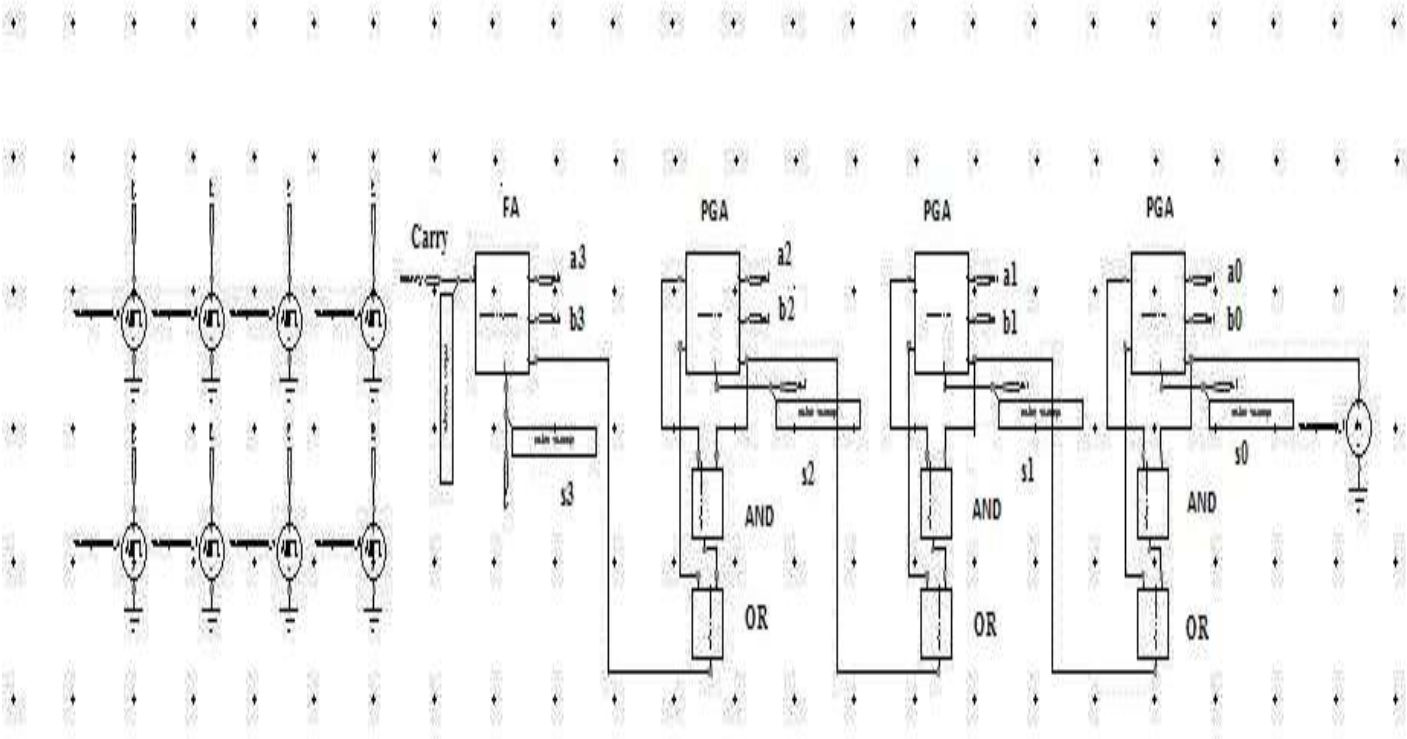

Fig. 10 Schematic of proposed 180 nm carry look ahead adder at 1.8 V

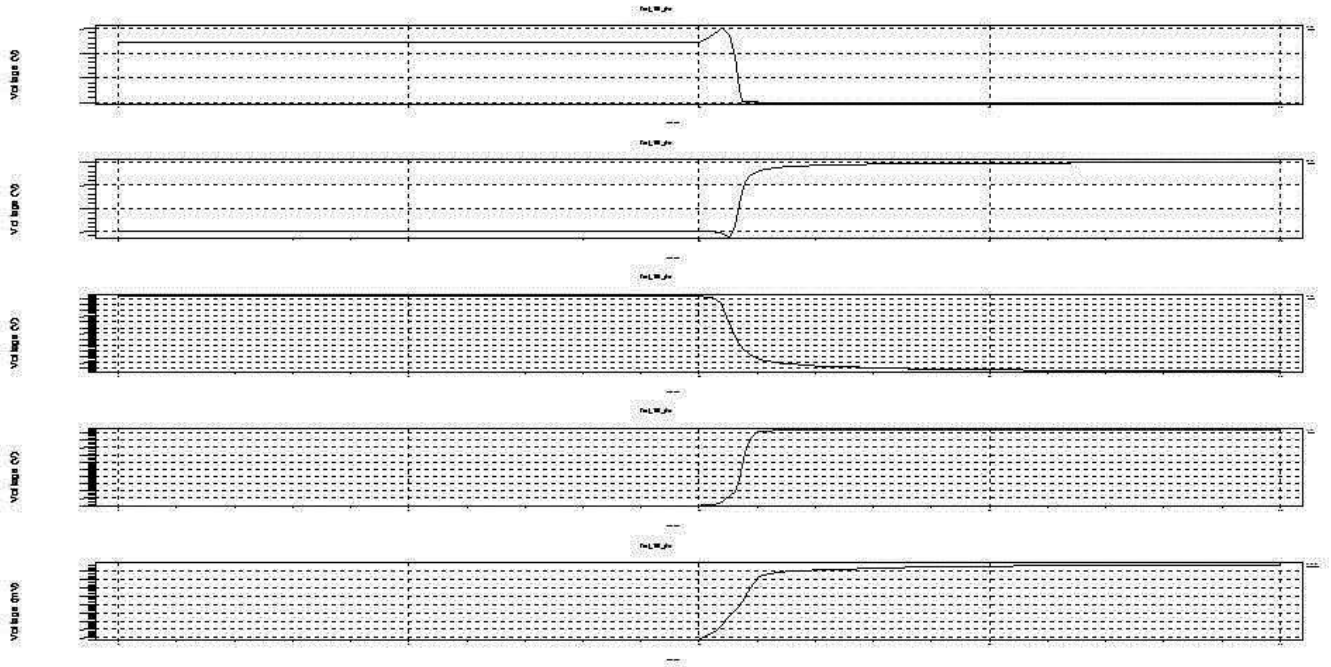

Fig. 11 Waveform of proposed 180 nm carry look ahead adder at 1.8 V

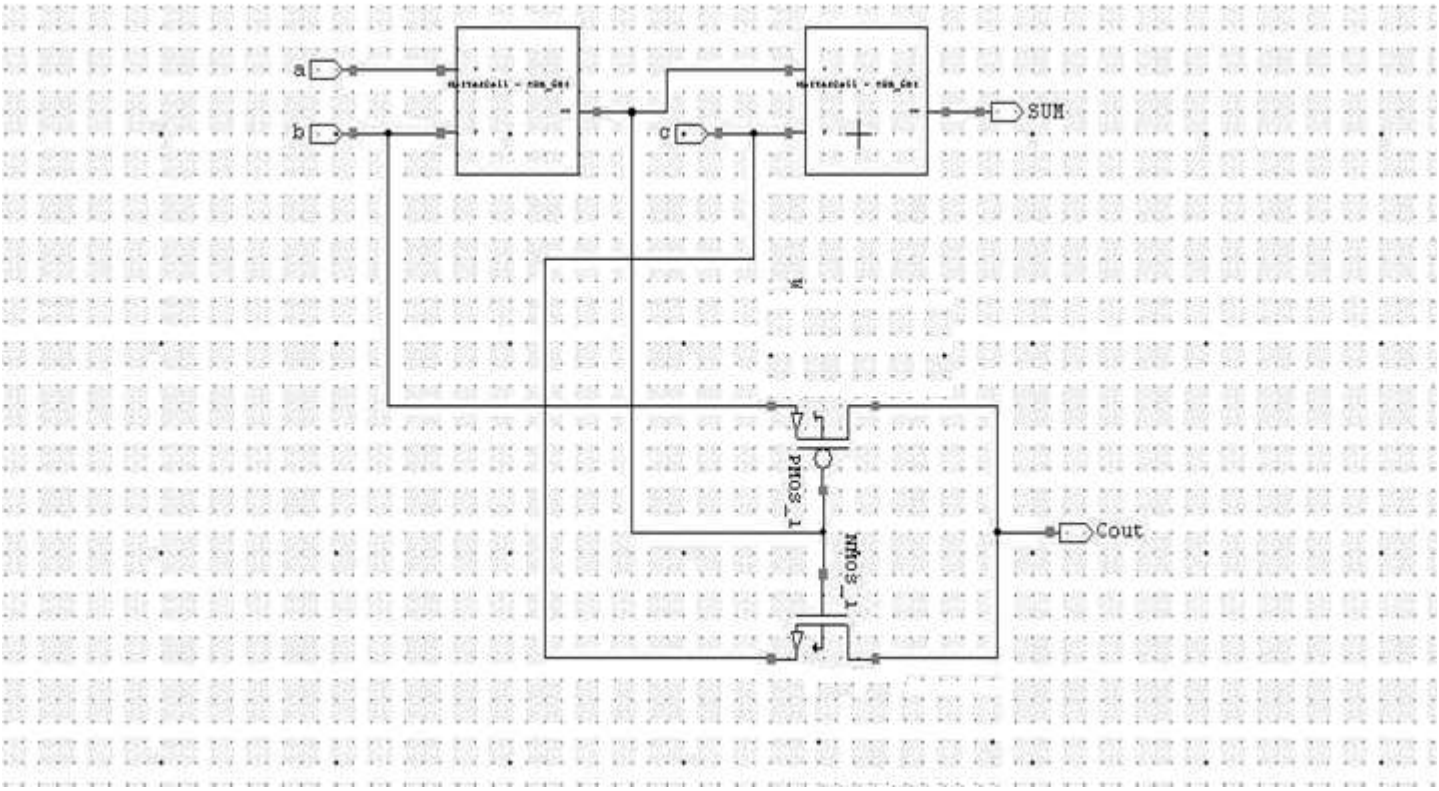

Fig.12 Schematic of Full Adder used

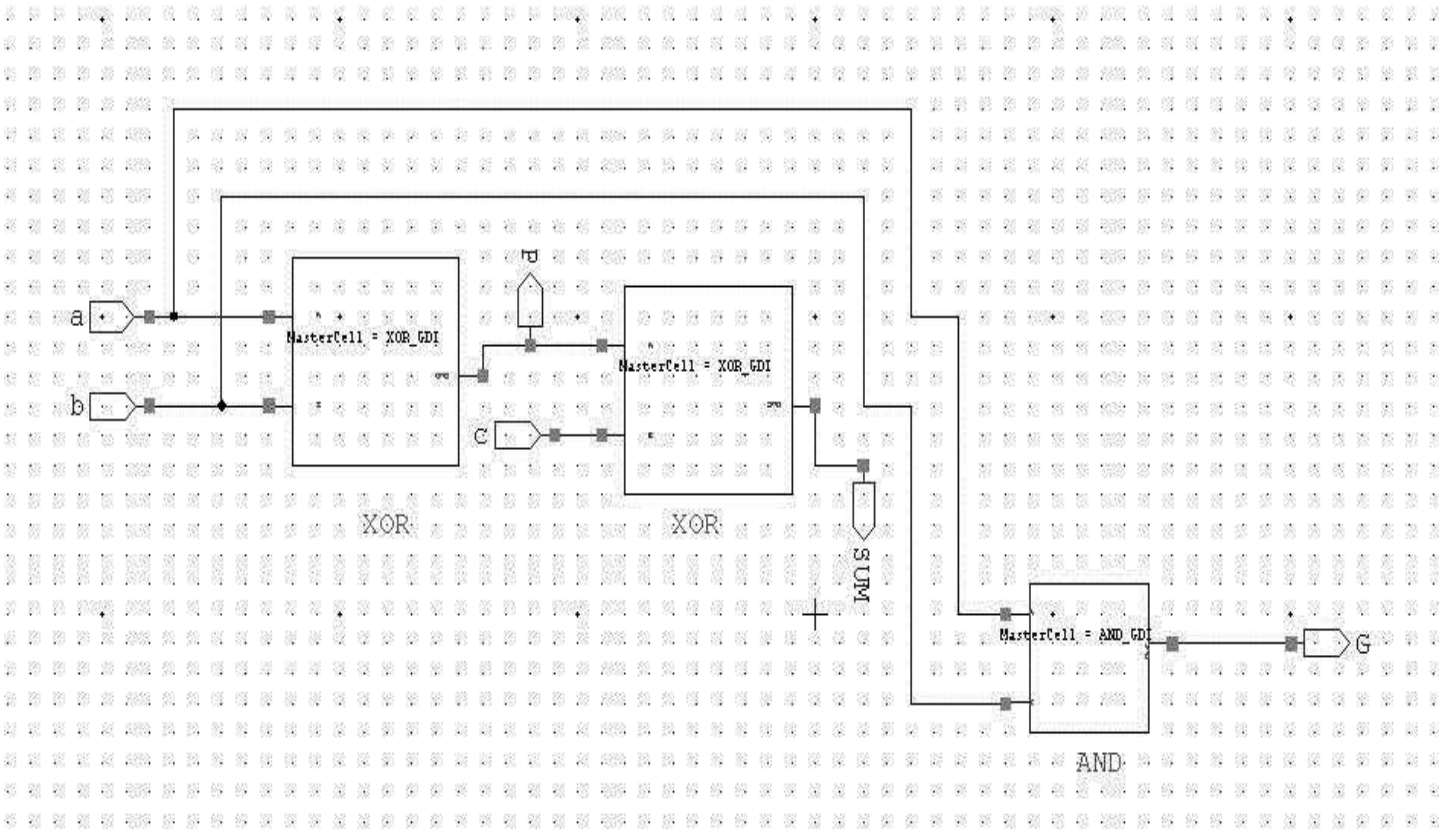

Fig.13 Schematic of PGA or Propagate Generate adder used

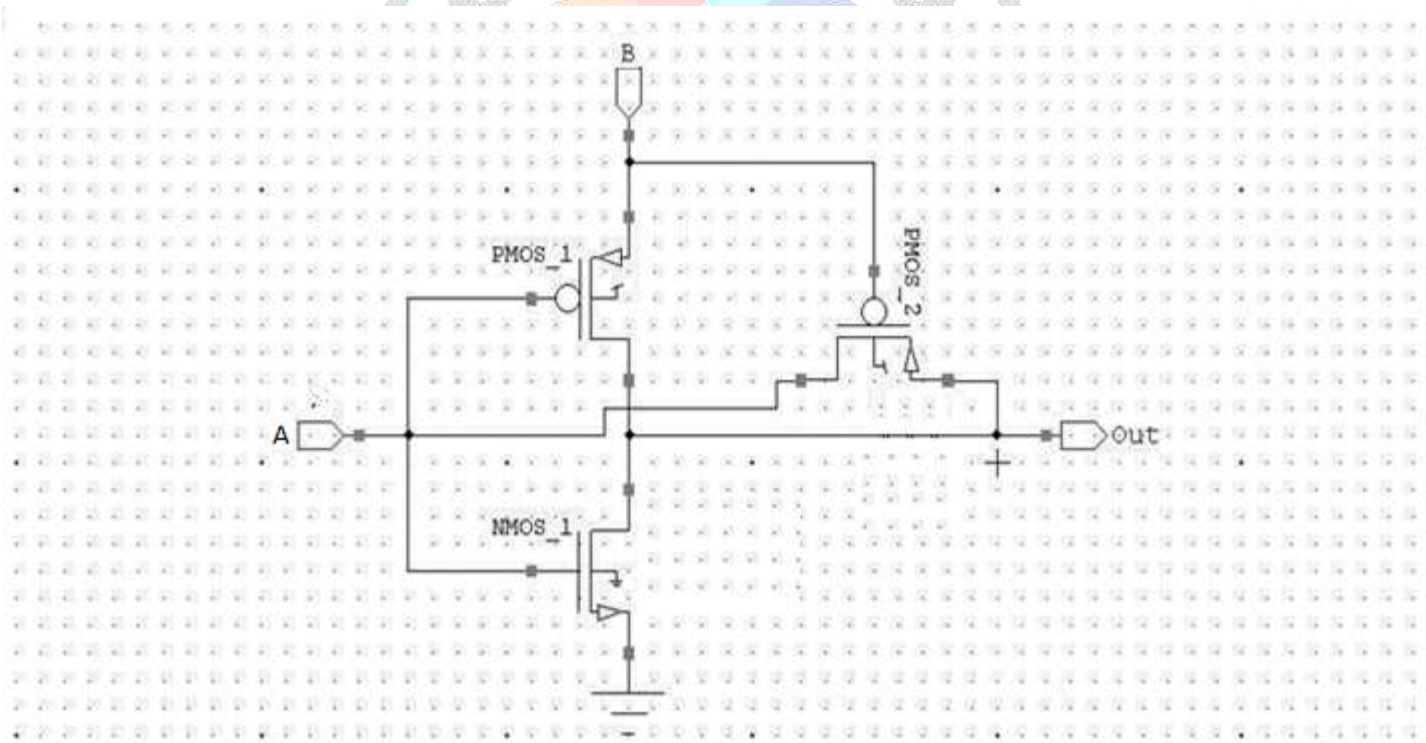

Fig.14 Schematic of XOR gate used

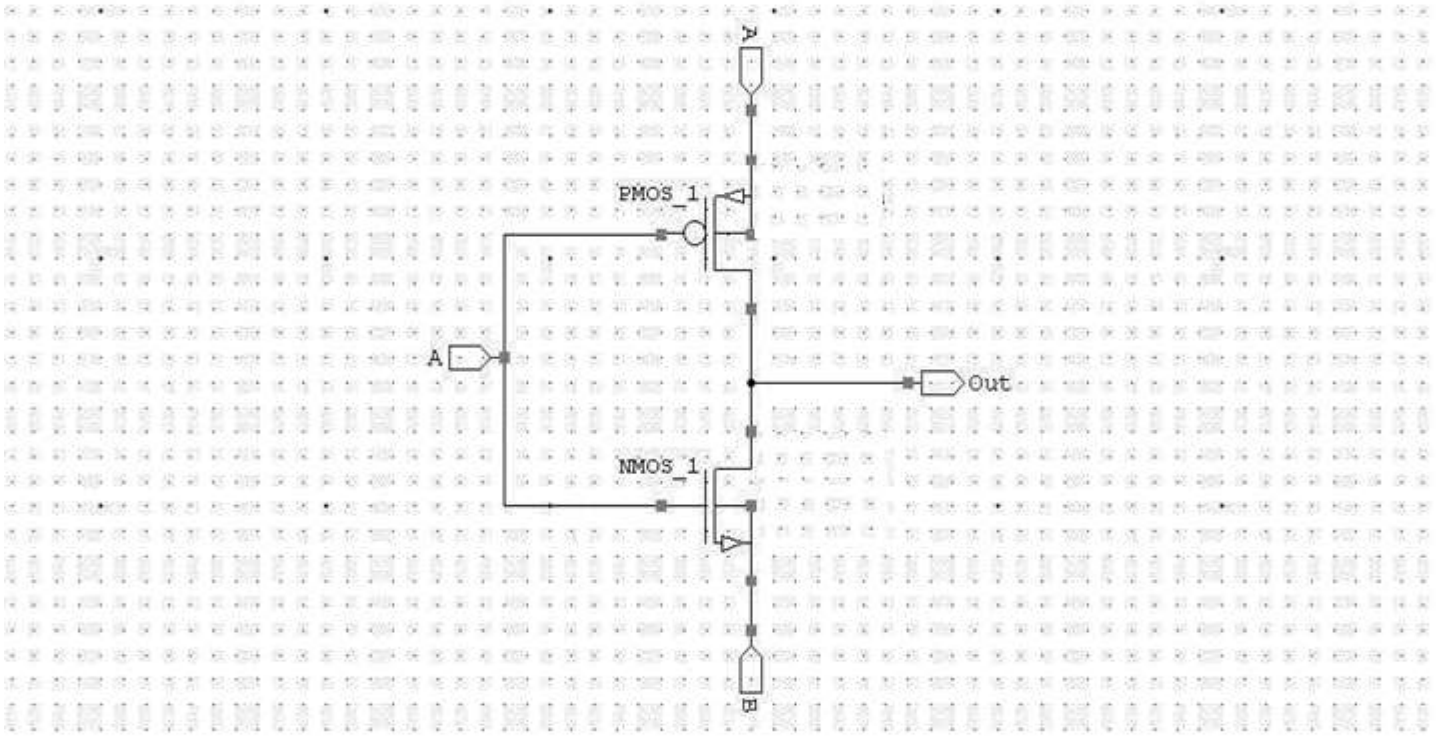

Fig.15 Schematic of AND gate used

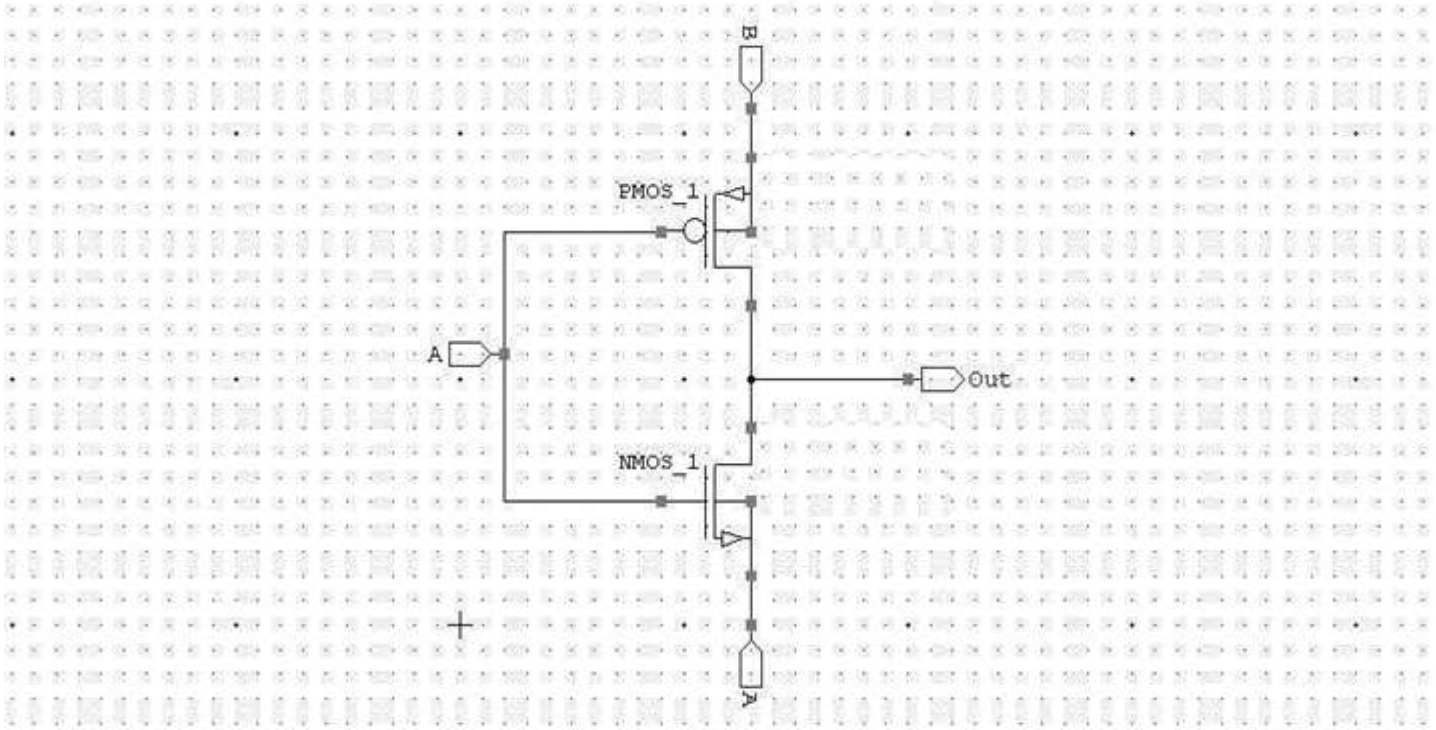

Fig.16 Schematic of OR gate used

IV. SIMULATION RESULTS

Comparison of previous and proposed carry look ahead adder in 90 nm, 130 nm and 180 nm technologies files at 0.9 V, 1.2 V and 1.8 V respectively is shown in the Table III. [9]

Table III. Comparison of MOCLA and Proposed Carry Look Ahead Adders

Parameters	MOCLA (90 nm)	Proposed Carry Look Ahead Adder (90 nm)	Proposed Carry Look Ahead Adder (130 nm)	Proposed Carry Look Ahead Adder (180 nm)
Power (W)	0.1236*10-8	1.2654*10-4	4.6341*10-4	1.0308*10-3
Number of Transistors	52	44	44	44

V. CONCLUSION

In this paper an area efficient carry look ahead adder is proposed in 90 nm, 130 nm and 180 nm technology at 0.9 V, 1.2 V and 1.8V respectively. The design is implemented using 44 transistors which reduce the area occupied by the earlier carry look ahead adder circuits. The power consumption is also reduced in all the technologies. On comparing proposed carry look ahead adders and MOCLA we conclude proposed carry look ahead adder has lowest area and lowest power consumption in comparison to previous carry look ahead adders.

VI. ACKNOWLEDGMENT

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VII. REFERENCES

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