DESIGN OF ADVANCED SEPIC CONVERTER FOR SOLAR POWER SYSTEM

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***Abstract:** This paper presents improved SEPIC DC-DC converter for photovoltaic applications. The modified SEPIC Converter contains clamping circuit to reduce leakage energy. Magnetic coupled inductor is implemented to reduce input current harmonics and improve power factor. Proposed converter has high static gain, high efficiency, high step-up voltage, optimized volume, weight and cost. Operation of SEPIC converter is analyzed using Simulink.*

Index Terms - Photovoltaic Technology, SEPIC Converter, Active clamping circuit.

I. INTRODUCTION

In the present scenario, due to ecological issues and energy demand with reduction in fossil fuels, an alternative sustainable power source demand is increasing. To take care of the energy demand, photovoltaic and wind turbine system are attracting attention.

The DC-DC converters are used to step-up/step-down the voltage from source. Buck, Boost, Buck-boost are basic DC-DC converters. By Performance the buck converter is more efficient [1] and boost converter is more lossy [2]. To overcome this problem three switch high-voltage converter (SEPIC) is used [3]. To provide electrical separation between input and output side flyback converter is used with boost converter [4]-[6]. Thereafter to remove transformer from circuit, switched capacitors and inductors are used [7]. SEPIC with flyback converter provide high step-up voltage but involves more switching losses. The magnetic coupling is introduced to replace the transformer in circuit. In this paper design of modified SEPIC converter by considering step-up of voltage is explained briefly.

II. METHODOLOGY

The proposed system with magnetic coupling can operate with a static gain double the classical boost converter for a high duty-cycle operation. A simple solution to increase the static gain without increasing the duty-cycle and the switch voltage is to divide the inductor into two parts. The inductor operation is similar to a buck-boost inductor and a secondary winding can increase the output voltage by the inductor windings turns ratio (n). The energy stored in the leakage inductance, due to the output diode reverse recovery current, results in high reverse voltage at the diode .This overvoltage is not easily controlled with classical snubbers or dissipative clamping. A simple solution for this problem is the inclusion of a voltage multiplier at the secondary side as presented in this paper. The voltage across the output diode is reduced to a value lower than the output voltage and the energy stored in the leakage inductance is transferred to the output.

III. PROPOSED CONVERTER CIRCUIT

The basic SEPIC converter is shown in figure.1. In SEPIC converter, step-up voltage gain is an important performance parameter for large input and output voltage ranges. However, the switching losses is more. The modification of SEPIC converter is done by adding few more components to the basic circuit and is shown in figure.2

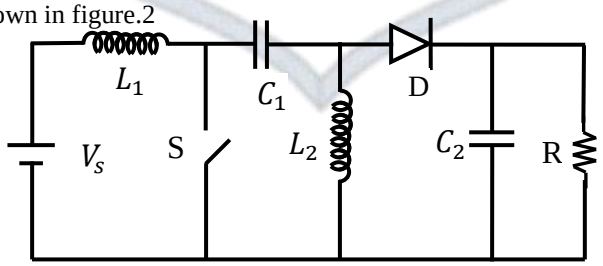

Figure 1. Basic SEPIC Converter

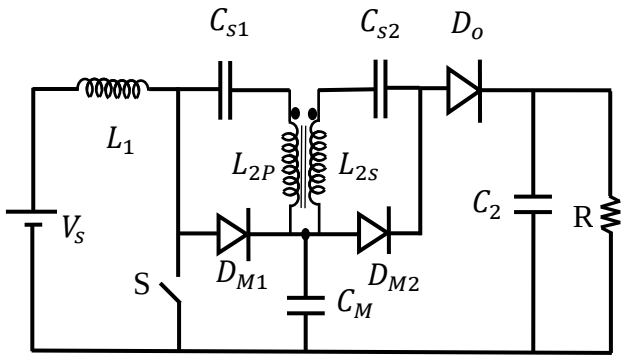

Figure 2. Modified SEPIC Converter

The circuit operation of modified SEPIC converter is distributed into 5 stages

Stage 1: Time duration (t_0-t_1)
As switch is turned on, inductor L_1 stores energy and secondary side winding L_{2s} releases energy and charge capacitor C_{s2}. At same time C_{s1} is charged in the opposite direction. With the output diode blocked, the diode voltage will be $(V_0 - V_{CM})$.

Stage 2: Time duration (t_1-t_2)
At the instant t_1, the charging of capacitor C_{s2} will be completed. Therefore diode D_{M2} goes blocked. At the instant t_2, when the switch is turned OFF, the inductors L_1 and L_2 store energy from input dc source.

Stage 3: Time duration (t_2-t_3)
The energy stored in the L_1 inductor is transferred to the C_M capacitor. Now L_{2p} is charged from capacitor C_{s1}. Energy is transferred to the output through the capacitors C_{s1},C_{s2}, inductor L_2 and output diode D_0.

Stage 4: Time duration (t_3-t_4)
At the instant t_3, the energy transferred to the capacitor C_M will be completed and D_{M1} will be blocked. Energy will be transferred to the output until time t_4, at which the power switch is turned ON. At the same time the Current through D_0 decreases.

Stage 5: Time duration $(t_4 - t_5)$
When the output diode is blocked, the converter returns to the first stage.
The main theoretical waveforms of the modified SEPIC converter with magnetic coupling is shown in Figure.3.

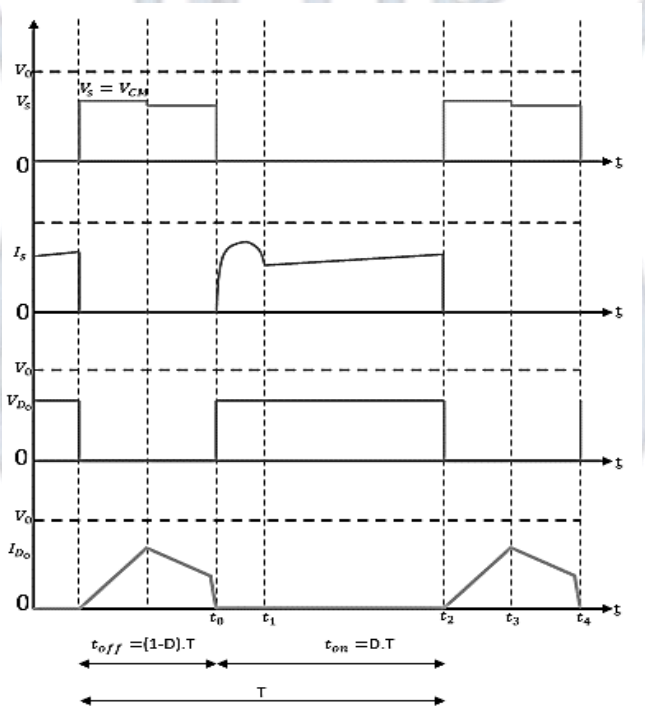

Figure 3. Theoretical waveforms

IV. DESIGN AND CALCULATION

The main equations considered to design advanced SEPIC converter with magnetic coupling are illustrated.

Inductor winding turns ratio, $n = 2.6$
Power output, $P_0 = 100\ W$
Output voltage, $V_0 = 240\ V$
Input Voltage, $V_i = 12\ V$
Switching frequency = 24 kHz

A. Switch Duty Cycle: $D = 1 - \frac{V_i}{V_0}(n+1)$

$D = 1 - \frac{12}{240}(1 + 2.6) = 0.82$

B. Switch voltage and diode voltages:

The switch voltage and voltage across the diode D_{M1} are equal.

$$V_s = V_{D_{M1}} = \frac{V_i}{1-D} = \frac{12}{1-0.82} = 66.67\ V$$

The voltage across the diode D_{M2} and output diode voltage are equal.

$$V_s = V_{D_{M1}} = \frac{V_i}{1-D} = \frac{12}{1-0.82} = 66.67\ V$$

C. L_1 and L_2 Inductance:

The current ripple (Δi_c) of both inductor L_1 and L_{2p} are assumed as 5A

$$L_1 = L_{2p} = \frac{V_i \,.\, D}{\Delta i_c \,.\, f} = \frac{12\times0.82}{5\times24\times10^3} = 82\mu H$$

Secondary winding L_{2s} of inductor L_2 is calculated by considering winding turns ratio

$$L_{2s} = n^2 . L_{2p} = 2.6^2 \times 82 \times 10^{-6}$$
$$L_{2s} = 554.32\mu H$$

D. Capacitor C_s and C_M:

Both capacitor C_s and C_M are having same Voltage ripple ΔV_c.

$$\Delta V_c = \left(\frac{V_i}{1-D}\right).\left(\frac{V_i}{P_0}\right) = \left(\frac{12}{1-0.82}\right)\left(\frac{12}{100}\right)$$

$$\Delta V_c = 6.667\ V$$

$$C_{s1} = C_{s2} = C_M = \frac{I_0 . n}{\Delta V_c . f}$$

$$C_{s1} = C_{s2} = C_M = \frac{0.4167 \times 2.6}{6.667 \times 24 \times 10^3}$$

$$C_{s1} = C_{s2} = C_M = 6.77\mu F$$

Output capacitor or filter capacitor is designed by considering duty cycle.

$$C_0 = \frac{I_0 . D}{\Delta V_c . f} = \frac{0.4167 \times 0.82}{6.667 \times 24 \times 10^3}$$

$$C_0 = 5.932\mu F$$

E. Semiconductor current:

Current through all diodes equal to the current at the output terminal.

$$I_{D_0} = I_{D_{M1}} = I_{D_{M2}} = I_0 = \frac{P_0}{V_0}$$

$$I_0 = \frac{100}{240} = 0.4167\ A$$

F. Resistive load:

$$R = \frac{V_0}{I_0} = \frac{240}{0.4167} = 576\Omega$$

I. SIMULATION AND RESULTS

The magnetic coupled topology shown below is for an input voltage of 12 V and output voltage of 240. Proposed converter has a static gain of 20.

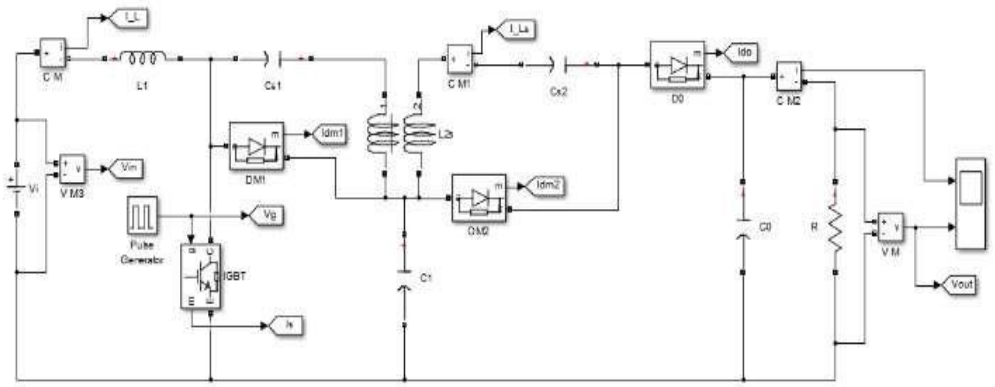

Figure 4. Simulation of converter with magnetic coupling

Converter output voltage and current waveform are shown in below figure.5

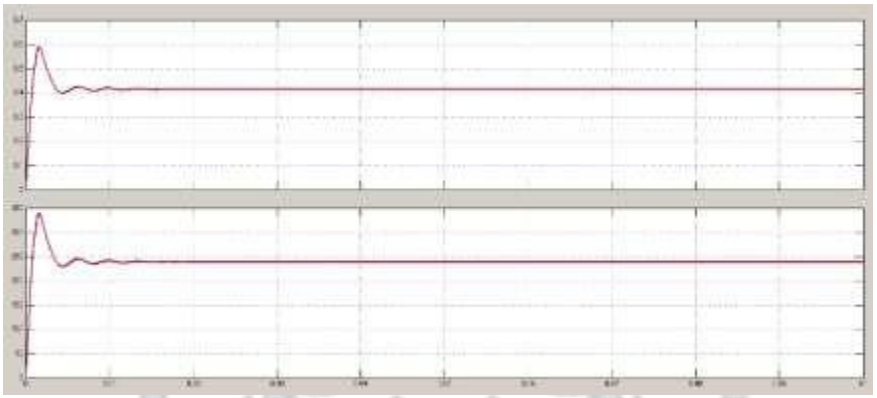

Fig. 5. Converter output current and voltage waveforms

The voltage and current waveforms of individual components in SEPIC converter are shown below.

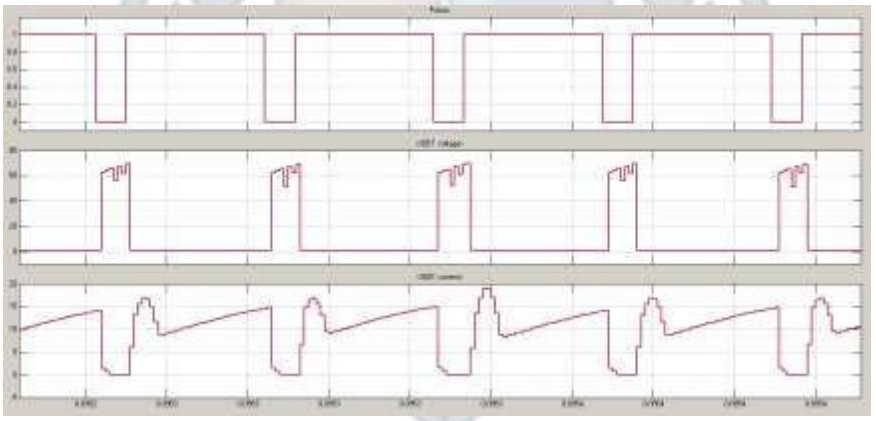

Fig. 6. Current and voltage waveforms of switch IGBT

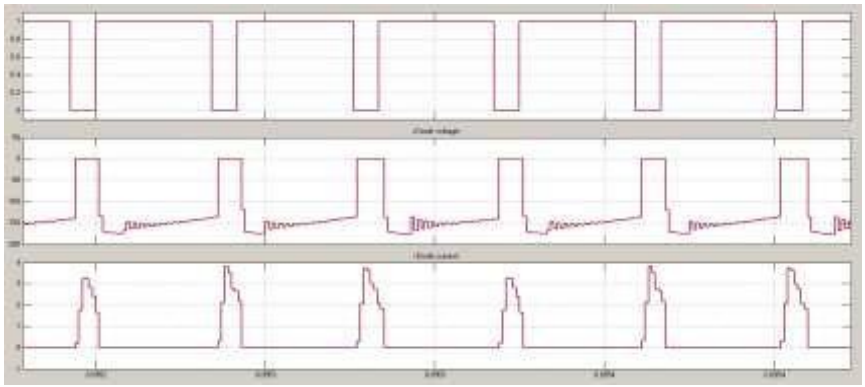

Fig. 7. Current and voltage waveform of diode

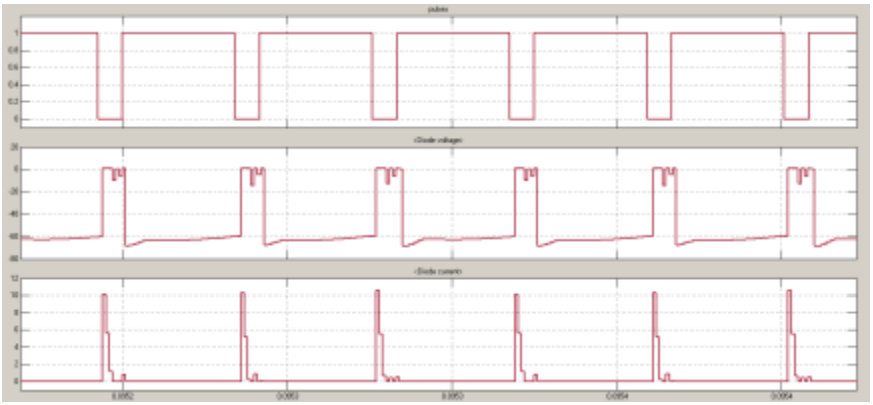

Fig. 8. Current and voltage waveform of diode

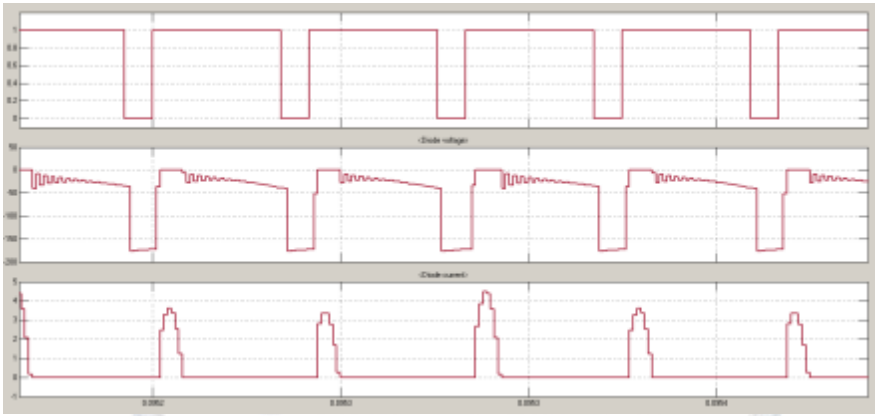

Fig. 9. Current and voltage waveform of diode

V. CONCLUSION

The modified version of the SEPIC converter is proposed for PV Applications. Although the proposed structure presents a higher circuit complexity than the classical boost converter, the advantages obtained are the higher static gain for the operation with the lower input voltage range, lower switch voltage operation and high efficiency operation with the lowest input voltage. Two clamping circuits are proposed in order to minimize the diode reverse recovery current problem.

The modified SPEIC converter provide a higher power efficiency (ɳ) compared to the basic SEPIC Converter (Vide table below).

	Input side			Output side			
	V	A	W	V	A	W	
Basic SEPIC converter	12.0	10.73	128.8	48.99	2.449	120	93.18
Modified SEPIC converter	12.0	8.558	102.7	240.1	0.4169	100.1	97.48

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