POWER OPTIMIZED CRUSOE PROCESSOR WITH REVERSIBLE LOGIC GATES USING ENHANCED VLIW ARCHITECTURES

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ABSTRACT:
The main objective of this project is to implement a novel processor for small-scale (minor) and large-scale (major) applications with low dense and low power consumption. In this, well-tuned pipelined architecture and enhanced power control schemes are introduced using modified MIPS (Micro Processor without Inter locked stages), VLIW (Very Long Instruction Word) and PFAL (Positive feed Back Adiabatic Logic) techniques along with BIST (Built in Self-Test) capability. Online and more accurate BIST is implemented with less processing time. This project is designed in such a way that; it is useful for both long and short distance; wired and wireless communications for both Synchronous and Asynchronous modes.

Key words: BIST, VLIW, PFAL, L.F.S.R (Linear Feed Back Shift Register), GALS (Global Asynchronous Local Synchronous), ILP (Instruction Level Parallelism)

INTRODUCTION: Now, days for every particular application; separate devices or processors are selected. If the applications are different; multiple processors are required with different structures. But there is no globalized processor for multi-purpose applications. Sub-micron VLSI technology reduces gate delays and increases wire delay in the system. This increases the impact of the clock skew on system performance. In synchronous model, global synchronization is difficult to achieve for the high performance system. In addition, clock synchronization cause power waste and supply clock signals to inactive functional modules too. To overcome such difficulties, researches are actively going on. An asynchronous system provides faster operation and lower power consumption for deep sub-micron systems. The circuits controlled with handshake protocol can avoid the clock-related timing problems, such clock-skew, by removing the global clock. Thus, the asynchronous system design is becoming one of the promising design styles [1]. Most of the asynchronous processors use pipeline architectures in order to improve system performance and handshake protocol, instead of the clock, which activates the pipeline stages. Chip fabrication amenities have transitioned to minor technologies, resulting in substantial rises in the number of hard errors, mainly due to variation, material defects, and physical failure during use, and the number of soft errors, due primarily to alpha particles from normal radiation decay, from cosmic rays striking the chip, or simply from random noise [1, 2, 3]. Soft errors are not measured to permanently break the circuit; on the other hand a hard error will permanently prevent a circuit from behaving as it was designed. It is therefore imperative that chip designers build robust fault-tolerance into computational circuits, and that these de-signs have the ability to detect hard and soft errors. That detection should capable of doing own itself. Without any manual interaction; the built in process in processor itself should check all errors in circuit under test. Generally, any processor consist only basic operations or extended to some D.S.P applications. But there is no device meant for all applications with more users friendly. Banking applications, bio medical applications, military applications, Telecom applications, general computer applications; for every applications, separately designed processor is required. But there is no unique processor to handle all these applications.

Analysis on Existing technologies:

- **VLIW:**

VLIW processor uses a long instruction word that is a combination Information about the machine needed by the compiler is broken down into six types of information, each of which has an associated hierarchy of sections. Register information several operations combined into one single long instruction word. VLIW architectures execute multiple instructions/cycle and use simple, regular instruction sets. This allows a VLIW microprocessor to execute multiple operations in parallel. In, VLIW architecture, the effectiveness of these processors depends on the ability of compilers to provide sufficient instruction level parallelism (ILP) in program code.

Draw backs:

.) A major drawback of VLIW is that it fully exposes the micro architecture of the machine to the instruction set architecture. A VLIW with 6 pipes has a 6-instruction bundle instruction word. If it is desired to expand to eight pipes in a new generation, then the ISA must change to reflect this, and all of the existing software becomes unusable without recompilation.

.)High program memory bandwidth requirements

.) High power consumption

.) Low through-put

.) The fact that individual threads can be unpredictably slowed by side effects from other threads means that such a design will be impossible to use for real-time applications such as native signal processing.

- **MIPS:**

MIPS concept follows the same theory using VLIW processor. MIPS measures roughly the number of machine instructions that a computer can execute in one second. Reduced instruction is the main criteria used to develop in this processor. With a single instruction scheme, more executions can be done using this MIPS concept.

MIPS instruction formats

Instructions are divided into three types: R, I and J. Every instruction starts with a 6-bit opcode. In addition to the opcode, R-type instructions specify three registers, a shift amount field, and a function field; I-type instructions require two registers and a 16-bit immediate value; J-type instructions follow the opcode with a 26-bit jump target. The following are the three formats used for the core instruction set:

Type	31 format (bits)					
R	opcode (6)	rs (5)	rt (5)	rd (5)	shamt (5)	funct (6)
I	opcode (6)	rs (5)	rt (5)	immediate (16)		
J	opcode (6)	address (26)				

Draw backs:

.)PC requires more clock pulses to execute any instructions.

.) Lot of decoding process exists in this type of architecture.

.) Formats are very complex to implement in practical manner.

- **Synchronous execution:**

In, general; more tasks execution per clock pulse is defined as Synchronous execution. Transmitter and receiver are appending with same frequency clock pulse. So, whenever we need high speed execution, synchronous execution is needed. Here, no need of inserting star bit and stop bit.

Draw backs:

.) Less reliable for long distance communications
.)More band width is needed to establish link

- **Adiabatic techniques:**

  The Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic), PFAL (Positive Feedback Adiabatic Logic), etc. Techniques are exists in present trend.

Draw backs:

.) These all techniques are limited in specified frequency range.
.) Adiabatic technique is highly dependent on parameter variation
.)More hardware complexity

Proposed Methodology

The Reversible Pipeline principle is described in CRUSOE processor with modified MIPS and VLIW. The entire architecture is having the capability to determine whether the yielded output is correct or not.

Figure1 depicts the modified pipelined MIPS architecture. As shown in figure, total process is divided in to two processes. Fetching and execution stages are only involved. Everything is in pipelined manner. It supports, single instruction multiple execution strategies. Here is no need to give multiple instructions to execute multiple operations. Single instruction itself gives multiple desired outputs without wasting bandwidth. D.S.P core is also implemented in this project with adiabatic techniques. It is mainly useful in signal processing for both short and long distance communications. In built parity, encoders, framing circuits are available along with this core.

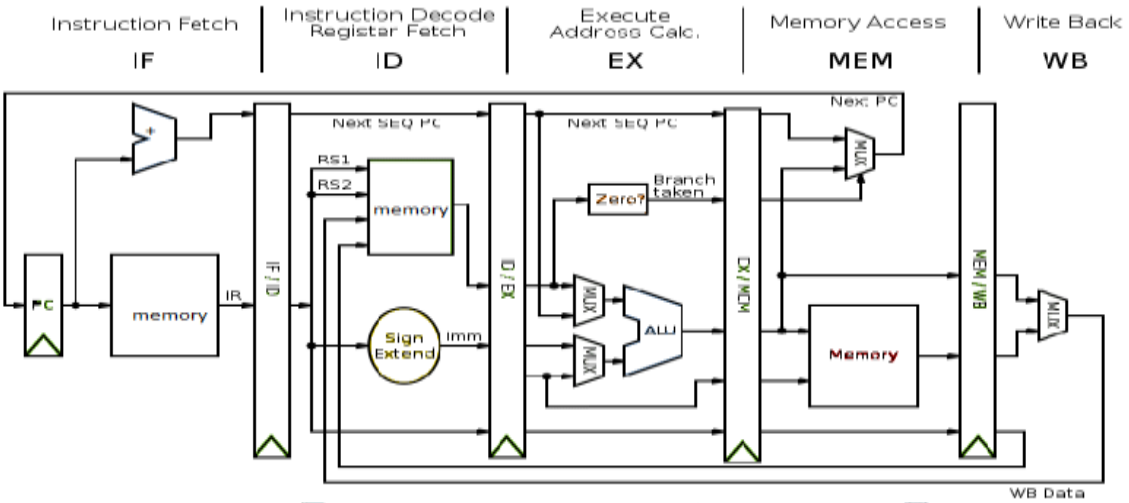


Fig1.Pipelined MIPS Architecture

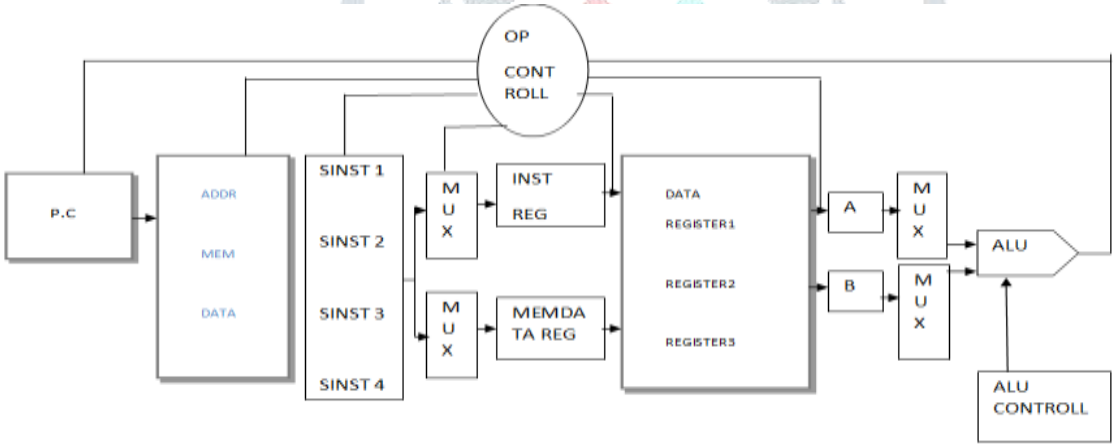


Fig2.Proposed architecture

Above block diagram is emblem for proposed technique. A.L.U is designed with reversible logic gates. A.L.U consists plenty of inbuilt operations, which are having switch level and system level instruction. Implies, constructed processor is having the capability to do all type of operations irrespective of applications. Every component in this project is constructed with modified PFAL ADIABATIC technique. For example, PFAL Inverter is as shown in below figure3.

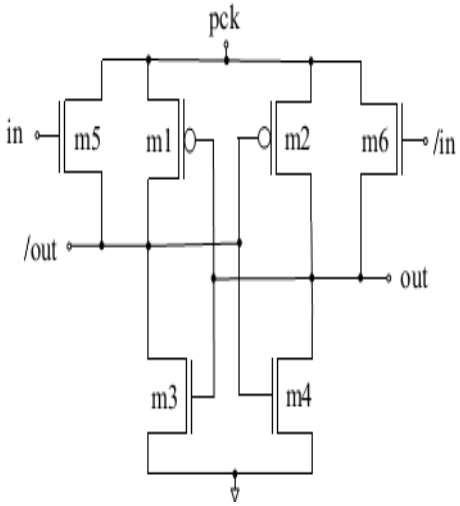


Figure.3 Modified PFAL inverter

Likewise, all components are implemented using modified PFAL technique. Along with that, designed processor is having efficient memory architecture.

MEMORYARCHITECTURE:

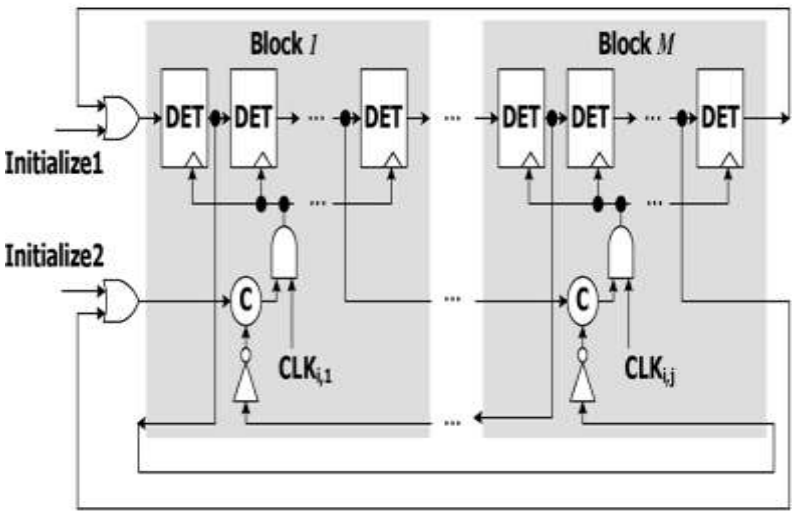


Figure.4 Efficient memory design with DET

Generally, multiplexers and De-multiplexers are used in front and after memory devices. Instead, those components, gated driver trees are utilized for more synchronization purpose. Entire memory is designed using Double edge triggered flip-flops. This D.E.T is having the capability to do work at both rising edge and falling edge. So, in a single clock pulse, these devices are having the capability to do two operations. Ring counter with clock gating technique is used for selecting rows in a memory.

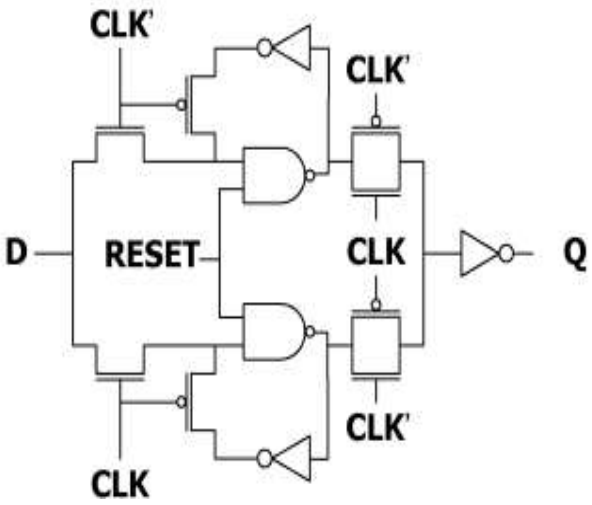
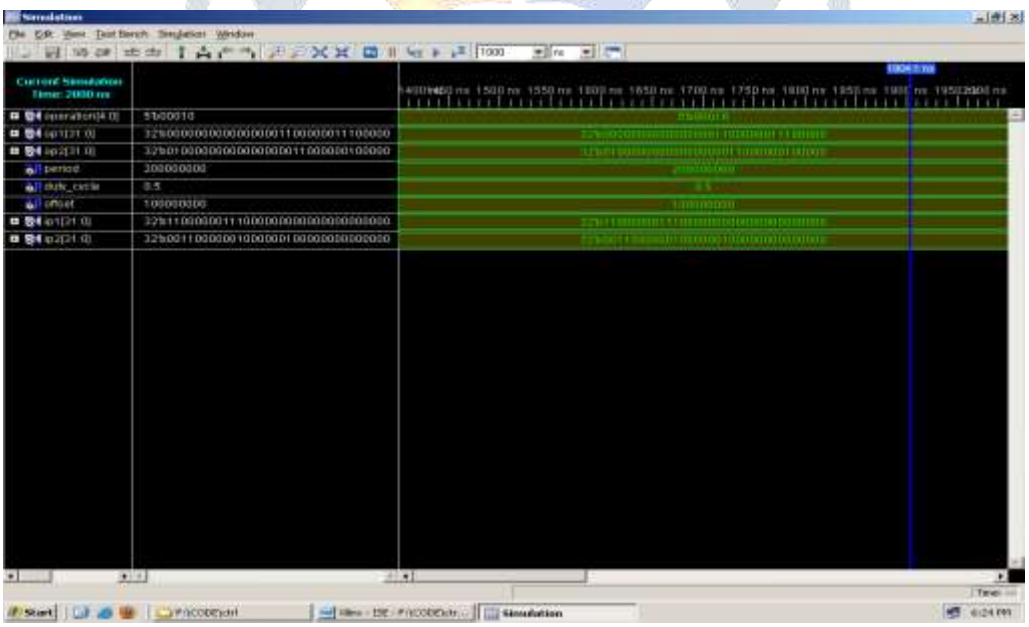


Fig5. Double edge triggered flip-flops

Designed memory architecture is having the capability to store two patterns in a single clock pulse. Implemented Processor exactly needs above memory architecture only, due to presence of S.I.M.E. Hence, exact synchronization takes place between processor and memory. The entire design is attached to BIST. Online based BIST approach with bit-swapping LFSR is having100% fault coverage. This BIST can be used for combinational circuits, sequential circuit and as well as for memories also. Generally, memory based tests requires more hardware. But in this technology, the scheme rests on partitioning of rows and columns of the memory array by employing low cost test logic. It is designed to meet requirements of at-speed test thus enabling detection of timing defects. The proposed BIST TPG decreases transitions that occur at scan inputs during scan shift operations and hence reduces switching activity in the CUT. This achieve very high fault coverage with a reason-able length of test sequence. Unacceptably long test sequences are often required to attain high fault coverage with pseudo-random test patterns for circuits that have many random pattern resistant faults. The main objective of most recent BIST techniques has been the design of TPGs that achieve high fault coverage at acceptable test lengths for such circuits.

SIMULATION RESULTS:



SYNTHESIS RESULTS:

RTL Top Level Output File Name : final.ngr

Top Level Output File Name : final

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

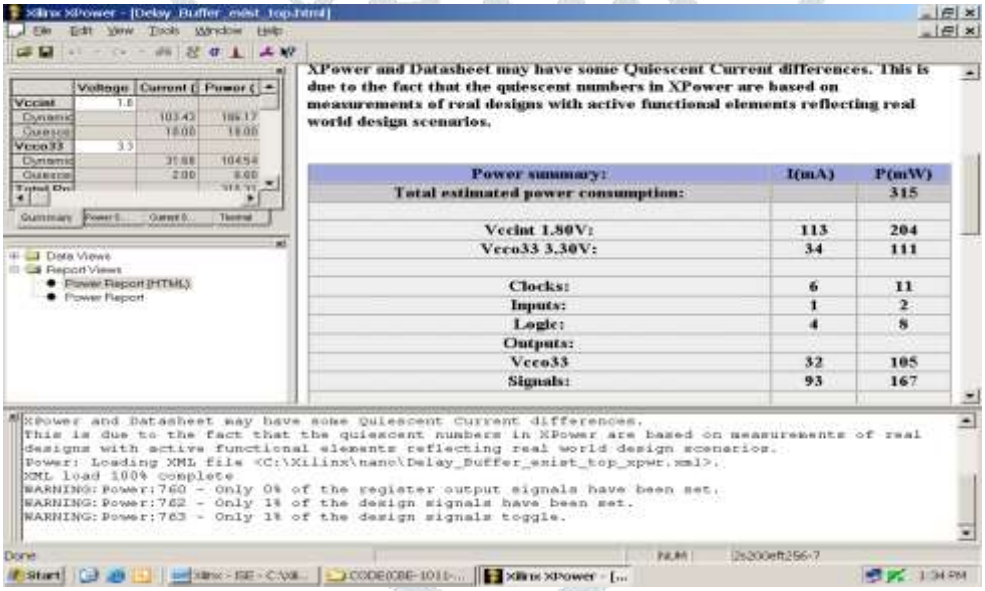
Design Statistics
IOs: 9Cell Usage :
BELS: 31# INV: 1#
LUT2: 15# LUT2_D : 1#
LUT2_L: 1#
LUT3_D : 2
FlipFlops/Latches: 14#

Clock Buffers: 1# BUFGP: 1# IO Buffers: 8#

IBUF: 5# OBUF: 3

Device utilization summary:

Selected Device: 3s500efg320-5
Number of Slices: 3892 out of 4656
Number of Slice Flip Flops: 8777 out of 9312
Number of 4 input LUTs: 589 out of 9312
Number of bonded IOBs: 25 out of 232
Number of GCLKs: 2 out of 24
POWER REPORT:



CONCLUSION:

A novel method for dynamically adapting the structure of a pipeline is implemented in this project. The processor has been designed for executing the instruction set comprising of fewer instructions in total. The processor design promises its use towards any signal processing applications. This brief has presented a pipelined/cached- processor for all communication system. GALS design and handshake clocking will become a major commercial design methodology primarily for power, performance and design modularity advantages. This will occur despite the significant technical obstacles. The paper discusses how scaling began to favor clocked design methodologies in present, and how it now favors advanced design methodologies.

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