A Brief Review on Multilevel Inverter Topologies

K.Chenchireddy
Department of EEE
Karunya University,
Coimbatore- 641114,India

V.Jegathesan
Department of EEE
Karunya University
India Coimbatore- 641114, India

Abstract-multilevel DC/AC inverters have various structures. They have many advantages unfortunately, most existing inverters content to many components (independent/floating batteries/sources, diodes, Capacitors and switches).the proposed "Ladder Multilevel DC/AC inverter" in this paper that is new approach of the development. This inverter uses fewer components. The proposed inverter simple structure and clear operation are obviously different from other existing inverters. Its application in solar panel energy system is successful.

Keywords- cascaded H-bridge, clamped flying capacitor multilevel inverter, diode clamped multilevel inverter, ladder multilevel inverter

I. INTRODUCTION

The power electronic device which has ability to convert the DC power into AC power is called as inverter. In 1925 David prince published his article named as "The Inverter". Initially the inverters were used to drive mostly the lightening load when the grid gets off. But, nowadays due to increased advancement in technology inverters enhances their horizon of applications. In earlier days only two level inverter were used and produces the output with two different voltage levels but it has high switching losses and harmonic voltage causes the flow of the harmonic current in the circuit and produces the losses. So, to overcome the disadvantages certain advancement takes place in existing inverter such that levels can be increased more than two so that pure sinusoidal waveform is produced at the output voltage and harmonics in the output can be suppressed and percentage of losses can be decreased and this topology is named as multilevel inverter topology.

There are mainly three different types of the multilevel inverter 1) Diode clamped multilevel inverter. 2) Flying capacitor multilevel inverter.3) Cascaded H-bridge inverter. Above these multilevel inverter has some advantages over the two level inverter [1].

1) Decreased Harmonic effect of distortion.
2) Pure sine waveform due to multiple voltage levels.
3) Operates at both fundamental and high switching frequency PWM
4) Reduced switching losses
5) High power quality
6) Low rate of change of voltage

Unfortunately multilevel inverters do possess some drawback one main drawback of these it requires number of switches even though they are of smaller rating. Each switch is related to its gate driving circuit because of that overall system becomes more complex and expensive

II. CONCEPT OF MULTILEVEL INVERTER

Conventional two level inverter produces only two levels in the output voltage and PWM is used to form the AC output waveform as shown in Fig.1. Even though the AC output waveform is produced it includes harmonics and these causes the high rates of change of voltage as compared to the multilevel inverter [1]. Some devices requests for low rate of change in voltage.

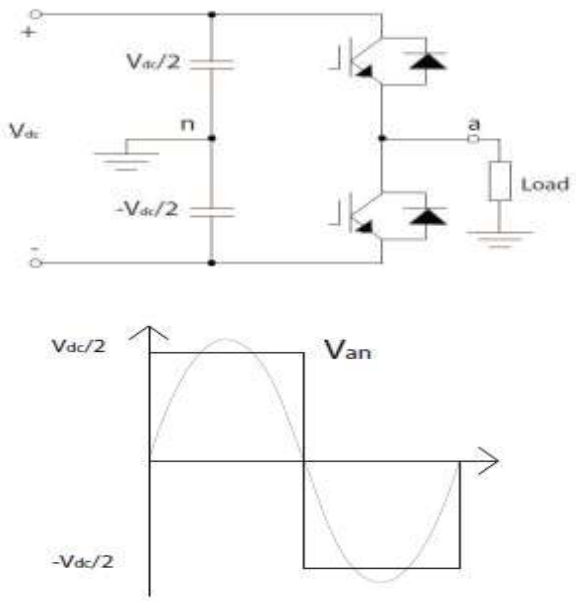


Fig.1. one phase limb of a two-level inverter and a two-level waveform without PWM

In multilevel inverter we generate more than two voltage levels which exhibits almost pure sinusoidal output voltage waveform. Which has low dv/dt, low harmonic distortions.[1,2] because of multiple voltage levels in the output the waveform becomes more smoother but with increasing levels the circuit becomes more complex due to addition of the valves. And complicated control circuit is also required.
For understanding purpose the circuit diagram of three level inverter is shown Fig.2 and Fig.3 below [1,2] which produces the voltage levels of +Vdc/2, 0, - Vdc/2. This design resembles to the two level inverter having only two additional switches and diodes are used and called as clamping diodes.

Fig.2. single phase leg of a three level inverter

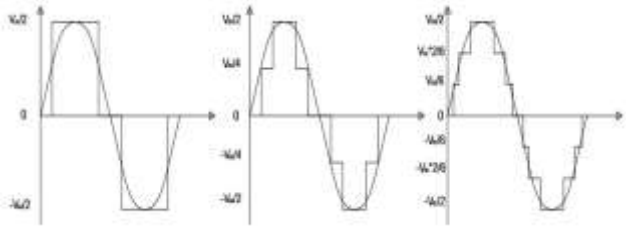


Fig.3. a 3 level waveform 5-level waveform and a 7-level multilevel waveform

III.DIFFERENT TOPOLOGIES OF MULTILEVEL INVERTER

There are basically three types of multilevel inverter classified according to the voltage source used in the inverter. The Fig.4 below shows the topologies of multilevel inverter.

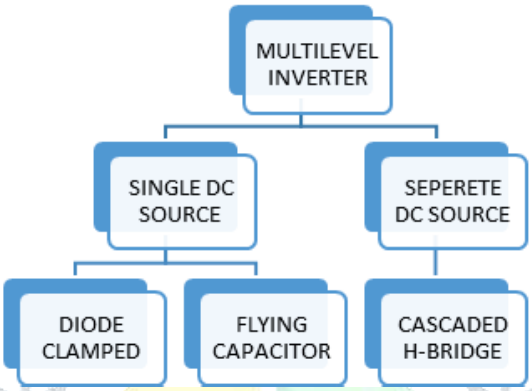


Fig.4. classification of multilevel inverter

A. DIODE CLAMPED MULTILEVEL INVERTER

This topology uses the diodes to clamp the voltage that is to suppress the voltage stress on power devices. These are the first practically implemented multilevel inverter topology. The configuration of the circuit topology is given below [1, 2].
Number of switches for m-level= 2(m-1).
Input voltage source= (m-1).
Diodes for clamping voltage= (m-1)(m-2).

The circuit diagram for five level inverter and its waveform is shown in Fig.5 and Fig.6

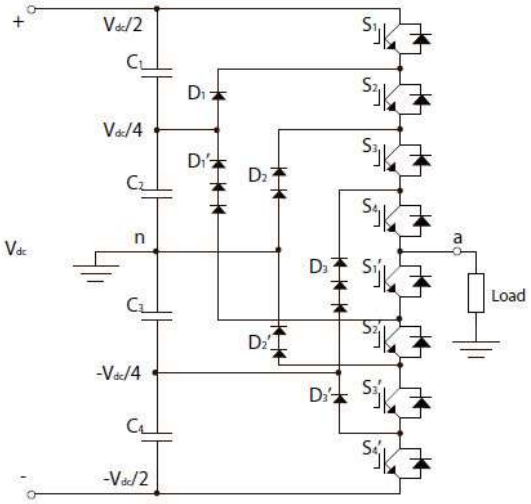


Fig.5.single phase leg of a 3-level inverter

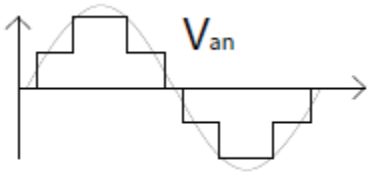


Fig.6.single phase- leg for a 5 level NPC inverter and waveform

In [5] proposed topology is derived from the traditional structure of MLI. This can be demonstrated by incorporating asymmetrical type of arrangement so that multiple voltage levels can be synthesized and this can be realized by high voltage GTO and fast switching IGBT. And finally present the comparison table for seven level inverter structure. In [6]present generalized structure of multilevel inverter which can balance the DC voltage without any external circuit. Traditional two level inverter can also be obtained from this generalized structure. Proposed generalized structure has more than three levels with self voltage balancing capability, even though it possess more capacitors, switches, diode in principle it is complete MLI. And also has capability to give some new MLI structure. In [7] presents and compares several topologies of MLI in high power application. this topology is concern with multicell converter with flying capacitor and proposed new stacked multicell converter(SMC) in that input voltage is distributed 'n' equal voltages corresponds to n stacks of topology, here study of multicell inverter shows their advantages concern with the energy stored and losses in the switches for given application. In [8] is concern with the design of the diode clamped MLI which can replace the heavy transformer connected to the grid. Their main agenda is design of the diode clamped MLI which can give the multiple voltage levels for that they derived the number of equations and figures. In [9] proposed practical way of balancing the DClinkvoltages. The back to back linking of the multilevel rectifier with multilevel inverter allows the balance of the DC link capacitor voltage and also offers power factor correction capability. In [10,11] proposed five level diode clamped inverter applied STATCOM. An offline optimization of switching angle together with fundamental frequency modulation strategy (FFM). When it is used in STATCOM there active power compensation is accomplished by controlling flow of active power between inverter circuit and ac system.

B. FLYING CAPACITOR MULTILEVE INVERTER

The flying capacitor multilevel inverter is alike to that of the diode clamped MLI only difference is that instead of clamping diodes capacitors are used for clamping purpose. This topology is having the tree structure of dc side capacitors where voltage of each capacitor differs from that of the next capacitor. The statistics for this topology is given below for five level.

The no. of switches for m-level= 2(m-1) = 8

The no. of DC-link capacitors= (m-1)= 4

The no. auxiliary capacitors= ((m-1)(m-2))/2=6

The circuit diagram and the waveforms are shown in Fig.7

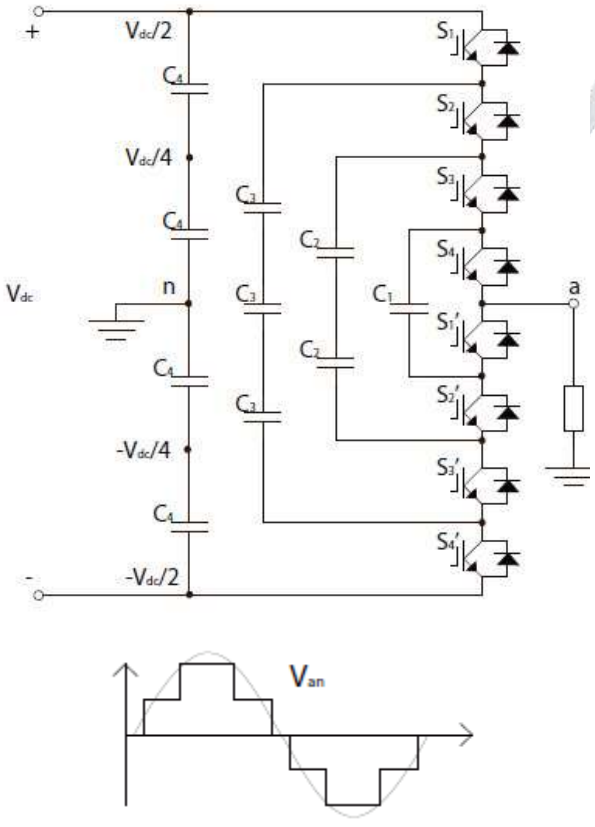


Fig.7. single phase of a 5-level Flying capacitor multilevel inverter

In [12] discussed about the developing the low cost boost-trappower supply for FCMLI and its gate drive circuit is also discussed. In [13] proposed

about the soft-switching technique in the flying capacitor multilevel inverter so that it can be extended from three level to any level. The advantage of this inverter is having low voltage and current rating of switching valves and this can be achieved by using the coupled inductor. Design, operation, control and switching patterns are also presented. In [14] proposed snubber for the flying capacitor multilevel inverter. Snubber circuit uses less no of switches, less switching losses, also improves efficiency. In [15] developed soft-switching active power filter for maglev train application. This active filter is having the flying capacitor MLI based on coupled inductor. And this proposed MLI active power filter is studied for various levels. In [16] proposed the new PWM strategy for DC capacitor balancing and can be called as the carrier rotation strategy. This strategy uses phase leg voltage redundancy for charging and discharging of the capacitor using the simple algorithm for using the switch combination. In [17] proposed novel design by combining the diode clamped or flying capacitor with the two level inverter legs. As compared to the conventional MLI this design need fewer clamping diodes and switches for the same no of levels.

C. CASCADED H-BRIDGE INVERTER

In H-bridge inverter it uses more than one DC sources. Every inverter generates output at different levels. The output voltage is the sum of all voltage levels generated by each cell. The number of levels in output voltage is = 2n+1Where 'n' is the number of input sources. Especial feature of this inverter is that it requires lesser no of switches than diode clamped multilevel inverter. The circuit diagram and the waveforms are shown in Fig.8 below

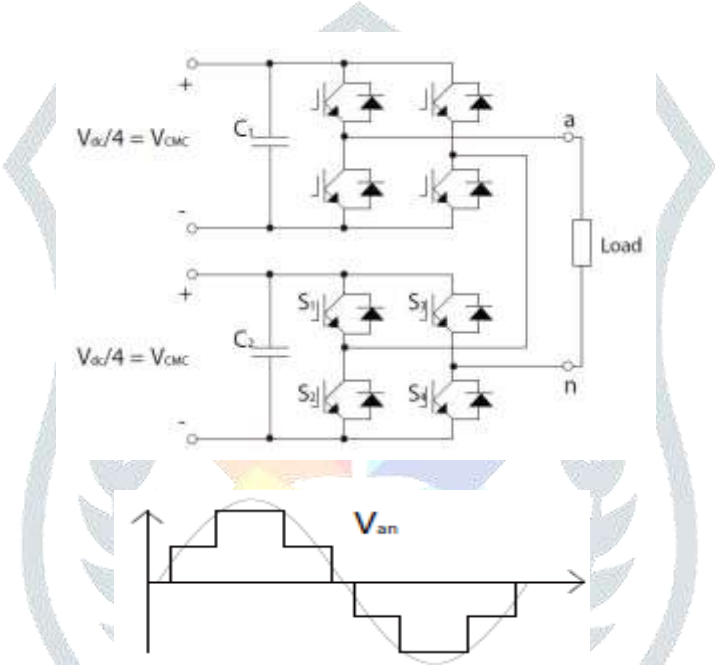


Fig.8.Single-phase structure of a 5 level multilevel cascaded H-bridge inverter.

In [18] proposed novel design of cascaded H-bridge building block by newly developed emitter turn off thyrister to show the superior act of the ETO and this can be used in reactive power compensation application. The h-bridge blocks can beaded or removed based on requirement of the power. And also proposed the new air core snubber inductor design which is lighter than conventional iron-core inductor and also decreases the losses. In [19] proposed the control procedure of the cascaded MLI used in shunt active filter and this can be expanded to more levels. and according to the design controller is proposed to suppress the harmonics and reactive190power for non-linear load. In [20] proposed the general structure of the h-bridge. Where voltage sources are connected in series and equations are to be introduced to choose the voltage ratios of the capacitor or sources to maximize the output voltage level. In [21] proposed novel cascaded multilevel inverter which considerably reduces the voltage ripples in the dc- link and this topology includes single diode joined for each basic H-bridge. In [22] proposed novel design of cascaded H-bridge which is combined with number of H-bridge cells as compared with

conventional cascaded H-bridge. This design reduce the cost as well as simplifies the circuit and THD is also limited here than conventional one. In [23] H- bridge inverter causes some oscillations under light load and these oscillations are analyzed and novel mitigation method is proposed. In [24, 25] a new control algorithm is investigated for inverter operating under faulty conditions.

IV.PROPOSED INVERTER MODEL

The proposed linear laddered inverter constructed following unit progression. The output voltage Vout has M levels and M=2b+1
$|Vdci| = E$
$i = -b, -(b-1), \ldots, -2, -1, 1, 2, \ldots, b-1, b$
The operation status is shown below

- Vout = bE: all positive wing switches on (others are off);
- Vout = (b − 1)E: switches S1 – Sb−1 are on (others are off);
- Vout = 2E: switches S1 – S2 are on (others are off);
- Vout = E: only switch S1 is on (others are off);

- Vout = 0: all switches are off;
  Vout = − E: only switch S−1 is on (others are off);
  Vout = −2E: switches S−1 – S−2 are on (others are off);
  Vout = −(b − 1)E: switches S−1 – S−(b−1) are on (others areoff);
  Vout = −bE: all negative wing switches on (others are off).
  We obtain n = 2b + 1 levels.
  For example ifb = 3, we havethe total level number n = 7 levels. The output voltage Waveform is shown in Fig. 9.

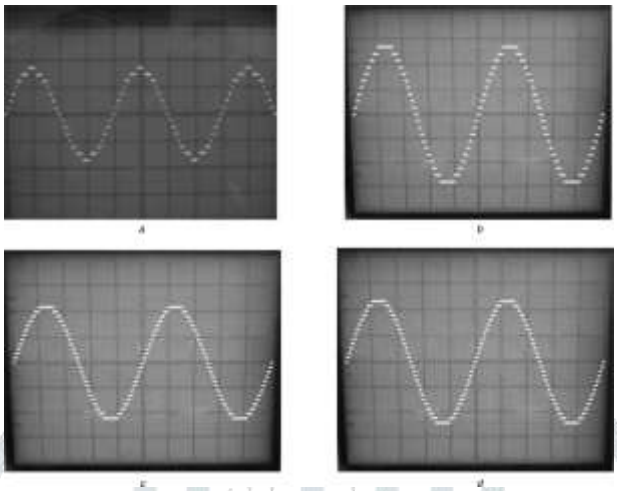
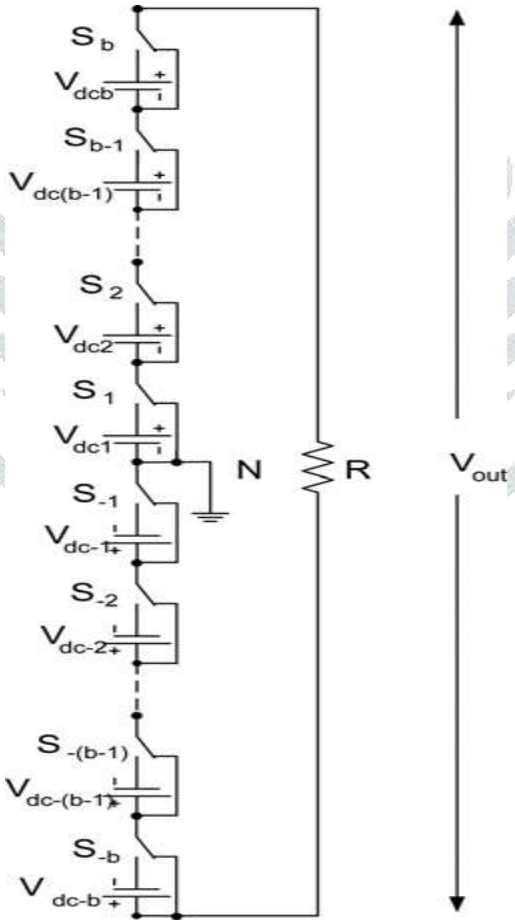
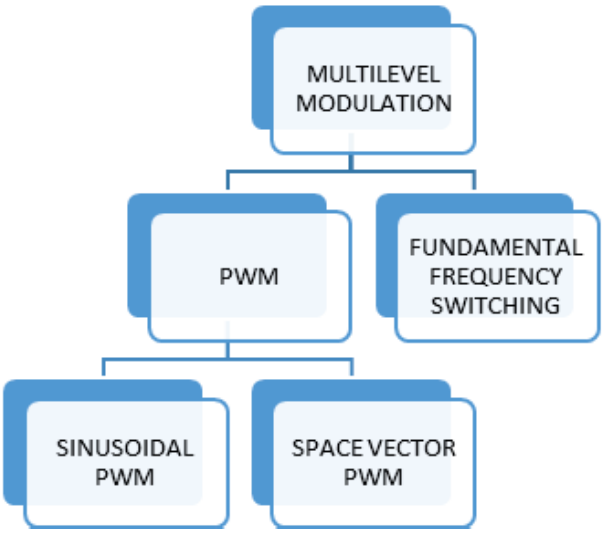


Fig.9.output ladder MLI



V. MODULATION TECHNIQUES FORMULTILEVEL INVERTER

Different modulation technique are given below



VI.CONCLUSION

Laddered multilevel inverters have simple structure, clear operation procedure, easy control and more output voltage levels. We can use fewer components to construct more level output voltage, therefore the cost is lower.

REFERENCES

[1] Anjali Krishna R. and Dr L Padma suresh "A brief review on multilevel inverter topologies" Conference on Circuit, Power and Computing Technologies [ICCPCT] 2016 .
[2] Nordvall "Multilevel inverter topology survey" thesis in electrical powerengineering 2011
[3] M. Murugesan and R. Sivakumar "Different types of multilevel invertertopologies-A technical Review" E-ISSN, mar 2016.
[4] A. Narendra babu and Sunil hansdah "Study and analysis of three phase multilevel inverter "Thesis, 2007
[5] M. D Manjrekar, Thomas A. Lipo "A hybrid multilevel inverter topology for drive applications" Power Electronics Conference and Exposition, 1998. APEC '98. Conference Proceedings 1998., Thirteenth Annual Year: 1998, Volume: 2 PP: 523 - 529 vol.2,
[6] Zheng Peng "A generalized multilevel inverter topology with selfvoltage balancing"IEEE Transactions on Industry Applications Year:2001, Volume: 37, Issue: 2 PP: 611 - 618
[7] L. Demas; T. A. Meynard; H. Foch; G. Gateau "Comparative study of multilevel topologies: NPC, multicell inverter and SMC 828 – 833.withIGBT" IECON 02 [Industrial Electronics Society, IEEE 2002, 28thAnnual Conference of the Year: 2002, Volume: 1
[8] J. von Bloh; R. W. De Doncker "Design rules for diode-clamped multilevel inverters used in medium-voltage applications" Power Electronics Congress, 2002. Technical Proceedings. CIEP 2002. VIIIIEEE International Year: 2002 PP: 165 - 170,
[9] M. Marchesoni; P. Tenca "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages" IEEE Transactions on Industrial Electronics Year: 2002, Volume: 49, Issue: 4 PP: 752 - 765
[10] S. Kincic; A. Chandra; S. Babic "Five level diode clamped voltage source inverter and its application in reactive power" Compensation "Power Engineering 2002 Large Engineering Systems Conference on,LESCOPE 02 Year: 2002 PP: 86 - 92,
[11] Alian Chen; Xiangning "A hybrid clamped multilevel inverter topology with neutral point voltage balancing ability" Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual Year:2004, Volume:5 PP: 3952 - 3956192
[12] S. A. Molepo; H. D. T. Mouton Power "A flying capacitor multilevel inverter with bootstrap- powered MOSFET gate drive circuits" Electronics Specialists Conference, 2002. pesc 02.2002IEEE 33rd Annual Year: 2002, Volume: 2 PP: 701 - 705
[13] Byeong-Mun Song; Juhyung Kim; Jih-Sheng Lai; Ki-Chul Seong; Hae-Jong Kim "A multilevel soft-switching inverter with inductor coupling";Sun-Soon Park IEEE Transactions on Industry Applications Year: 2001,Volume: 37, Issue: 2 PP: 628 - 636,
[14] In-Dong Kim; Eui-Cheol Nho; Heung-Geun "A generalized Undelandsnubber for flying capacitor multilevel inverter and converter" IEEE Transactions on Industrial Electronics Year: 2004,Volume: 51, Issue: 6PP: 1290 – 1296
[15] B. -M. Song; J. -S. Lai; Chang-Yong Jeong Dong-Wook Yoo "A soft switching high-voltage active power filter with flying capacitors for urban Maglev system Applications" Industry Applications Conference,2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001IEEE Year: 2001, Volume: 3 PP: 1461 - 1468
[16] D. -W. Kang; W. -K. Lee; D. -S. Hyun "Carrier-rotation strategy for voltage balancing in flying capacitor multilevel inverter" IEEE Proceedings - Electric Power Applications Year: 2004,Volume: 151,Issue: 2 PP: 239 – 248
[17] Sanmin Wei; Bin Wu; R. Cheung" A novel SVM algorithm for reducing oscillations in cascaded H-bridge multilevel inverters" Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE Year: 2003, Volume: 1 PP: 18 - 23
[18] Sanmin Wei; Bin Wu; Fahai Li; Xudong Sun" Control method for cascaded H-bridge multilevel inverter with faulty power cells" Applied Power Electronics Conference and Exposition, 2003. APEC '03.Eighteenth Annual IEEE Year: 2003, Volume: 1, PP: 261 – 267
[19] K. Corzine; Y. Familiant "A new cascaded multilevel -bridge drive K.Corzine;" IEEE Transactions on Power Electronics Year Volume: 17,PP: 125 – 131, Year: 2002,
[20] Andrés A. Valdez-Fernández, Pánfilo R. Martínez-Rodríguez, GerardoEscobar, Cesar A. Limones-Pozos,José M. Sosa" A Model-Based Controller for the Cascade H-Bridge Multilevel Converter Used as a Shunt Active Filter" IEEE Transactions on Industrial ElectronicsYear:2013, Volume: 60 PP: 5019 – 5028
[21] S M. Carpaneto,G. Maragliano, M. Marchesoni and L. R. Vaccaro," ANovel approach for DC-link voltage ripple reduction in cascaded multilevel converters" PEEDAM 2006. International Symposium on Power Electronics, Electrical Drives, Automation and Motion Year:2006 PP.571 – 576

[22] Sanmin Wei; Bin Wu; Fahai Li "Control method for cascaded H-bridge multilevel inverter with faulty power cells" Xudong Sun Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE Year: 2003, Volume: PP: 261 - 267
[23] Corzine Y. Familiant "A new cascaded multilevel H-bridge drive" IEEETransactions on Power Electronics Year: 2002, Volume: 17, Issue: 1 PP:125 – 131
[24] Andrés A. Valdez-Fernandez "A Model-Based Controller for the Cascade H-Bridge Multilevel Converter Used as a Shunt Active Filter"IEEE Transactions on Industrial Electronics Year: 2013, Volume: 60,Issue: 11 PP: 5019 – 5028.
[25] M. Carpaneto; G. Maragliano "A Novel approach for DC-link voltage ripple reduction in cascaded multilevel converters" International Symposium on Power Electronics, Electrical Drives, Automation and
Motion, 2006. SPEEDAM 2006. Year: 2006 PP: 571 – 576.
[26] Surin Khomfoi and Leon M. Tolbert Chapter 31 Multilevel Power Converters The University of Tennessee193