IMPLEMENTATION OF MODIFIED BOOTH MULTIPLIER USING MODIFIED HYBRID ADDER

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Abstract: ***In digital circuit multiplier plays a very important role. Multiplier has important role in DSP, microprocessor and microcomputer applications. The time that required to do calculation in multiplier is reduced by using modified booth multiplier. The speed of multiplier determines the speed of any processor. So there is a need of high speed multiplier. In this paper modified booth multiplier is used to design the multiplier. In this paper, Multiplication algorithium is analyzed by modified Booth algorithm, Wallace Tree architecture and modified Hybrid Adder design [1]. Modified booth multiplier is to design so that the partial product is going to be decreases. Wallace Tree is boost up the speed by parallel addition of Partial Products. Adders play an important role in addition of partial products. If the speed at which the addition operation is performed is increased than the overall speed of the multiplier design will increase. So the main motivate in this paper is to increase the speed of the adder. Modified hybrid adder design is used in the multiplier design which, has less delay and occupies less area and consume less Power. Area, delay and power complexities of the proposed Multiplier design are reported [2]. The proposed Modified Booth Multiplier using modified Hybrid adder design shows better performance as compared to conventional using Hybrid adder design and has advantages of reduced area, Power and critical path delay. The proposed multiplier design has been synthesized using Xilinx ISE 14.7design tool and simulated using Model Sim. The programming language used is Verilog HDL.***

Index Terms- Modified Booth Multiplier, Wallace Tree, Hybrid Adder, Modified Hybrid Adder, VLSI.

I. INTRODUCTION

Multipliers are very important part of digital Signal system. It is widely used component in computer arithmetic and Very large scale integration. Multipliers are more complex as compared to the subtract or and adder. The multiplier basically used to resolve the operating speed of digital signal processing with many technologies scheme is referred [2]. The techniques have been proposed to design multiplier which provides high speed, lower power consumption, and small area.

The procedure of multiplication is divided into three sections: partial product (PP) generator, a tree structure to add the partial products and final addition. In partial product generation stage booth encoder is used to generate as well as reduce the number of partial products. In case of the Modified booth multiplier the number of partial products are reduced to half that is much faster than booth multiplier[2]. A Wallace tree structure is used for parallel addition of partial products. In final addition, the high speed adders are used for fast additions.

II. OVERVIEW OF KOGGE STONE ADDER

Kogge Stone adder is the parallel prefix type carry look ahead adder. The kogge stone adder was developed by Peter M. Kogge and Harold S. Stone that they printed in 1973. It is considered as one of the fastest addition method.The Kogge Stone has low complexity, high node count, and minimal fan out. While a high node count implies a larger area, the low logic complexity and minimum fan-out allow faster performance. Carry generation is much faster because of parallel computation. The Kogge Stone adder comprises of three stages like Pre-processing Stage, Carry generation Stage and Post-Processing Stage.

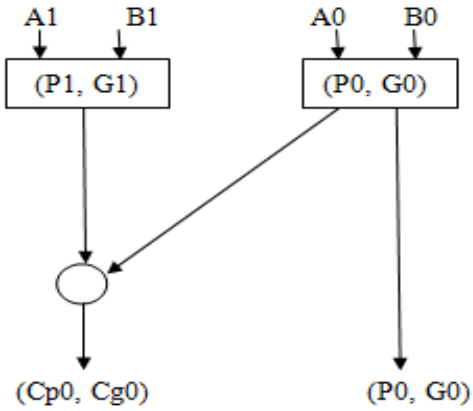

Fig 1: 2-bit Kogge Stone Adder

In the pre-processing stage propagation and generation signals are generated Carry Generation Stage is used to generate carry for the next stages and finally Post-processing Stage is used to generate Sum and carry out bit[2] .

In fig 1 every vertical stage produces Propagate and Generate bits. Generate bits are created within the last stage and these bits are XOR ed with the initial propagate once the input to apply the add bits.

III. MODIFIED KOGGE STONE ADDER

All the designing levels of digital systems or IC's Packages depend on number of gates on a single chip. Modified Kogge Stone adder can be reduced the area or number of gates. The matter of complexity can be reduced by the designing of gates. Less number of gates provides the less area for designing in digital processing. XOR gate is comprised with five gates. XOR can also be replaced by multiplexer (MUX). In digital electronics we are having two type of universal gates like NAND and NOR gate.

By using these to gates be can design any type of gate. Same as multiplexer behaves like as universal gates. By using multiplexer any type of gate can be design[10].

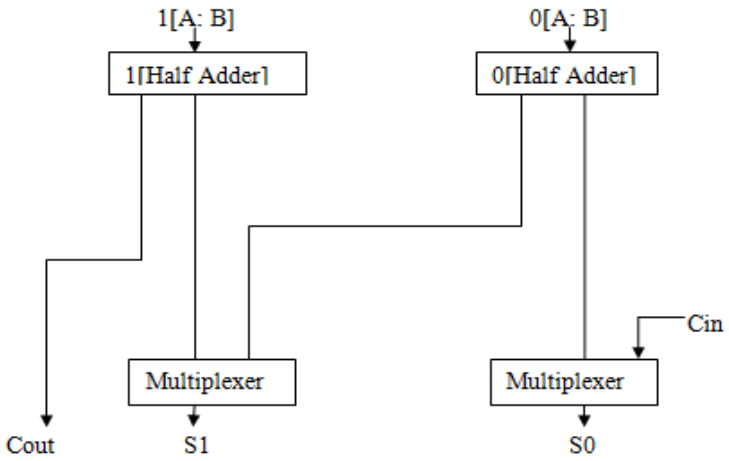

Fig 2: 2-Bit Modified Kogge Stone Adder

To design the two inputs XOR gate one input of MUX must be invert to the other and both input would be connected together. Another input of XOR gate would be applied to the select line of multiplexer. So, the output of multiplexer would be as same as the output of XOR gate. The advantage of this type of designing is that it produces both true and complementary outputs when provided with true and complementary inputs.

IV. HYBRID ADDER DESIGN

Hybrid adder (kogge stone based carry select adder) is the faster addition technique generated by merging two adder designs that is carry select adder and kogge stone adder. The carry-select adder is simple but fast. The carry select adder consist of two Ripple Carry Adder circuits and Multiplexer. The main idea to save delay in carry select is to calculate all the bits and thus choosing only the correct one to obtain the result.

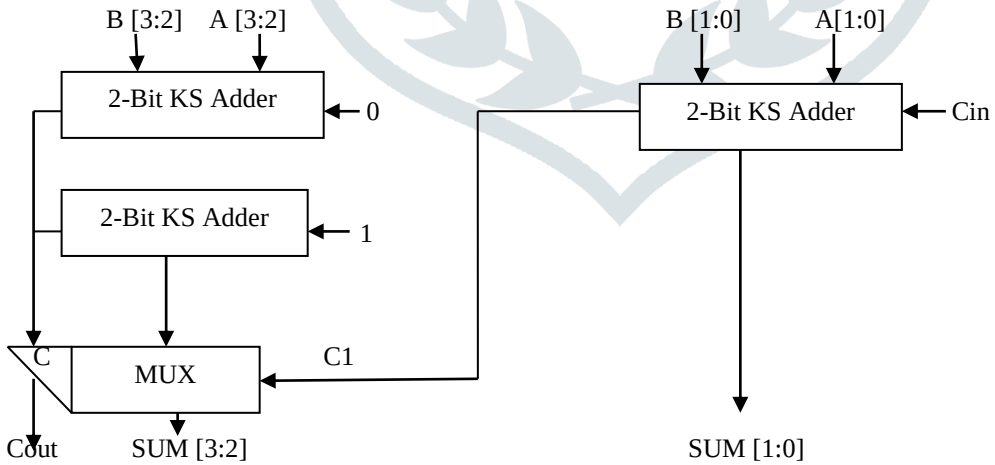

Fig 3: Block Diagram of 4-Bit Hybrid Adder (kogge Stone Based Carry select)

Hence the two adders will calculate the sum and carry bits simultaneously and correct sum and carry bits are selected by multiplexer once the carry in bit is known. Since Ripple Carry Adder is used in the circuit the delay is much more increased so replace RCA with Kogge Stone Adder which is a parallel prefix form of carry look ahead adder. Kogge Stone generates carry bit fast. Hence in both adders the delay is reduced so the properties of both the adder can be used to design the high speed adder circuit. A Pair of 2:1 Multiplexers is used in order to select actual sum bit. From the fig 3, it is clear that first two bit operation is done using kogge stone addition method and assuming two different carry signal i.e. either 0 or 1, all other paired block have been calculated two times by the same way. Many multiplexers are used in order to select actual sum as number of input bit increases.

V. MODIFIED HYBRID ADDER DESIGN

Modified Hybrid adder (Modified kogge stone based carry select adder) is the faster addition technique generated by merging two adder designs that is carry select adder and modified kogge stone adder. In this hybrid adder design, Kogge stone is replaced with Modified kogge stone adder. Modified kogge stone adder is speedier and gate count of modified kogge stone adder is less as compared to simple kogge stone adder[7].

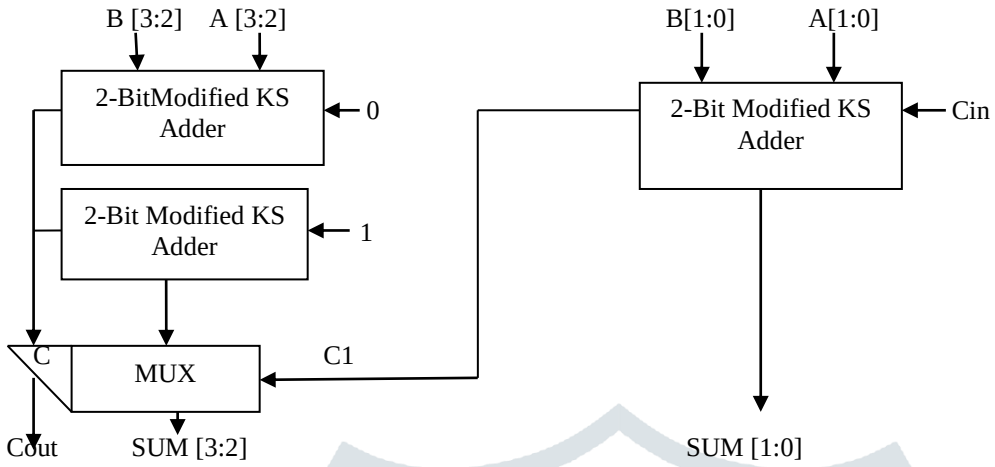

Fig 4:-Block Diagram of 4-Bit Modified Hybrid Adder (Modified kogge Stone Based Carry select)

VI. PROPOSED MODIFIED BOOTH MULTIPLIER

The proposed multipliers are combination of two multiplier architecture such as modified booth multiplier and Wallace tree multiplier architectures. In modified booth multiplier, by booth encoding the numbers of partial products are reduced and the speed of the multiplication is to be increased. Wallace tree architecture is used to increase the speed of parallel addition of partial products. When we are combined together then the speed of multiplication is to be increased [5] [6] [7].

The proposed modified multiplier consists of four parts: booth encoder, booth decoder, complement generator, Wallace tree architecture. The booth encoder encodes all the multiple signals and the output of given signal is fed to the booth decoder which generates the partial products. These partial products are arranged parallel in Wallace tree architecture and carry save adder. In the final stage, fast adder that is modified kogge stone based carry select adder is used to add the last two rows of sum and carry output.

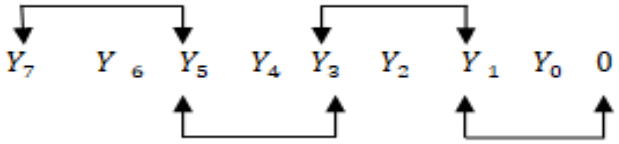

Fig 5**:** Grouping of three bits in the multiplier for encoding the partial products

Two's complemented are needed whenever signed operations are performed. It differentiates to the positive and negative multiplicand numbers to be added. Booth encoder is used to decrease the partial products as compared to simple booth multiplier. Booth encoder can multiply not only positive but also negative numbers and at the same time reduce the number of partial products. Booth encoder provides the signal to the booth decoder on the basis of bits obtained in the multiplier.

The based on encoder signals the decoder will produces the partial products. These signals will indicate the operation to be performed by the decoder on the multiplicand in order to produce the partial products. The multiplexer unit takes the input signals from booth encoder and complements values of multiplicand and generates the value in the form of bar or not bar.

TABLE I
Encoded Values of Booth

A2(x2i + 1)	A1(x2i)	A0(x2i -1)	Fn	neg	two	one	Zero
0	0	0	+0	0	0	0	1
0	0	1	+x	0	0	1	0
0	1	0	+x	0	0	1	0

0	1	1	+2x	0	1	0	0
1	0	0	-2x	1	1	0	0
1	0	1	-x	1	0	1	0
1	1	0	-x	1	0	1	0
1	1	1	0	1	0	0	1

Wallace tree architecture is used to increase the speed of parallel addition of partial products. When we are combined together then the speed of multiplication is to be increased.
Once the addition operation is performed on partial products in the Wallace tree structure it results in to two rows which consist of sum and carry bits. These two rows are added by using Modified Hybrid adder.

VII. IMPLEMENTATION

The results of proposed design are compared with conventional design. The results of the proposed Hybrid adder (kogge stone based carry select) design is compared with the modified hybrid adder (modified kogge stone based carry select) design in terms of area and power and delay.

TABLE II

Delay, Area and Power analysis of adder designs

ADDERS DESIGN	HYBRID ADDER	MODIFIED HYBRID ADDER
Number Of Slice LUT's	4 out of 28800	4 out of 28800
Number of occupied slices	3 out of 7200	3 out of 7200
Gate Count	130	76
Delay	4.017 ns	3.774 ns
Dynamic Power	12.39 (m W)	10.32 (m W)

The consumption of designs is measured in terms of Power obtained and the area in terms of number of LUTs utilized and gate count and speed is measured in terms of delay.
Table II shows the comparison between the Modified Hybrid Adder and existing Hybrid adder architectures with respect Power, area and delay. We can see that the Modified Hybrid Adder is most efficient in terms of power and area. The designs are simulated using the Model Sim simulator and synthesized using Xilinx ISE14.7. The target implementation device is Xilinx Vertex5 (family), XC5VLX50 (Device),FF676 (Package),-3(Speed Grade) FPGA under the working environment of Xilinx ISE 14.7.
The results of the proposed Modified booth Wallace Tree multiplier using modified hybrid adder (Modified kogge stone based carry select) design are compared with the modified Booth Wallace Tree multiplier using hybrid adder (modified kogge stone based carry select) design in terms of delay, area and power.

TABLE III

Comparison table of Modified Booth Multiplier using Adder design

PARAMETERS	MODIFIED BOOTH MULTIPLIER USING HYBRID ADDER	MODIFIED BOOTH MULTIPLIER USING MODIFIED HYBRID ADDER
Number Of Slice LUT's	81 out of 28800	80 out of 28800
Number of occupied Flip-Flop slices	36 out of 7200	34 out of 7200
Gate Count	1094	1040
Delay	7.912 ns	7.741 ns
Dynamic Power	37.78 (m W)	37.73(m W)

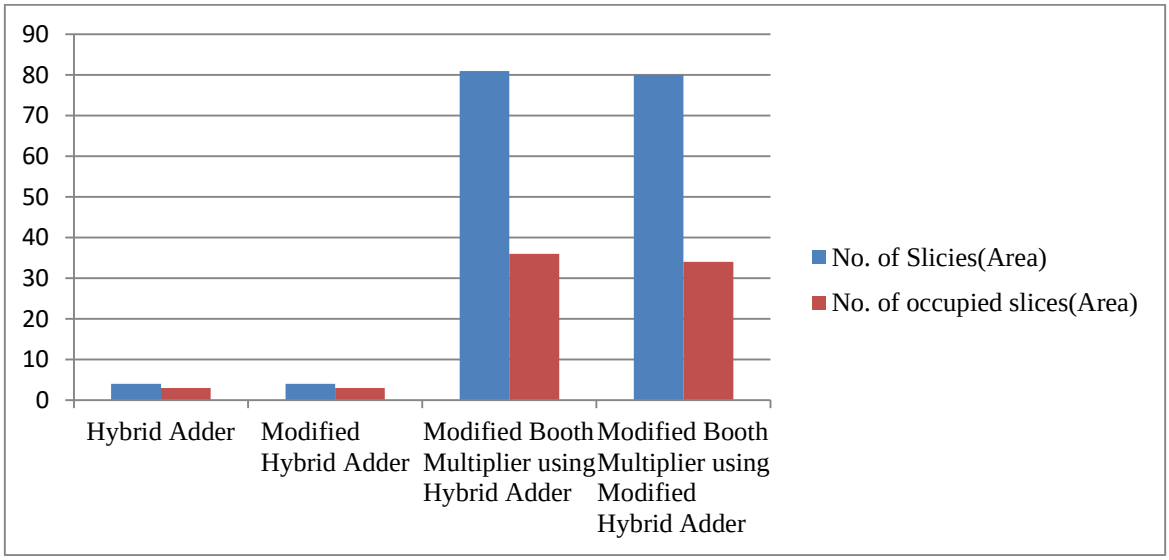

Fig 6: Comparison of Area in terms of Number of slices

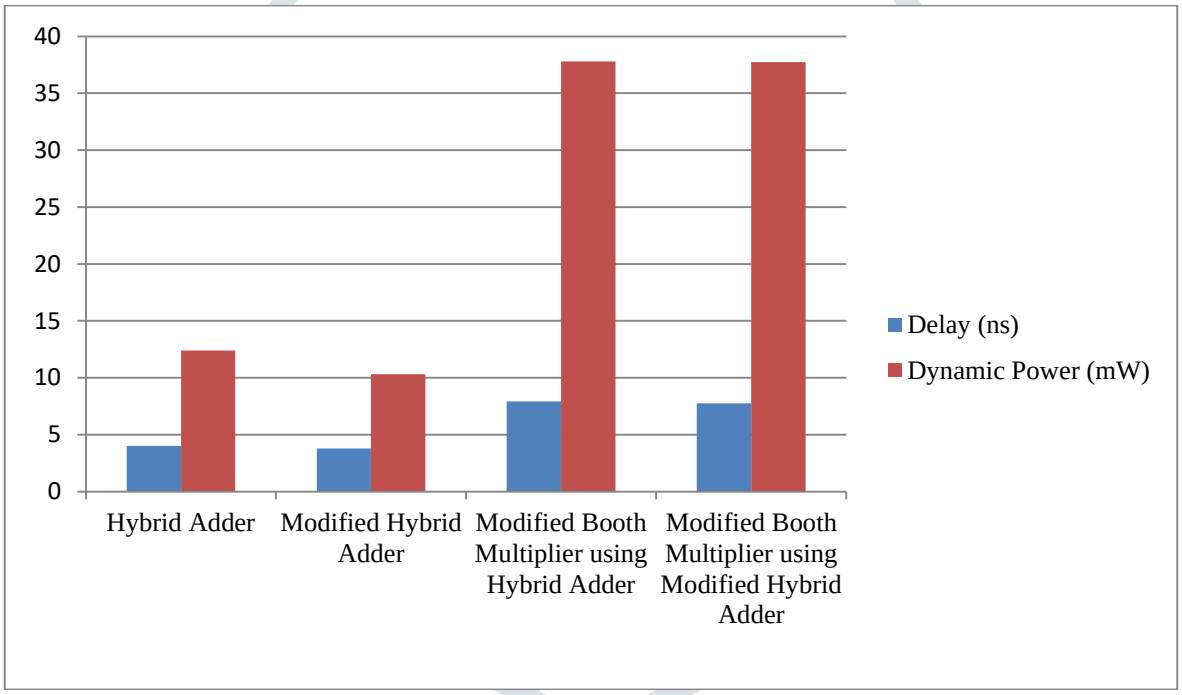

Fig 7: Comparison of Delay in Terms of (ns) and Power in terms of (mW)

VIII. CONCLUSION

In this Paper, Modified Booth Multiplier using Modified Hybrid Adder is proposed. Modified hybrid adder has less delay, less chip Area and low power as compared to hybrid adder. The architecture from conventional design has more power consumption, more chip Area and more delay. But in Proposed design has low power, less chip area and improvement in delay.

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