

Design of a Reversible 6-bit Reversible Unsigned Square Root using Modified Restoring Algorithm

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Abstract - A need for low power ICs arises to keep the power density of ICs within tolerable limits. While the power dissipation increases linearly with advanced version processors, the power density also increases exponentially, because of the ever shrinking size of the integrated circuits. Reversible logic is emerging as an important research area in the recent years due to its ability to reduce power dissipation, which is the main requirement in low power digital design. In this work, a reversible 6 bit reversible unsigned square root is proposed using modified restoring algorithm. In this design we try to reduce optimization parameters like power consumption and quantum cost. The experimental results obtained for implementation in Xilinx ISE 14.2 shows the considerable reduction in terms of Quantum Cost & Power consumption in comparison with the existing design using conventional gates.

Keywords - Low Power digital design, Reversible Logic, Floating-point square root, Power Consumption.

I. Introduction

Researchers in academia and industry believe that Moore's law is ending, and even newly delivered deep-submicron transistors are not significantly more efficient than their previous generations [1]. Therefore, new computing paradigms should be investigated in order to overcome the predicted performance wall which will be reached in 2020 [1].

Conventional irreversible logic gates like two input AND, OR, NOT map two-bit input state to one-bit output state. Erasure of one bit and impossible to construct input from output consequently leads to energy loss. To avoid such energy loss two input states can be mapped to two output states so that input states can be uniquely recovered from output states and under such circumstances, a gate is said to be reversible. Reversible logic gates differ from Conventional irreversible logic gates as they don't permit feedback. The optimized reversible logic circuit consider various metrics like quantum cost, ancillary input lines, garbage output lines.

The quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V+ and CNOT gates from NCV gate library and integrated qubit gates. Integrated qubits are a combination of Feynman gate and either controlled V or controlled V+ gate. Quantum cost of integrated qubit gate as well as 1*1 and 2*2 is one.

The output lines which are not required but deliberately need to be added to maintain reversibility criterion of a reversible gate are known as Garbage Outputs. Garbage outputs are always undesired in any reversible circuit.

Sometimes constant values 0 or 1 are deliberately applied to maintain reversibility criterion of a reversible gate. These constant values are also called as Ancillary Input lines. Ancillary inputs are also undesired in any reversible circuit.

The objective of this paper is to implement and comparatively analyze the proposed modified restoring technique using Reversible Controlled-Subtract-Multiplex block having reduction in quantum cost and power consumption. To bring down the quantum cost optimized Reversible controlled- subtract-multiplex blocks are introduced in the proposed work.

II. The Modified-Restoring Square Root Algorithm

An improved classical non-restoring algorithm proposed in [7] uses the binary digits "01" or "11" and utilizes either add or subtract as the main building block. In [8], a further improved technique is proposed in which only the digit "01" is used and it employs subtract as the main block. The number of stages involved in calculating the square root using this modified approach is 'n' for odd number of bits and 'n/2' for even number of bits where 'n' represents the number of bits. The following are the steps involved in calculating the fixed-point square root using modified non-restoring technique as proposed in [8].

1) Let the n-bit input radicand 'R' and the n-bit result root 'U' be represented as $R_{n-1} R_{n-2} \dots R_0$ and $U_{n-1} \dots U_0$.

2) Divide the significand 'R' into two groups exactly at the decimal point in both directions.

3) **Case i)** If 'n' is an odd number, $R_1 = R_{n-1}$.

During the 1st iteration, i.e. $i = 1$, let $S_i = R_1 - 01$. If the result is positive, then root obtained U_{n-i} is 1 else it is 0.

For $i = 2$ to n do Shift the input radicand 'R' by one bit and select R_1 again.

$$S_i = \{D, R_1\} - \{U [n-1:n-i+1], 01\}$$

Where 'D' represents the remainder of (i-1)th iteration if the result of subtraction is positive else 'D' represents the previous input of subtraction. The square root is U_{n-i} .

4) **Case ii)** if 'n' is an even number, $R_1 = R_{n-1} R_{n-2}$

During the 1st iteration, i.e. $i = 1$, let $S_i = R_1 - 01$. If the result is positive, then root obtained i.e. $U_{(n/2)-i}$ is 1 else it is 0.

For $i = 2$ to $n/2$ do Shift the input radicand 'R' by two bits and select R_1 again. $S_i = \{D, R_1\} - \{U[(n/2)-1 : (n/2)-i+1], 01\}$ where 'D' represents the remainder of (i-1)th iteration if the result of subtraction is positive else 'D' represents the previous input of subtraction. The square root is $U_{(n/2)-i}$.

5) End.

In steps 3 and 4, let Bout be the borrow-out of full subtractor operation

$$S_i = \{ D, R \} - \{ U[n-1 : n-i+1], 01 \}.$$

Bout can be expressed as $Bout = a'b + bc + a'c'$ and 'U' is the square root. If the result of subtraction is negative then Bout is 1. If the result of subtraction is positive then Bout is 0. If Bout = 1, U = 0 then $D = a - b$ -else if Bout = 0, U = 1 then $D = a$ where 'a' represents the previous remainder.

This can be expressed as $D = Ua + U'(a - b - c) \dots \dots \dots (1)$

On simplification, $D = Ua + U'(a \oplus b \oplus c) \dots \dots \dots (2)$

$$D = Ua + U'(a'b'c + a'bc' + ab'c' + abc) \dots \dots \dots (3)$$

From Eq. (3), it is clear that a Multiplexer is required as one of the blocks to determine the input to carry out the subtraction process for the next stage. Thus, multiplexer and subtractor are used as the basic building block in this algorithm. Hence, a Reversible Controlled-Subtract-Multiplex (RCSM) is proposed for the square root implementation.

III. Modified Reversible Controlled-Subtract-Multiplex

To realize a reversible full subtractor, TR gates are used. To implement a reversible multiplexer, Modified Fredkin gate is used. To copy the signal, Feynman gate is used. The quantum cost of the Feynman gate is 1, the quantum cost of the TR gate as a full subtractor is 6 and the quantum cost of the Modified Fredkin gate is 4. Thus, the quantum cost of the proposed Reversible Controlled-Subtract-Multiplex is 11. Fig. 1 shows the symbolic representation of a Modified Reversible Controlled-Subtract-Multiplex.

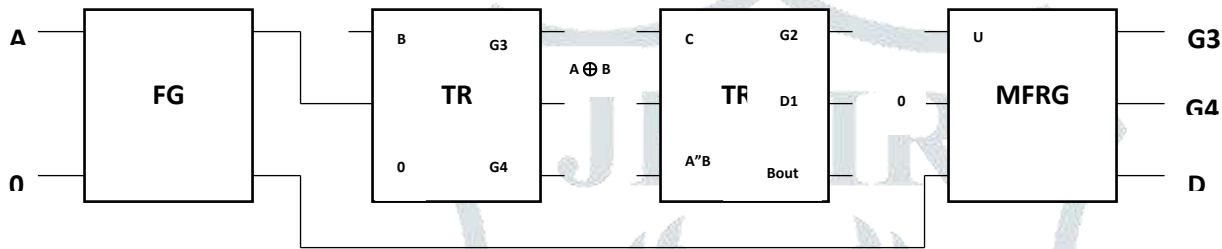


Fig. 1. Symbolic representation of a reversible controlled-subtract-multiplex

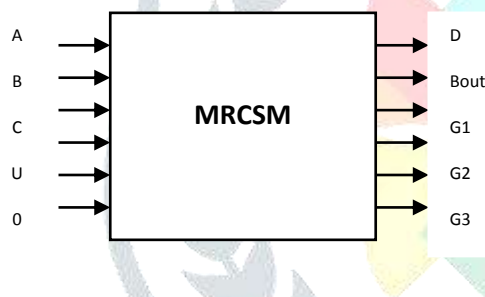


Fig. 2. Block representation of a reversible controlled-subtract-multiplex

In Fig. 1, the input 'A' is copied by feeding the second input as '0' in Feynman gate FG. Then two TR gates are used to realize a full subtractor. The signal D1 represents the difference and Bout represents the borrow-out. Lastly, a Modified Fredkin gate is used to realize a multiplexer. If the signal 'U' is 1, then D represents the previous remainder i.e. the input 'A' else D represents the current remainder 'D1' i.e. $a - b - c$. G1, G2, G3 and G4 represents the garbage output. Fig. 2 shows the block representation of a Reversible Controlled- Subtract-Multiplex.

Thus, the Reversible Controlled-Subtract-Multiplex (RCSM) accepts four primary inputs A, B, C and U and two constant inputs. It produces two output signals, difference D and borrow out Bout along with four garbage outputs.

IV. Realization of Proposed 6-bit Reversible Unsigned Square Root

In the fig. 3, MRCSM represents the Modified Reversible Controlled-Subtract Multiplex block and FG represents the Feynman gate which is used to produce the true and complement form of the input signal. At certain places of the design, the Feynman gates are represented in a reverse manner (flipped) for easy representation. As it is a 6 bit reversible unsigned square root it make use of 6 inputs, input radicand be an unsigned 6-bit number $N_5, N_4, N_3, N_2, N_1, N_0$ in which N_5 is the MSB and does not represent the sign bit.

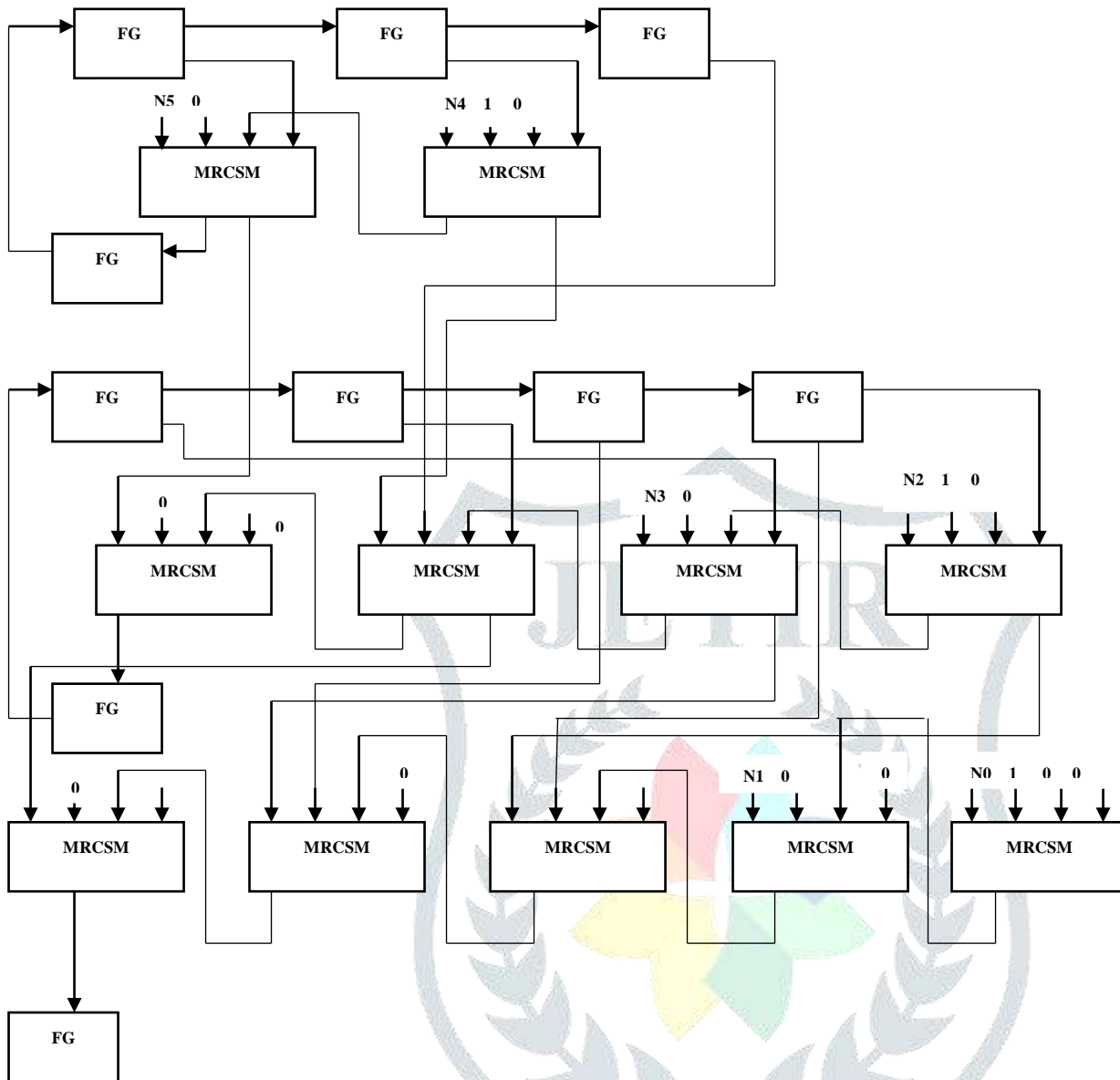


Fig. 3. Realization of Proposed 6-bit reversible unsigned square root

From Fig. 2, it is clear that each MRCSM block produces 4 garbage outputs. As 11 MRCSM blocks are used in the realization, 44 garbage outputs are produced. Along with G1, G3, the unused outputs of the MRCSM block, thus a total of 46 garbage outputs are produced. Each MRCSM block internally uses 4 reversible gates and in addition to MRCSM, 10 Feynman gates are used. Thus, a total of 54 reversible gates are required for the realization.

The quantum cost of each MRCSM block is 11 and the quantum cost of Feynman gate is 1. Since a total of 11 RSCSM and 10 Feynman gates are used, the quantum cost to realize the reversible 6-Bit unsigned square root is 131 which is less than the existing design. The following figure shows the Proposed 6-bit Reversible Unsigned Square Root architecture.

V. Implementation & Results

Table1: Comparison of Proposed work with Existing work

Circuit Name	Quantum Cost	Power Consumption (W)
Proposed 6-bit Square RootDesign [Fig. 3]	131	1.332 W
6-bit Square Root Design [15]	142	2.400 W

VI. Simulation Methodology

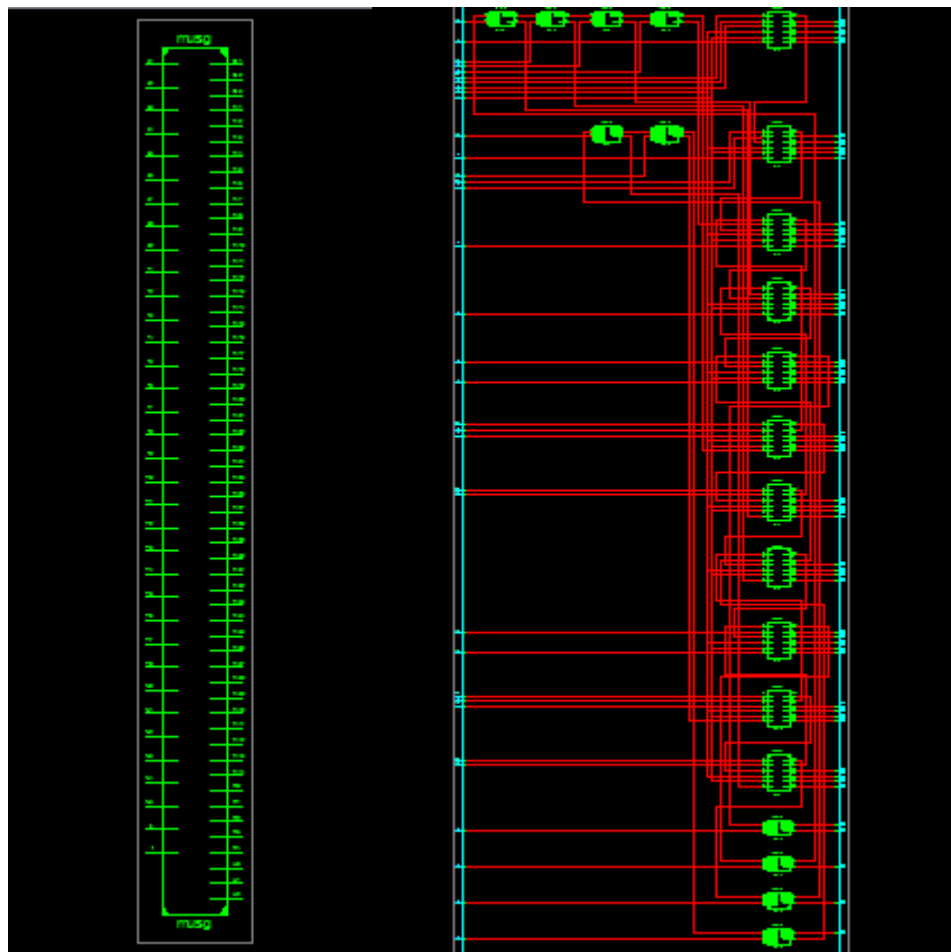


Fig. 4 RTL view of proposed 6-bit Reversible Unsigned Square Root circuit

The performance of the proposed design is verified by simulation using Xilinx ISE 14.4. The results obtained from the simulation for Proposed 6-bit Reversible Unsigned Square Root architecture is verified and shown in the fig. 4. The fig. 4 shows the RTL schematic of top module for our proposed 6-bit Reversible Unsigned Square Root architecture using MRCSM & FG gates.

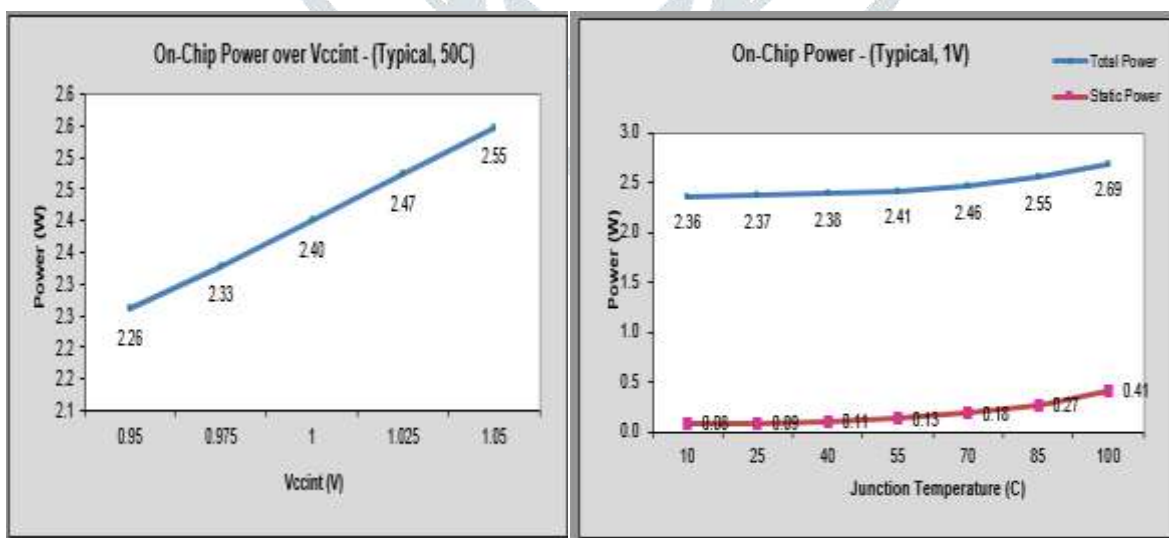


Fig. 5 Power Consumption Graph of Existing 6-bit Reversible Unsigned Square Root Circuit [15]

Fig. 5 shows that the maximum consumed power observed from 6-bit Reversible Unsigned Square Root Circuit using RCSM and Feynman gate is 2.40 W

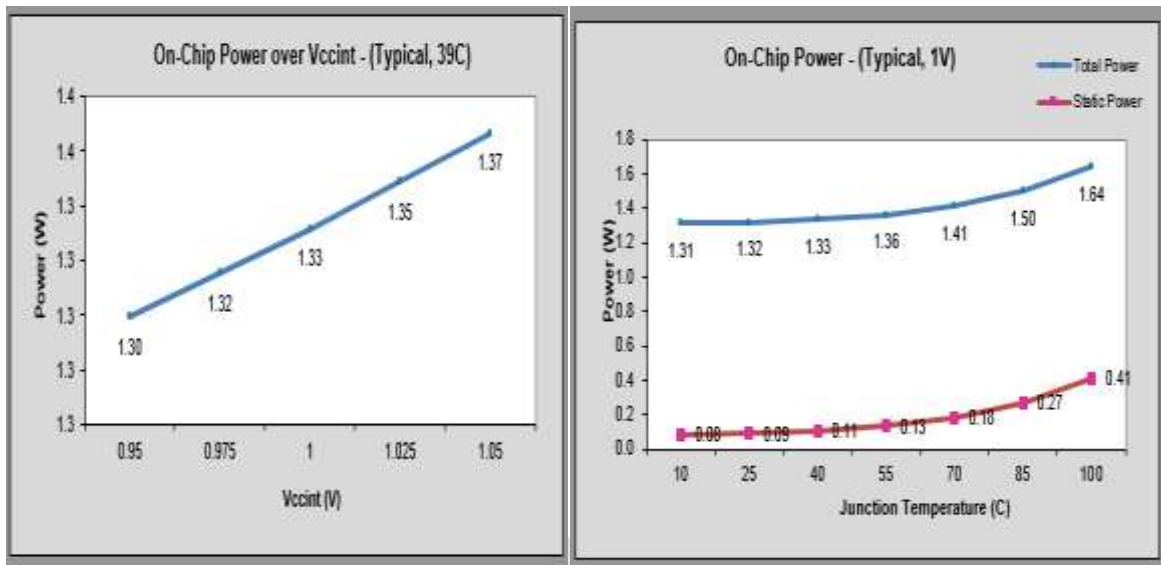


Fig. 6 Power Consumption Graph of Proposed 6-bit Reversible Unsigned Square Root Circuit

Fig. 6 shows that the maximum consumed power observed from 6-bit Reversible Unsigned Square Root Circuit using MRCSM and Feynman gate is 1.33 W

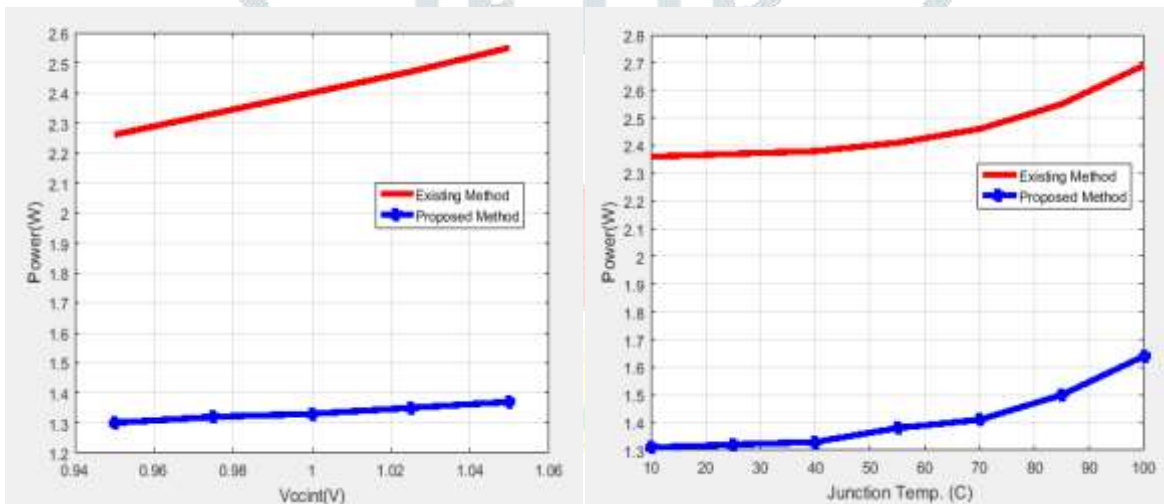


Fig. 7 Comparative Results of Power Consumption Graph for Proposed & Existing 6-bit Reversible Unsigned Square Root circuit [15]

In the fig. 7 the graph between the Vcc and Output power shows that the proposed design consumes 1.33 Watt power while the existing design consumes 2.40 Watt power. Similarly the graph between the Junction Temperature and Power shows that the propose design consumes 1.33 Watt power while the existing design consumes 2.40 Watt power.

Hence it can be concluded that the proposed circuit consumes less power as compared to the existing 6-bit Reversible Unsigned Square Root circuit.

VII. Conclusion

An efficient Reversible 6-bit Reversible Unsigned Square Root circuit is implemented using the Modified Non-Restoring algorithm. Optimized Modified Reversible Controlled- Subtract-Multiplex block is introduced in order to minimize the quantum cost of the circuit. The proposed Reversible 6-bit Reversible Unsigned Square Root circuit is efficient in terms of power consumption and quantum cost. The proposed design has less power consumption & quantum cost when compared to the existing design. Due to its merits, this design can be used for the realization of several signal-processing algorithms that require the square root operation.

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