Design and Implementation of a 6-bit low-power TIQ flash ADC using fat-tree encoder

1Gawas Santoshi Shyamsundar, 2Sunil M P
1M.Tech Scholar-ESD, 2Assistant Professor
1, 2Department of Electronics & Communication Engineering, 1, 2 School of Engineering and Technology, Jain University
Bangalore, India

Abstract: Flash type Analog-to-Digital Converters (ADCs) are the most desired ones for high speed and low to medium resolution applications because of low latency and high data rate. For high speed applications flash and pipeline ADCs are often used. The flash type is the faster of two but limited to lower resolution and consumes more power due to a large number of components. Conventional Flash ADC consists of: a) 2N resistor string, b) 2N ~ 1 comparators, and c) thermometer to binary encoder. In this research work, a 6-bit low power Flash ADC with high conversion rate in 90 nm technology has been designed. Design of circuit and simulations are carried out in Cadence tool virtuoso platform. The utilization of an inverter as a voltage comparator is the explanation behind the strategy’s name – Threshold Inverter Quantization (TIQ). The inverter switching threshold voltage Vm is characterized at Vin = Vout point on the voltage transfer curve of an inverter. In the TIQ comparator, the Vm is interior to the inverter, altered by the transistor sizes. The parallel output through the comparator array is called as thermometer code. After the comparators produce a thermometer code (TC), the thermometer code to binary code (TC-to-BC) encoder generally changes over it to a binary code (BC) in two stages. The TC is changed over to a 1-out-of-n code using ‘01’ generator before coding into BC.

Index Terms - Flash, TIQ Comparator, ADC, CMOS, 6-bit

I. INTRODUCTION

Analog-to-digital converters (ADCs) are utilized to change over analog signals into digital representations of those signals. Digital signal processing can then proficiently separate data from the signals. At whatever point we require the analog signal back, digital-to-analog converter (DAC) is utilized. ADCs are fundamental to numerous present day frameworks that require the combination of analog signals with digital systems. The utilizations of digital system can go from sound engineering to communications applications to restorative applications. These converters are implemented utilizing an assortment of architectures, sizes and speeds. The interest for the converter is situated on area, power, and speed of the converters.

A direct-conversion ADC or flash ADC has a set of comparators examining the information signal in parallel, in which every comparator firing for their decoded voltage range. Since flash ADC is working in parallel transformation strategy, greatest operating frequency in the range of gigahertz (GHz) is achievable. Flash ADC is the speediest ADC in examination with other ADC architectures available. Therefore flash ADC is the best decision in high-speed low resolution applications. Flash ADC is exceedingly utilized in the applications such as high speed instrumentation, digital oscilloscopes, radar, optical communications and high data rate links. The speed of an ADC is additionally influenced by the kind of solid-state technology used to actualize the converter. Three different kinds of solid-state technologies are accessible for fast ADC implementation: the CMOS technology, the bipolar technology, and the Gallium Arsenide (GaAs) technology. The GaAs technology is the speediest of the three and the CMOS technology is the slowest. The high-speed ADCs are actualized with parallel type architecture utilizing the GaAs technology. The present GaAs technology is not feasible with the silicon based CMOS technology, which makes it extremely hard to realize the single-chip framework arrangement pointed by the present System-on-Chip (SOC) trend. Thus, a high-speed CMOS flash ADC design including the threshold inverter quantization (TIQ) technique with low power consumption is utilized as a part of this project. The TIQ system permits faster analog-to-digital conversion speed utilizing the standard digital CMOS logic hardware favored for SOC usage. The bipolar transistor technology permits speedier operation and it is perfect with the CMOS technology. In any case, the BiCMOS technology requires all the more handling strides and higher cost contrasted with standard digital CMOS technology. Mixed-signal circuit implementation utilizing just the standard digital CMOS technology is the favored decision for the SOC components.

II. LITERATURE SURVEY

Kiran Kumar Lad et.al [1], proposed a 1-V 1-GS/s 6-bit low power flash ADC in 90 nm CMOS technology. In this proposed Flash ADC consists of reference generator, comparator array, 1-out-of N code generator, Fat tree encoder and output D-latches. The proposed ADC consumes 15.75 mW from 1V supply while operating at 1 GS/s. The comparator consists of three stages: a preamplifier stage, a latch and a post amplifier stage. Preamplifier is used in order to overcome dynamic offset in regenerative latch. The latch stage consists of cross coupled pair of NMOS and PMOS transistors that are connected to the ground through the clock enable transistor. The post amplifier stage consists of a self-biased single-ended differential amplifier and two inverters. Fat-tree encoder is used as T-B encoder.

Mohamed O. Shaker et.al[2], proposed a 6-bit flash ADC, with a maximum acquisition speed of 1 GHz, is implemented in a 1.2 V analog supply voltage. The proposed 6-bit flash ADC consumes about 72 mW in a commercial 90 nm CMOS process.
The new design offers lower number of comparators and lower power consumption compared with the traditional flash ADC. The new design uses 10 comparators and 9 multiplexers while the traditional one uses 63 comparators.

Mishra S.N. et.al [3], proposed a power efficient 6-bit TIQ ADC design for portable applications. This paper infers that low power and low voltage requirements are becoming increasingly important issues as the MOSFET channel length shrinks below 0.25 submicron in the digital domain. The high speed and low power ADC design is achieved by using TIQ (threshold inverting quantization) comparator instead of traditional high gain differential comparator, and the decoder is designed using multiplexer instead of traditional ROM decoder. The designed model achieves maximum speed of 1Gsps with 1.23 mw of power consumption.

Chen M.W. et.al [4], proposed a 2GS/s 6-bit flash sub-ADC with an op-amp free track-and-hold (T&H) for use in an 8GS/s 4-way time-interleaved ADC was implemented in 45nm SOI CMOS. The T&H utilizes a passive charge sharing technique and achieves a 4GHz input bandwidth at 2GS/s clock rate without an op-amp. The flash sub-ADC consumes 74mW at 2GS/s and occupies an area of 0.2mm2.

Jincheol Yoo et.al [5], proposed a 1GSPS CMOS flash A/D converter for system-on-chip applications. A 6-bit TIQ based flash A/D converter was designed with the 0.25 µm standard digital CMOS technology parameter. It operates with sampling rate up to 1 GSPS, dissipates 66.87mW of power at 2.5 V, and occupies 0.013 mm2 area. The design uses ROM encoder for TC-BC conversion.

Dhruva Ghai et.al [6], proposed a 6-bit 1 Gs/sec flash analog-to-digital converter (ADC) for low voltage and high speed system-on-chip (SoC) applications, simulated with the 45nm Predictive Technology Model. The Threshold Inverter Quantization (TIQ) technique is used with WPMOS/WNMOS < 1 for many transistors to keep the power consumption as low as possible. It is also observed that the ADC consumes 45.42µW of peak power and 8.8µW of average power at full speed while it operates on a power supply voltage of 0.7V.

Ankush Chunn et.al [7] performed the comparison of T-B encoders for flash ADCs. In this paper different T-B encoders employed in flash ADCs are analyzed in terms of bubble error, delay and power consumption. ROM encoder, Wallace tree, Fat-tree and Multiplexer-based encoder were compared for their performance. This paper concludes that Mux-based encoder is most power efficient, whereas fat-tree has the lowest propagation delay. Mux-based and Wallace tree encoders are less prone to bubble error. So, it is concluded that the Mux-based encoder is better than other encoders with flash ADC.

III. PROPOSED DESIGN

The proposed flash ADC features the threshold inverter quantization (TIQ) method for high-speed and low-power applications using standard CMOS technology. Fig.1 demonstrates the block diagram of the TIQ flash ADC. The utilization of two cascading inverters as a voltage comparator is the reason behind the method’s name. The voltage comparators compare the input voltage with internal reference voltages of the respective comparators, which are dictated by the transistor sizes of the inverters of the comparators. Consequently, we needn't bother with the resistor ladder circuit utilized as a part of a conventional flash ADC. The gain boosters make sharper thresholds for comparator outputs and give a full digital output voltage swing. The comparator yields - the thermometer code - are changed over to a binary code in two stages through the ’01’ generator and the fat-tree encoder as appeared in Fig.1.

![Fig.1. Block diagram of the TIQ flash ADC using the fat-tree encoder](image-url)
IV. DESIGN AND IMPLEMENTATION

A. TIQ Comparator

The comparator is the most critical part in the design of an ADC. Its role is to change over an information voltage (V_{in}) into a logic ‘1’ or ‘0’ by comparing a reference voltage (V_{ref}) with the Vin. Output of the comparator is ‘1’, if V_{in} is greater than V_{ref}, otherwise ‘0’.

Usually utilized comparator structures as a part of CMOS ADC design are the fully differential latch comparator and dynamic comparator. The former is now and again called a "clocked comparator", and the latter is known as an “auto-zero comparator” or “chopper comparator”.

The TIQ comparator utilizes two cascaded CMOS inverters as a comparator for high speed and low power consumption. The inverter threshold (V_{m}) is characterized as the Vin = V_{out} in the voltage transfer curve (VTC) of an inverter. Mathematically,

\[ V_{m} = \left[ r \left( V_{DD} - |V_{Tp}| + V_{Tn}\right) \right] \bigg/ \left( 1 + r \right) \]

where \( r = \sqrt{K_p/K_n} \) .......(1)

Where, \( V_{Tp} \) and \( V_{Tn} \) represent the threshold voltages of the PMOS and NMOS transistors, respectively. Fig.2 demonstrates the schematic of an inverter and its VTC from the simulation. At the first inverter, the analog input signal quantization level is set by inverter threshold (V_{m}) depending upon the W/L ratios of PMOS and NMOS transistors. The second inverter is utilized to increase voltage gain and to prevent an uneven propagation delay. In Fig.2.b, the slope of Vout is indicated larger than the slope of Vout1. The inverter threshold relies on upon the transistor sizes. The inverter VTC Va and Vb demonstrate the difference from the VTC of Vout. With a fixed length of the PMOS and NMOS transistors, we can get wanted estimations of Va and Vb by changing just the width of the PMOS and NMOS transistors, respectively. This outcome can be affirmed by the accompanying equation of the inverter threshold Vm.

\[ V_{m} = \left[ \sqrt{\mu_p*wp}/(\mu_n*wn) \left( V_{DD} - |V_{Tp}| + V_{Tn}\right) \right] \bigg/ \left( 1 + \sqrt{\mu_p*wp}/(\mu_n*wn) \right) \] .......(2)

Where ‘\( \mu_p \)’ and ‘\( \mu_n \)’ are the electron and the hole mobilities of the PMOS and NMOS devices. To derive equation 2, we consider that both transistors are in the active region, the gate oxide thickness (Cox) for both transistors is the same, and the lengths of both transistors (Lp and Ln) are same. From equation 2, we realize that Vm is moved depending on the transistor width ratio (Wp/Wn). That is, expanding Wp makes Vm bigger, and expanding Wn results in Vm being smaller on the VTC.

This varying of the widths of the PMOS and NMOS devices with a fixed transistor length is the real trick of the TIQ comparator. We can utilize the inverter threshold voltage Vm as an internal reference voltage to compare the input voltage. A TIQ comparator basically uses the VTC of an inverter as depicted in Fig.3.a. By changing its transistor sizes, the threshold voltage Vm can be changed. Fig.3 demonstrates the comparison of the TIQ comparator with a differential voltage comparator used in a conventional flash ADC. The circuits are distinctive however the VTCs are comparative.
The mathematical expression used for deciding the switching voltages of comparator is given as:

\[ V_{th} = \frac{\sqrt{\mu_p W_p (V_{DD} - |V_{tp}|) + V_{tn}}}{1 + \sqrt{\mu_n W_n}} \]

Where, \( W_p \) = PMOS width, \( W_n \) = NMOS width, \( V_{DD} \) = supply voltage, \( V_{tp} \) = PMOS threshold voltage, \( V_{tn} \) = NMOS threshold voltage, \( \mu_n \) = electron mobility, \( \mu_p \) = hole mobility.

We fix the length of both the PMOS and NMOS transistors at a constant size, and different inverter switching threshold voltages \( (V_{th}) \) is obtained by varying width of PMOS and NMOS increasing \( W_p \) makes \( V_{th} \) larger, and increasing \( W_n \) results in \( V_{th} \) being smaller on the VTC.

<table>
<thead>
<tr>
<th>Wp</th>
<th>Wn</th>
<th>Lp</th>
<th>Ln</th>
<th>Vth</th>
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<tbody>
<tr>
<td>180nm</td>
<td>400nm to 12.5um</td>
<td>10.4um to 400nm</td>
<td>360nm</td>
<td>477mV to 1.1 V</td>
</tr>
<tr>
<td>90nm</td>
<td>180nm to 800nm</td>
<td>600nm to 180nm</td>
<td>180nm</td>
<td>347mV to 530 mV</td>
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Fig. 5. DC parametric sweep of the 6-bit TIQ comparator array

B. ‘01’ Generator

Changing over thermometer code into binary code is one of the principle design issues of any flash ADC. After the comparators produce a thermometer code (TC), the thermometer code to binary code (TC-to-BC) encoder generally changes over it to a binary code (BC) in two stages. The TC is changed over to a 1-out-of-n code using ‘01’ generator before coding into BC. The TC is changed over to the 1-out-of-n code, utilizing XOR logic. The 1-out-of-n code has stand out ‘one’, the rest are ‘zeroes’. The point where the code changes from one to zero is the point where the input signal becomes smaller than the corresponding comparator reference voltage levels.

Fig. 6. Block diagram of ‘01’ generator

The TC is changed over to 1-out-of-N code utilizing an array of NOT and AND gates as shown in Fig.6. This NOT-AND array is realised utilizing NOT and NOR gates. This 1-out-of-N code is bolstered to a fat tree encoder, which changes over it into a binary code.

C. Fat-tree Encoder

The TC-to-BC encoding is done in two steps in the fat-tree encoder: the primary stage changes over the thermometer code into 1-out-of-N code. The 1-out-of-N code is same as an address decoder output. This code conversion is carried out in N bit parallel utilizing N gates. Fig.8 demonstrates the two-stage fat tree TC-to-BC encoder.
Fig. 7. A fat-tree encoder

Fig. 8. Two-stage fat-tree TC-to-BC encoder

The second stage changes over the 1-out-of-N code into BC utilizing the multiple trees of OR gates. Fig. 7 demonstrates a case of a 4-bit ADC. A 16-bit 1-out-of-N code is introduced to the leaf nodes of the tree and 4-bit BC yield is delivered at the root nodes of the trees. As the tree height increments, an edge count of node increases - so it is named a fat tree.

Algorithmically, the fat tree circuit signal delay is $O(\log_2 N)$ whereas the ROM circuit signal delay is $O(N)$. In addition, the Wallace-tree encoder signal delay is $O(\log_{1.5} N)$. Hence, the fat tree circuit is the quickest speed circuit amongst two-stage TC-to-BC encoders.
**IV. RESULTS AND DISCUSSION**

In 180nm, for the 6-bit ADC; the PMOS transistors widths are chosen between 400nm to 12.5µm and that of NMOS transistors is chosen between 10.4µm to 400nm. The lengths of both transistors are fixed to 360nm. The threshold voltages are obtained between 477mV to 1.1V. In 90nm, for the 6-bit ADC; the PMOS transistors widths are chosen between 180nm to 800nm and that of NMOS transistors is chosen between 600nm to 180nm. The lengths of both transistors are fixed to 180nm. The threshold voltages are obtained between 347mV to 530mV.

The total power consumption of the 6-bit flash ADC using the fat-tree encoder is 997.7mW in 180nm, and 519.9mW in 90nm. The delay is 993.2ns in 180nm, and 646.8ns in 90nm.

<table>
<thead>
<tr>
<th>Encoder</th>
<th>Power in 180nm</th>
<th>Power in 90nm</th>
</tr>
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<tbody>
<tr>
<td>Fat-tree</td>
<td>997.7mW</td>
<td>519.9mW</td>
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The TIQ flash ADC offers higher data conversion rates while maintaining a comparable power consumption level.
CONCLUSION AND FUTURE SCOPE

The fat tree encoder overcame the speed limitation of the ROM type encoder, which is the bottleneck of high speed ADCs. Mux-based encoder greatly reduces the transistor count compared to other encoders. Mux-based encoder is most power efficient, whereas fat-tree has the lowest propagation delay. Automatic generation of fat-tree encoder. Modify the Mux-based encoder to get lesser fan-out in critical path. Redundant comparator structure using TIQ technique might be designed.

REFERENCES