Efficient Design and Analysis of Super-Regenerative Receiver using CMOS Technology for Short Range Communication

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Abstract

Super-regenerative receiver (SRR) is employed in wireless communication, having low power consumption, low lost and high signal to noise ratio. In this paper low voltage SRR is designed operating at higher frequency for short range communication. Proposed SRR consists of three circuits, first one is low noise amplifier (LNA), which is used as impedance matching between the RF signal and super-regenerative oscillator (SRO) second one is super regenerative receiver which controls the gain and third one is an envelope detector (ED) which provide the envelope output. The receiver framework is very simple and highly efficient for the use of short range communication. Proposed SRR is designed in 0.18 μm CMOS technology in the cadence virtuoso. Experimental results shows proposed SRR have low power consumption of 0.0029 W at 1 volt power supply.

Key index: Envelope detector (ED), Low noise amplifier (LNA), Super-regenerative Oscillator (SRO).

I. Introduction

Super-regenerative plays an important role in the field of short range communication which make new ideas for interconnections like wireless sensor networks and personal area networks. There are several applications like clinical diagnosis, wild life monitoring and so on of these networks. It can be easily produced because of highly integrated so these networks have low cost [1-6]. For this kind of system low power is an important factor because of bulky batteries and deployment of short-term sensors is not acceptable. A wireless transceiver which is a critical parameter provides communication connection between distributing of nodes which minimizing overall cost and power consumption tends to global cost and saving of power, portability and enhanced lifespan of field deployed sensors [5-8]. To analyses the possibility of minimizing power consumption of a super regenerative receiver by utilization of super-regeneration principle. SRR is a deigned for short range communication because it's having less power consumption and simplicity of architecture. It is also used for low & medium data rate and wireless sensor network applications. In the super-regeneration radio frequency signal is amplifying from the pre setup of oscillations [9],[10]. For the applications of low power and low complexity, super regenerative (SRR) are very useful devices due to its simple design and having less power consumption. To exhibit the workability of super-regenerative receiver from the principle

of super regeneration, a regenerative receiver is designed using CMOS technology in 0.18 micro meter at 60 GHz

II. Proposed Work

Super regenerative receiver is plays an important role in the field of wireless communication which is employed in data transfer between hard drives, MP3 and MP4 players and HD (High definition) video receivers. In this work, we presented a novel super regenerative receiver having high data rate at higher frequency of 60 GHz using the 0.18 μm CMOS technology, which provide a very low consumption. The framework of proposed super regenerative receiver is shown in fig 1. The proposed circuit is shown in fig.2 implemented in cadence virtuoso.

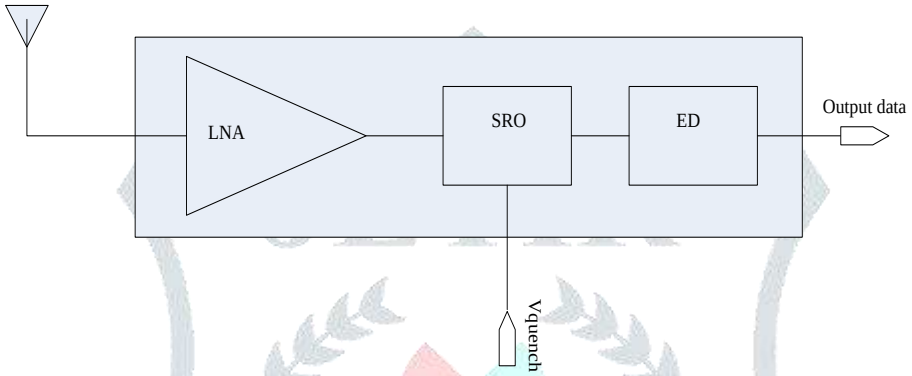

Fig.1 Super-regenerative receiver block diagram

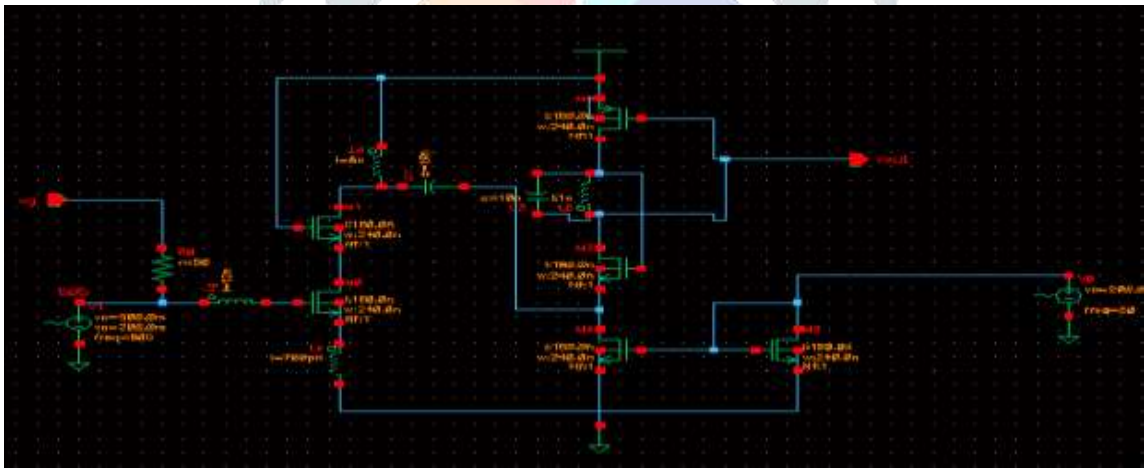

Fig. 1 Structure of Super regenerative receiver

Proposed circuit consist of three section: first one is low noise amplifier which amplifies incoming RF signal and then it is injected into the oscillatory nodes of the super regenerative oscillator, second one envelope detector which provides envelope for the original signal and the third section is super regenerative oscillator (SRO) which is main function of the Super regenerative receiver that can be handled by a low frequency generator called quench generator.

A. Low Noise Amplifier

The low noise amplifier deals many functions in SRR front-end. Firstly it amplifies the received poor Radio Frequency signal to a prescribed level so that noise in following stages is relatively insignificant. Then it

performs as an impedance matching network between the antenna and the super regenerative oscillator and then it protect the high-power oscillation of super regenerative oscillator through coupling back into the antenna. The schematic diagram of low noise amplifier is shown in fig 3.

Fig.3 Schematic test bench for Low Noise Amplifier

Low noise amplifier provides a buffer between the antenna and oscillator. In the fig. 3 schematic test bench for low noise amplifier is designed through cadence virtuoso having port zero at the input voltage and port one at the output voltage. The simulation results for the test bench of LNA is shown in fig.4 defines the S-parameter analysis described small signal gain (S_{21}, G_A, G_T, G_p), small signal stability, small signal noise and input-output matching are simulated.

B. Super Regenerative Oscillator

Super regenerative oscillator which is main function of the super regenerative receiver that can be handled by a low frequency generator called quench generator. This controls the gain of the SRO. The schematic design of Equivalent RLC circuit for the super regenerative oscillator is shown in fig.5

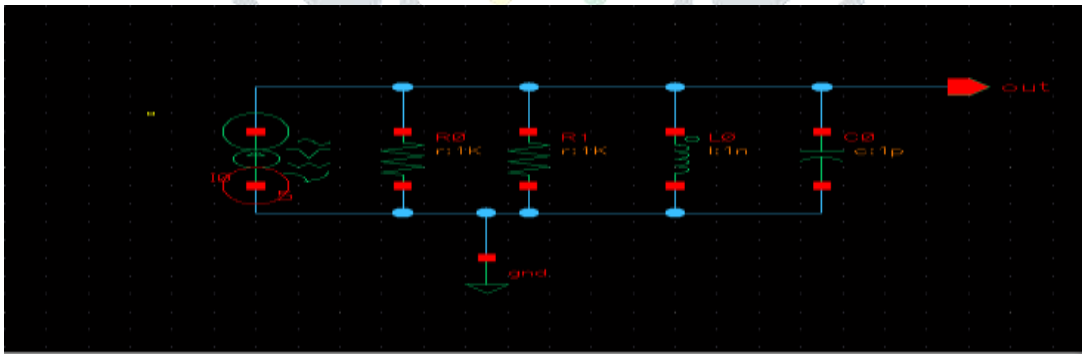

Fig.5 Equivalent RLC circuit for super regenerative oscillator

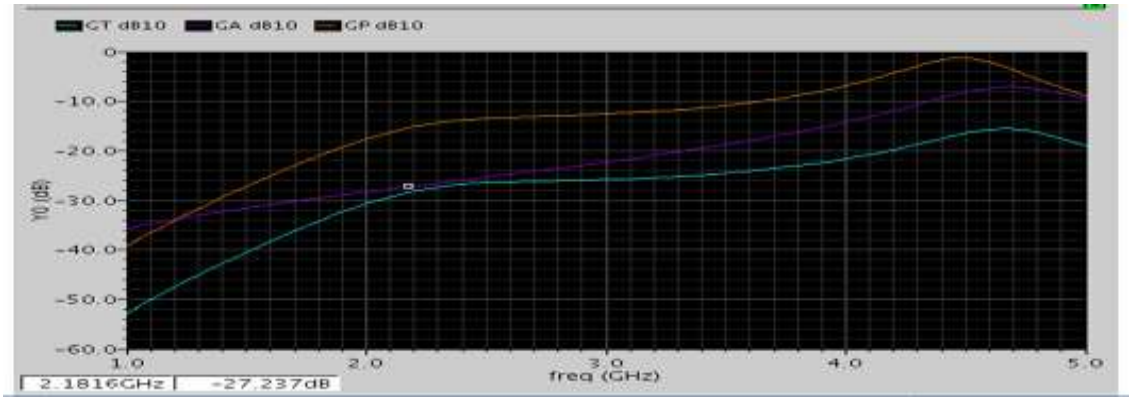

Fig 4 Small signal gain for low noise amplifier test bench

C. Envelope Detector

In the proposed circuit envelope detector is designed through CMOS and capacitor in which high frequency signal is provided as input and it produces enveloped output of the signal. Here in the rising edge capacitor store the charges in the form of voltage and then transfer the stored charges slowly through resistor during falling edge.

III. Simulation Results

Figure 4 shows the equivalent RLC circuit of the SRO and simulated result for the SRO which is implemented in the CADENCE Tool. Figure 5 shows the Simulated Transient response and spectral power wave of SRO. Figure 6 and 7 shows Simulated Noise response of SRO and Frequency of the SRO respectively

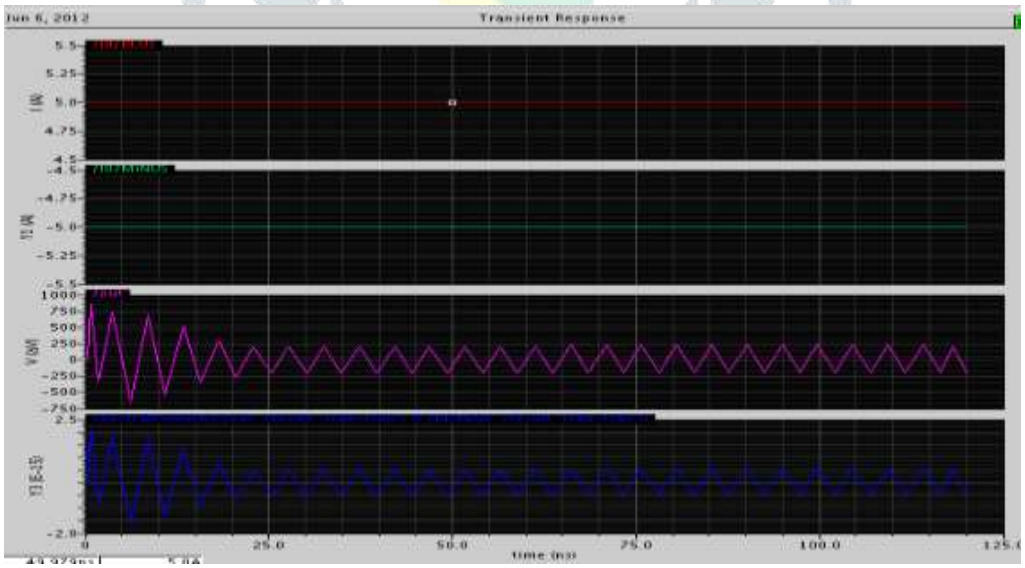

Fig. 5 Transient response and spectral power wave of SRO

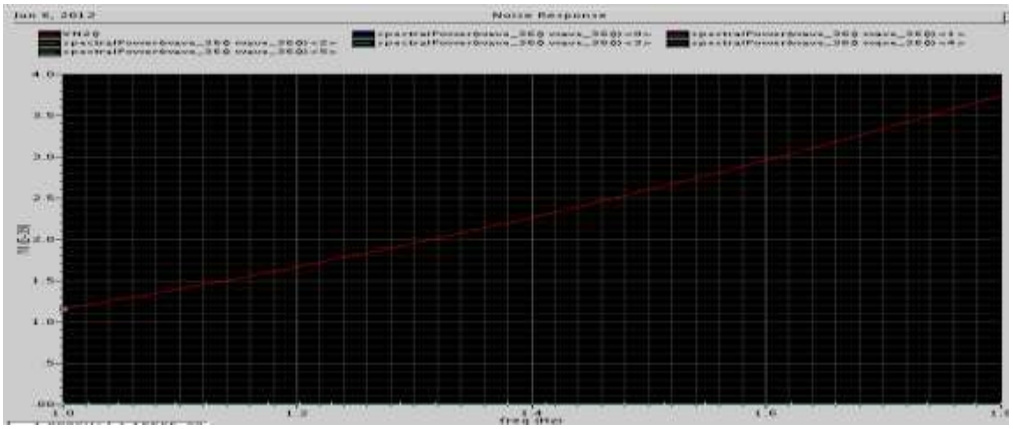

Fig. 6 Simulated Noise response of SRO

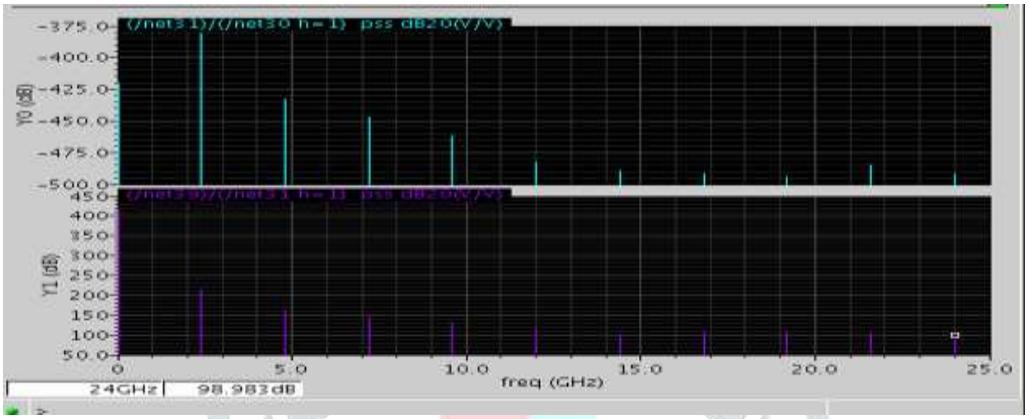

Fig.7 LNA Voltage gain and Harmonic distortion

The simulated setup environment is according to the prototype receiver showing in Figure 1

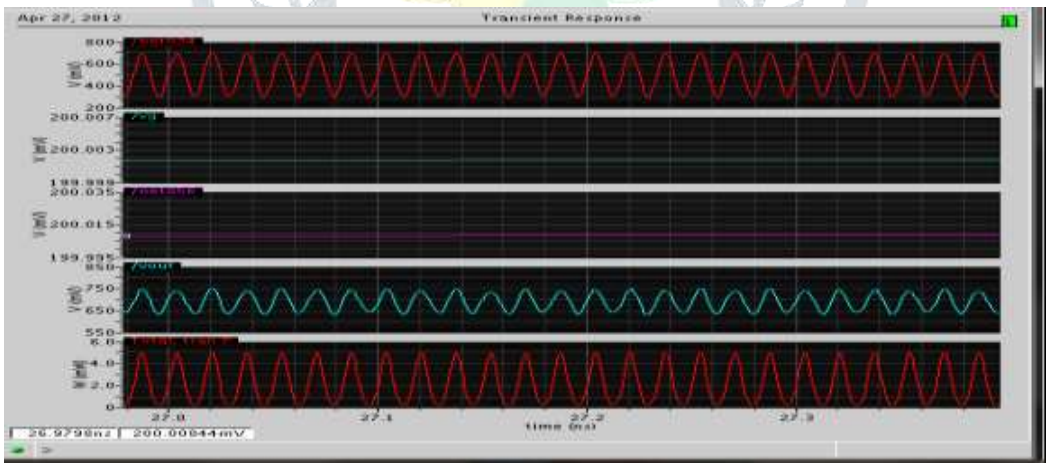

Fig. 8 Simulation results for SRR output

There is an open loop design in the proposed SRR due to this we can manually align signal for getting high data rate. Simulation results of transient analysis for the SRR is shown in fig. 8. The 1st graph is a input signal having 60 Ghz frequency. The SRO was conducted in a fragile region as a detector. As super regenerative receiver explore the consistent input signal then starts to damping. In the simulation result second graph is output waveform. Here envelope detector is proposed for demodulating the signal to the message signal. In

the proposed SRR there is low power consumption of 2.19 mw which obtain a synchronous receiver providing the manual time delay that is 2.4 ns in simulation which is need. Yet, the close loop receiver design is a ordinary solution for getting synchronization. In the Table I, previous implemented design is given for comparison with the proposed work.

Table 1 Previous implemented design for comparative analysis

Reference	CMOS technology	Frequency	DC Power
[1]	0.9 µm	2.4 GHz	206 mw
[2]	0.18 µm	UBW	11 mw
[3]	0.18 µm	UBW	137 mw
Proposed	0.18 µm	60 GHz	2.19 mw

IV. Conclusion

In this paper a new super regenerative receiver have been proposed using 0.18 µm CMOS technology for short range communication and data transfer. The proposed SRR is used very low power at very high frequency and achieves a higher data rate. Because of hangover limitations, noise figure was increased progressively 12 db. The proposed design simulated in high frequency with an acceptable tradeoff between sensitivity, throughput and power consumption.

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