AN EFFICIENT IMPLEMENTATION OF HIGH SPEED, LOW POWER VEDIC MULTIPLIERS USING REVERSIBLE GATES

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Abstract:--*Multipliers are vital components of any processor or computing machine. More often than not, performance of microcontrollers and Digital signal processors are evaluated on the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. It's simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation. Power dissipation is another important constraint in an embedded system which cannot be neglected. In this paper we bring out a Vedic multiplier known as "Urdhva Tiryagbhayam multiplier". The Urdhva Tiryagbhayam literally means .This will be implemented using reversible logic. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications*

The purpose of this project is to implement a 16x16 Vedic multiplier using reversible gates which are operated at very high speed. The functionality of RT is verified by using Xilinx 14.5.

Index Terms: Urdhva Tiryagbhayam, Multipliers.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation-Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications**.** This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier**.**

Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application.

II. Literature Review

Energy loss is an important consideration in digital circuit design. A part of this problem arises from the technological non ideality of switches and materials. The other part of the

problem arises from Landaulet's principle for which there is no solution. Landaulet's Principle states that logical computations that are not reversible necessarily generate k*T*in joules of heat energy, where k is the Boltzmann's Constant k=1.38xlO-23 J/K, T is the absolute temperature at which the computation is performed. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to information lost, which will be a noticeable amount of heat loss in next decade. Also by second law of thermodynamics any process that is reversible will not change its entropy. On thermo dynamical grounds, the erasure of one bit of information from the mechanical degrees of a system must be accompanied by the thermalization of an amount of k*T*in joules of energy.

REVERSIBLE LOGIC

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity.

Feynman Gate:

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.

Peres Gate:

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.

HNG Gate:

It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost six. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.Fig.1 shows the block diagram of reversible logic gates.

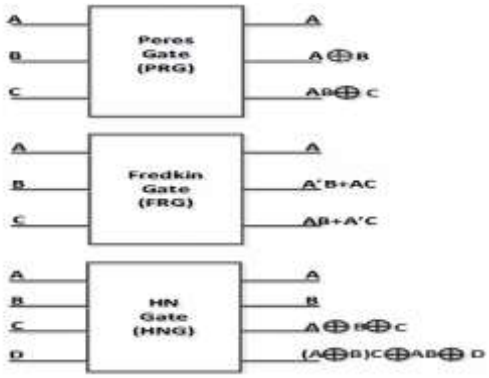

Fig.1: Reversible logic gates

III. PROPOSED ARCHITECTURES.

The proposed reversible Vedic multiplier multiplies two binary numbers and gives 16bit binary output. Peres gate and Feynman gates are used for designing the multiplier. The beauty of UT architecture is the generation of partial products and additions are done concurrently. The proposed Vedic multiplier is design using reversible 2x2 and 4x4 Vedic multiplier as its sub unit. Proposed 2x2, 4x4 and 8x8 and16x16 Vedic multiplier are describes below.

A) 2x 2UT Vedic multiplier

Fig.2 illustrates the steps to multiply two 2 bit numbers. Converting the above figure to a hardware equivalent we have 5 Peres gate and 1 CNOT gate which will act as 2 bit multipliers and half adders to add the products to get the final product. Here is the hardware detail of the multiplier

Here "a" and "b" are two numbers to be multiplied and "y" is the product. With this design we are now ready to code this in virology easily using reversible gates. To make the design more modular we write code for gates first and then instantiate it to have the final product.

The circuit requires a total of six reversible logic gates out of which five are Peres gates and remaining one is the Feynman Gate

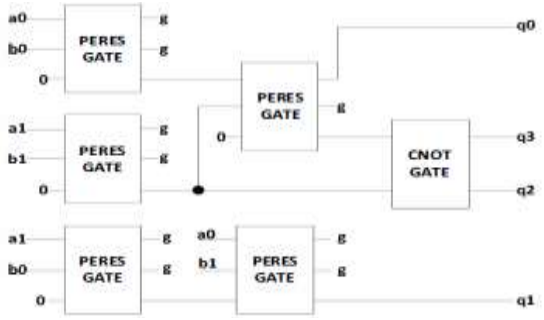

Fig.2: 2x 2UT Vedic multiplier.

B) 4x4UT Vedic multiplier

The block diagram of the 4X4 Vedic Multiplier is presented in the fig.3. It consists of four 2X2 multipliers each of which procedures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder. The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third 2X2 multipliers and output of four bit ripple carry adder are given as inputs to the five bit ripple carry adder. The upper bit output of the five bit ripple carry adder and output from the fourth 2x2 multiplier are final output bits .These bits forms the upper bits of the final result.

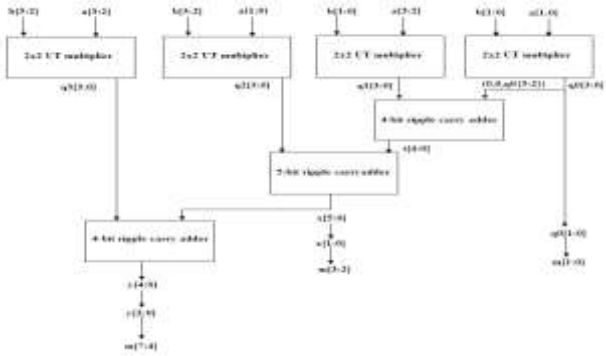

Fig.3: 4X4 UT Multiplier

The ripple carry adder is consummated (realized) using the HNG Gate. The number of bits that need to be ripple carried verdicts the number of HNG gates to be used. Thus a 4 bit ripple carry adder needs 4 HNG gates and the 5 bit adder requires 5 HNG gates. This design also does not take into consideration the fan out gates.

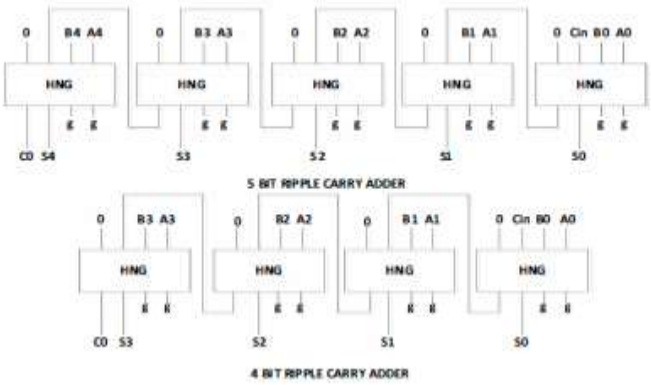

Fig.4: 4 bit and 5 bit Ripple Carry Adders.

C) 8x8UT Vedic multiplier

The block diagram of the 8x8 Vedic Multiplier is presented in the figure.5. It consists of four 2X2 multipliers each of which procedures 16 bits as inputs; 8 bits from the multiplicand and 8 bits from the multiplier. The output of the first 4x4 multiplier are entrapped as the lowest four bits of the final result of multiplication the second 4x4 multiplier output and third 4x4 multiplier are given as input to the ripple carry bit 8 adder. The output from the 8-bit carry adder along with the four zeros are concatenated upper four bits of the output of the first 4X4 multiplier are given as input to the nine bit ripple carry adder the upper four bits are entrapped as the middle bits in the final result. The upper bit output of the nine bit ripple carry adder concatenated with two zeros along with the fourth output of 4x4multiplier gives the final higher output bits. These bits forms the upper bits of the final result.

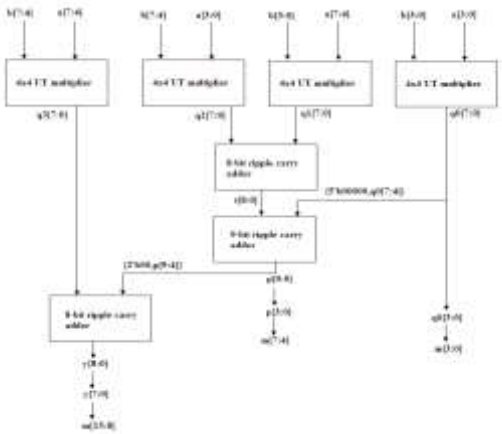

Fig.5:8X8 UT Multiplier.

1)8-bit Reversible Ripple Carry Adder: Reversible adder is proposed using HNG gate. In HNG gate if fourth input, D is made constant zero and inputs is given through A and B and carry to third input C then it act as reversible one bit full adder and output is taken from R and S respectively.

The proposed 8-bit reversible adder is form using HNG gate having two 8 bit inputs and a carry which is propagate from the list significant bit (LSB) to most significant bit (MSB) also known as ripple carry adder. The size of the reversible ripple carry adder is very small and it is very simple to design, so normally ripple carry adders are used for cascading. Each HNG gate act as one bit full adder so total eight HNG gates are required to built 8-bit ripple carry adder. Output is represented as SO-SI and 'g' is the garbage. The 4

bit ripple carry adder is made with same HNG gate n proposed adder total 16 garbage values are produced and having quantum cost of 48. The proposed reversible 8-bit ripple carry adder is shown in the fig.5.

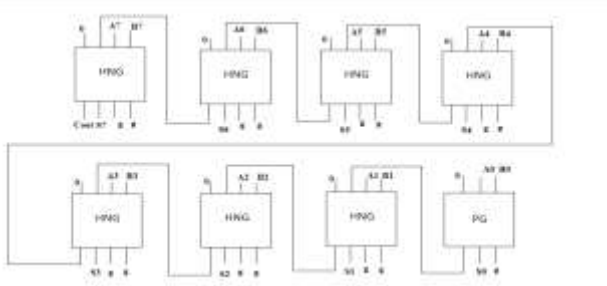

Fig.5: 8-Bit Ripple Carry Adder

D) 16x16 bit Reversible Vedic multiplier:

The reversible 16X16 UT multiplier requires four reversible 8x8 UT multipliers which is shown in Figure-14. The result of first 8x8 reversible UT multiplier whose inputs are b[7:0], a[7:0] forms the LSB's of the final result (y[7:0]). The results of second and third 8x8 reversible UT multipliers q1 [15:0] and q2[15:0] are added using the upper 16 bit reversible ripple carry adder. The sum outputs (q a[15:0]) except carry (C1) of upper 16-bit reversible ripple carry adder, the remaining bits of first 8x8 reversible UT multiplier (q0[15:8]) and LSB bits of fourth 8x8 reversible UT multiplier (q3[7:0]) are applied as a inputs to the lower 16-bit reversible ripple carry adder. The sum outputs of this adder serve as eighth to twenty third bits of the final result (y[23:8]) . The carry bits C1 and C2 of the reversible ripple carry adders are applied to the reversible OR gate. The remaining bits of the final result (y[31:24]) is generated by using eight reversible half adders. The 16-bit Reversible ripple carry adder is designed using 16 HNG gates as shown in Fig.6.

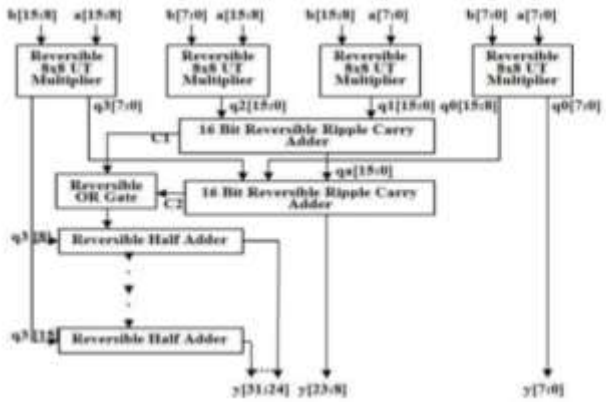

Fig.6:16x16UT Vedic multiplier

1)16- BIT REVERSIBLE RIPPLE CARRY ADDER.

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A propagation delay inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is "0″ the output will be "1″ and vice versa. The time taken for the NOT gate's output to become "0″ after the application of logic "1″ to the NOT gate's input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (C out) signal.

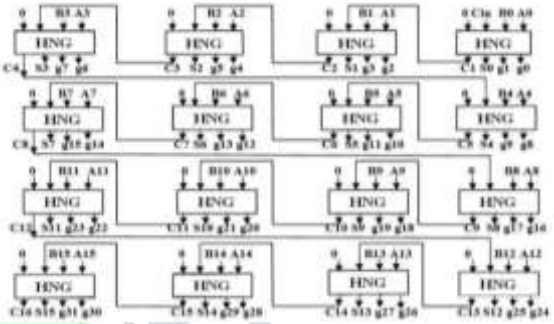

Fig.6. 16- Bit reversible ripple carry adder.

VI. RESULTS

The proposed reversible UT multiplier designs are functionally verified through a logic simulation process. To perform simulation, test benches are created for the reversible UT multiplier designs. The Virology HDL is used to code the designs. The simulation is carried out using Xilinx 14.3 ISE. The Fig.7, Fig.8,Fig.9 and Fig.10 shows the simulation waveforms for reversible 4x4, 8x8 and 16x16 UT multipliers.

Fig.7: Simulation results for 2x2 UT Vedic multiplier.

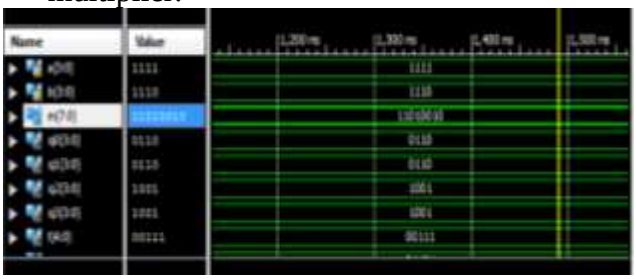

Fig.8: Simulation results for 4x 4 UT Vedic multiplier.

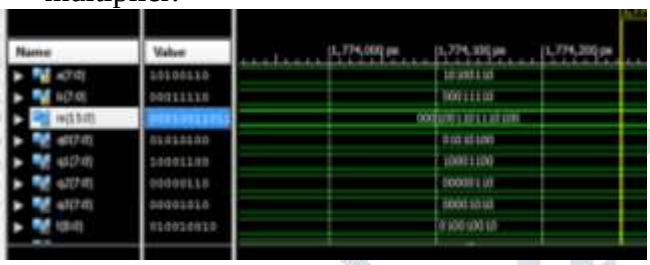

Fig.9: Simulation results for 8x8 UT Vedic multiplier.

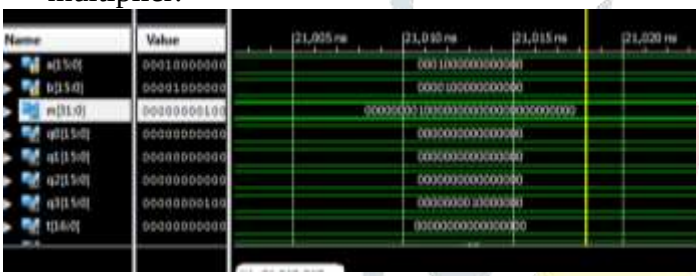

Fig.10: Simulation results for 16x16 UT Vedic multiplier.

VII. CONCLUSION

In this thesis the UT Vedic Multipliers is realized using reversible logic gates. First 2X2 UT multiplier is designed using Peres gate and Feynman gate. The ripple carry adders which were required for adding the partial products were constructed using HNG gates. A 16-bit modified multiplier is designed. The 16-bit multiplier is realized using four 8-bit Vedic multipliers and modified ripple carry adders. Results also indicate a increase in the speed when compared to normal Vedic multiplier. This design has high speed, smaller area and less power consumption when compared with other reversible logic multipliers.

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