DESIGN OF CMOS PLC RECEIVER USING DUAL POWER LINES FOR DESIGN-FOR-TESTABILITY

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Abstract:

As the circuit complexity increases, the number of internal nodes increases proportionally, and individual internal nodes are less accessible due to the limited number of available I/O pins. To address the problem, we proposed power line communications (PLCs) at the IC level, specifically the dual use of power pins and power distribution networks for application/ observation of test data as well as delivery of power. A PLC receiver presented in this design intends to demonstrate the proof of concept, specifically the transmission of data through power lines. The main design objective of the proposed PLC receiver is the robust operation under variations and droops of the supply voltage rather than high data speed. The PLC receiver is designed and fabricated in CMOS 0.18-μm technology under a supply voltage of 1.8 V. The measurement results show that the receiver can tolerate a voltage drop of up to 0.423 V for a data rate of 10 Mb/s. The power dissipation of the receiver is 3.26 mW under 1.8 V supply, and the core area of the receiver is 74.9 μm $\times$ 72.2 μm. .

1. INTRODUCTION

WITH each new generation of deep sub micrometer VLSI technologies, testing, debugging, and diagnosis of VLSI circuits become more difficult and expensive. In addition to higher circuit complexity for a deeper sub micrometer technology, larger process variations, greater interconnection delays relative to transistor switching time, and larger leakage current also contribute to make the testing more challenging. It is a general consensus among test engineers that accessibility, i.e., controllability and observability, to internal nodes for both 2-D and 3-D ICs is essential to address the testing problems [1]–[12]. Conventional design-for-testability (DFT) methods, such as scan design, provide dedicated or shared signal paths between I/O pins and internal nodes [13]–[15]. As the circuit complexity increases, the number of internal nodes increases proportionally, and individual internal nodes are less accessible due to the limited number of available I/O pins. One promising approach to provide ubiquitous accessibility to internal nodes is the dual use of power pins and power distribution networks (PDNs) for data communications as well as power delivery, which is essentially power line communications (PLCs) at the IC level [1]. The PLC at the IC level would be useful for low data rate communications such as scan design, system debugging, and fault diagnosis. The approach also eliminates the need to route a data path from the

node to an external data pin. To the best of our knowledge, PLC in an IC environment was exclusively reported in [1] and [21]–[29].
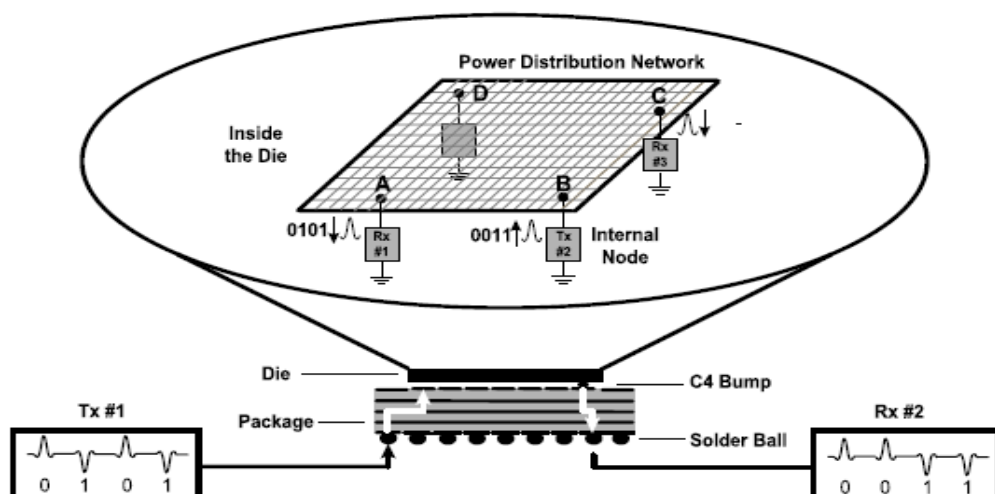

Fig.1.1: Proposed conceptual PLC system in an IC environment.

Fig.1.1 shows the conceptual PLC system in an IC environment considered for our research. A test instrument sends the data superimposed on the supply voltage of a system board. The signal travels through a power pin(s), the power planes of a package, and the PDN, and then it reaches at the intended node(s). The PLC receiver embedded inside a chip extracts the data from the power line. All the previous PLC receivers designed in [21]–[23], [25]–[27], and [29] report only the simulation results. This paper presents a PLC receiver, whose main design objective is robust operation under supply voltage variations and droops. The proposed PLC receiver was designed and fabricated in CMOS 0.18-μm technology with a supply voltage of 1.8 V. The remainder of this paper is organized as follows. Section II provides the background of the proposed work, specifically operating conditions of PLC in ICs and our previous works. Section III describes the proposed PLC receiver and its building blocks.
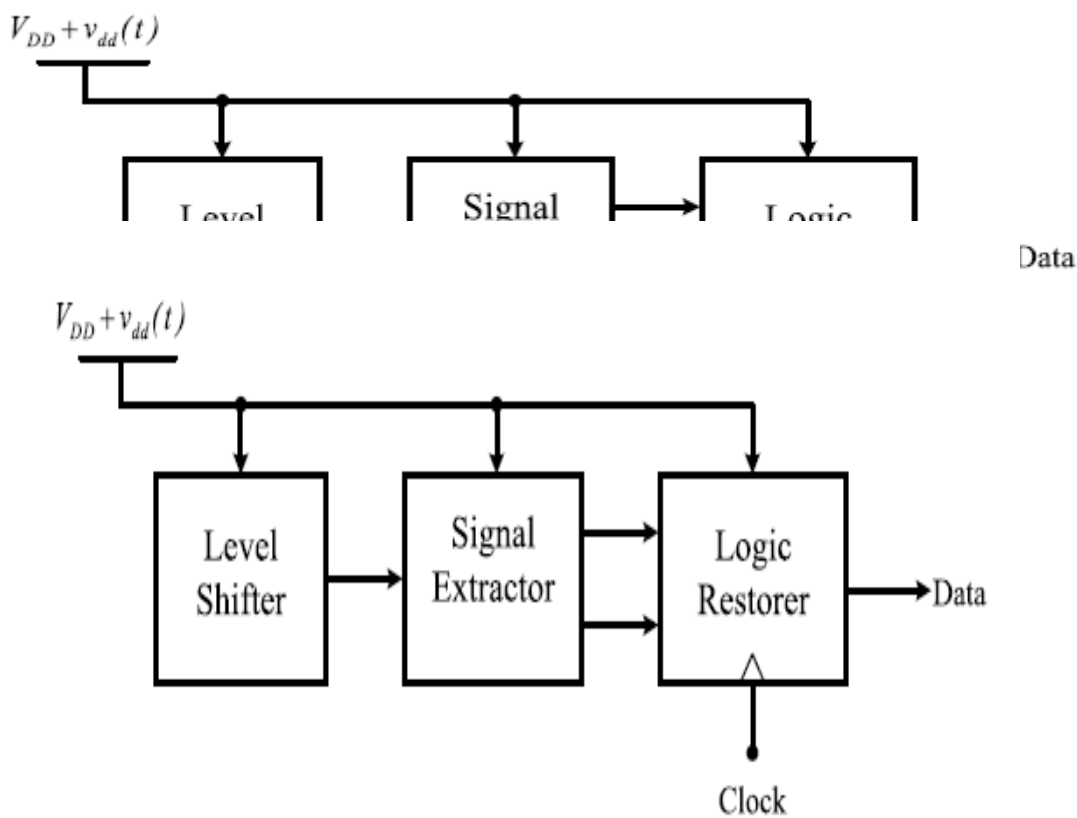
Figure 2.1: Basic diagram of the proposed PLC receiver.

The proposed on-chip PLC receiver receives the data superimposed on power lines, and the data (such as scan test data) are sent from a test instrument. Therefore, the transmitter for the PLC receiver is an external instrument rather than the one on the same chip. The receiver was designed in CMOS 0.18-μm technology with a supply voltage of 1.8 V. It consists of three building blocks, and this section describes the design of each building block.

A block diagram of the proposed PLC receiver is shown in Fig.2.1 The proposed PLC receiver consists of three blocks, each sharing the same supply voltage (*VDD* + *v*dd*(t))*. The first block is a level shifter, which lowers the dc level of the signal superimposed on the supply voltage. The level shifted signal is processed by the subsequent block, a signal extractor, which amplifies the signal and converts it to a differential signal. The logic restorer, which is a differential Schmitt trigger, recovers logic values from the differential signal. The design and operation of each block is explained below.

3. LEVEL SHIFTER

The level shifter shown in Fig. 3.1 can be treated as a common source amplifier with diode-connected load as, in which the amplifier input is fixed to a bias voltage *V*bias. The level shifter propagates the data signal *v*dd*(t)* imposed on the supply voltage *V*DD to the output while lowering the dc voltage level of the signal to 0.5 *V*DD. To propagate the data signal superimposed on the supply voltage to the output, the output should be sensitive to supply voltage variations. In other
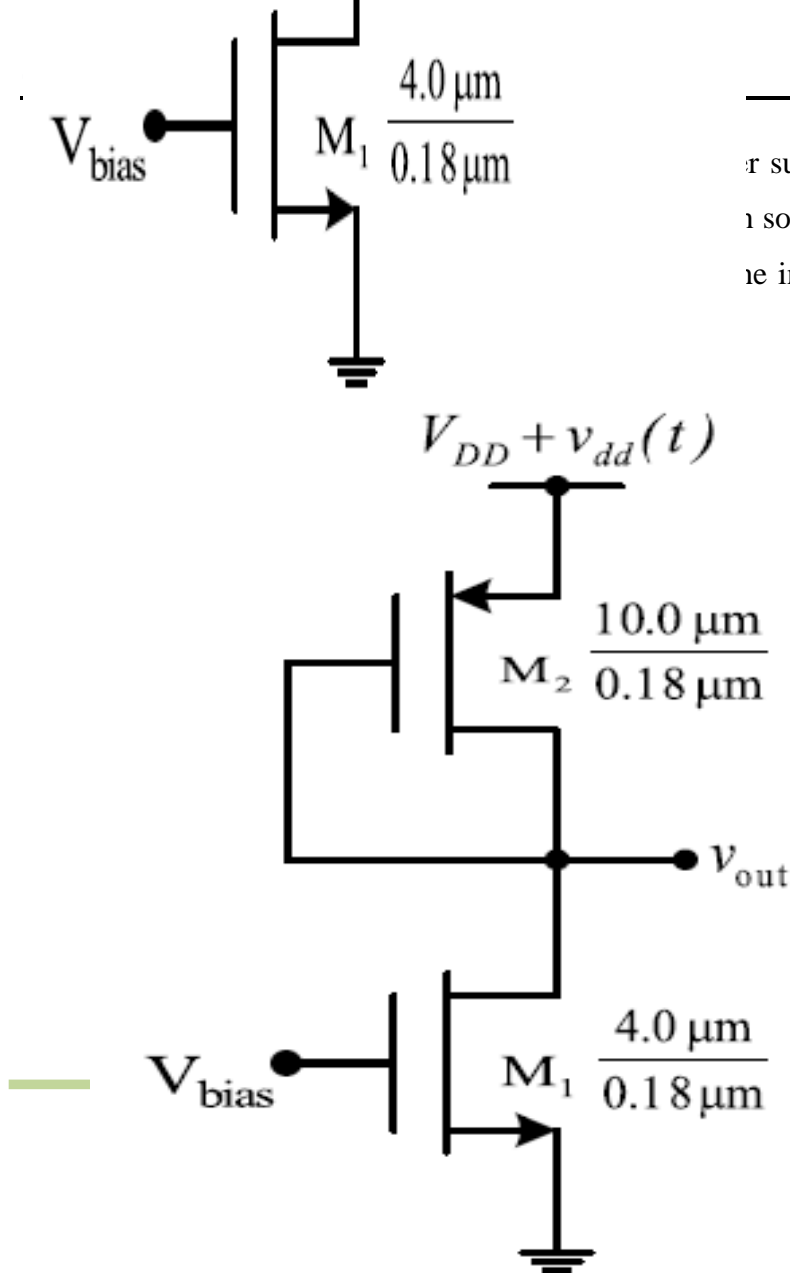
r supply rejection ratio (PSRR) of the level

n source amplifier with the gate of M1 as the

ne input to the voltage gain from the supply

Fig 3.1: Level shifter.

4. SIGNAL EXTRACTOR

The input signal of the signal extractor is the data signal offset with 0.5 VDD, and the signal extractor amplifies the data signal while removing the dc offset voltage. The signal extractor shown in Fig. 4.3 is a differential amplifier, in which one input is connected to an RC low-pass filter. The low-pass filter intends to extract the dc value of the signal. The differential amplifier rejects the common-mode signal of the two inputs or the dc value. It also converts a single-ended input into a differential output pair. The voltage gain of the differential amplifier is expressed as

$$A_v = -g_{m_{2,3}} R_D$$

Where *gm2* and *gm3* are equal to *μCox(W/L)(VGS–VTH)*. The gain increases by increasing *W/L* and/or *RD* at the cost of a larger device size and increased parasitic capacitances. A larger *RD* also leads to a higher voltage drop to limit the maximum voltage swing. The transistor size, *W/L*,The *RC* low-pass filter intends to pass the dc value, which can possibly vary or fluctuate, while removing the signal. The filter is off-chip for our test chip, which enables us to try different cutoff frequencies. The resistor *R* of the filter is set to 3 K_ and the capacitor 5 nF for our experiments. The −3 dB cutoff frequency of the *RC* filter is 10.6 KHz. Note that it is desirable for the *RC*-filter to be on-chip for the final design, which is possible through the increase of the data rate and hence the cutoff frequency.
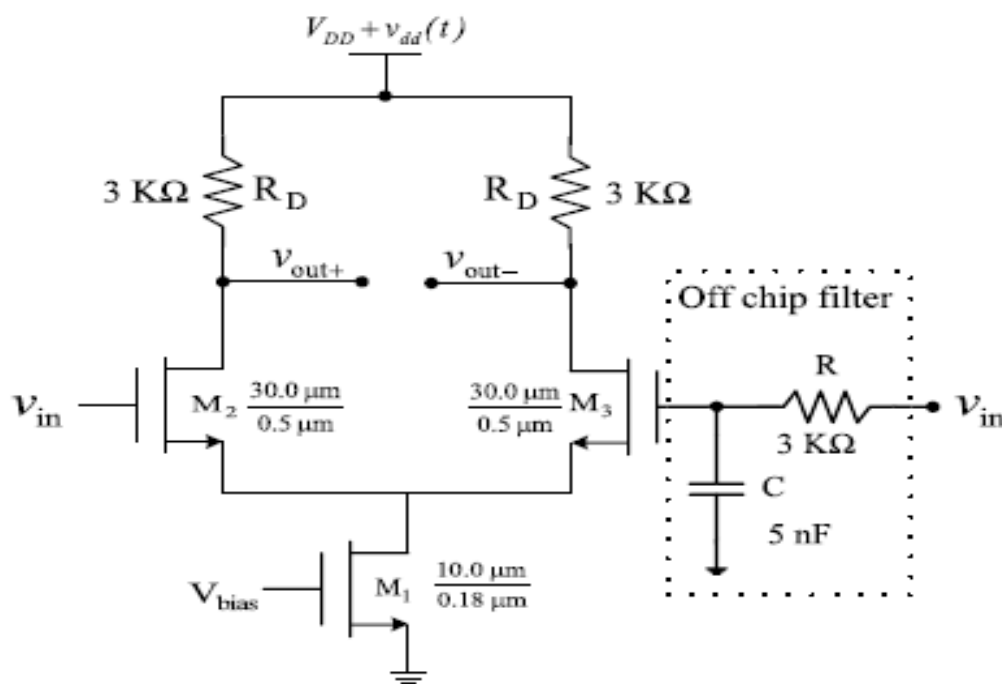

Fig 4.1: Signal extractor.

5. LOGIC RESTORER

The logic restorer translates the data in the form of an analog differential signal into logic values. It is based on the differential Schmitt trigger presented in [36] and is shown Fig.5.1.

A key aspect of the Schmitt trigger is the hysteresis generated through the regenerative feedback circuit, specifically a cross-coupled inverter pair. When a new data signal is applied to the logic restorer, the clock is turned from low to high and turns OFF *M5* and *M6*. It reduces the current supplied to the differential amplifier, which results in a smaller gap between the high and the low threshold voltages. The cross-coupled inverter pair settles to a high or low state, and hence the output of the logic restorer. Then, the clock signal becomes low, and *M5* and *M6* are turned ON. The

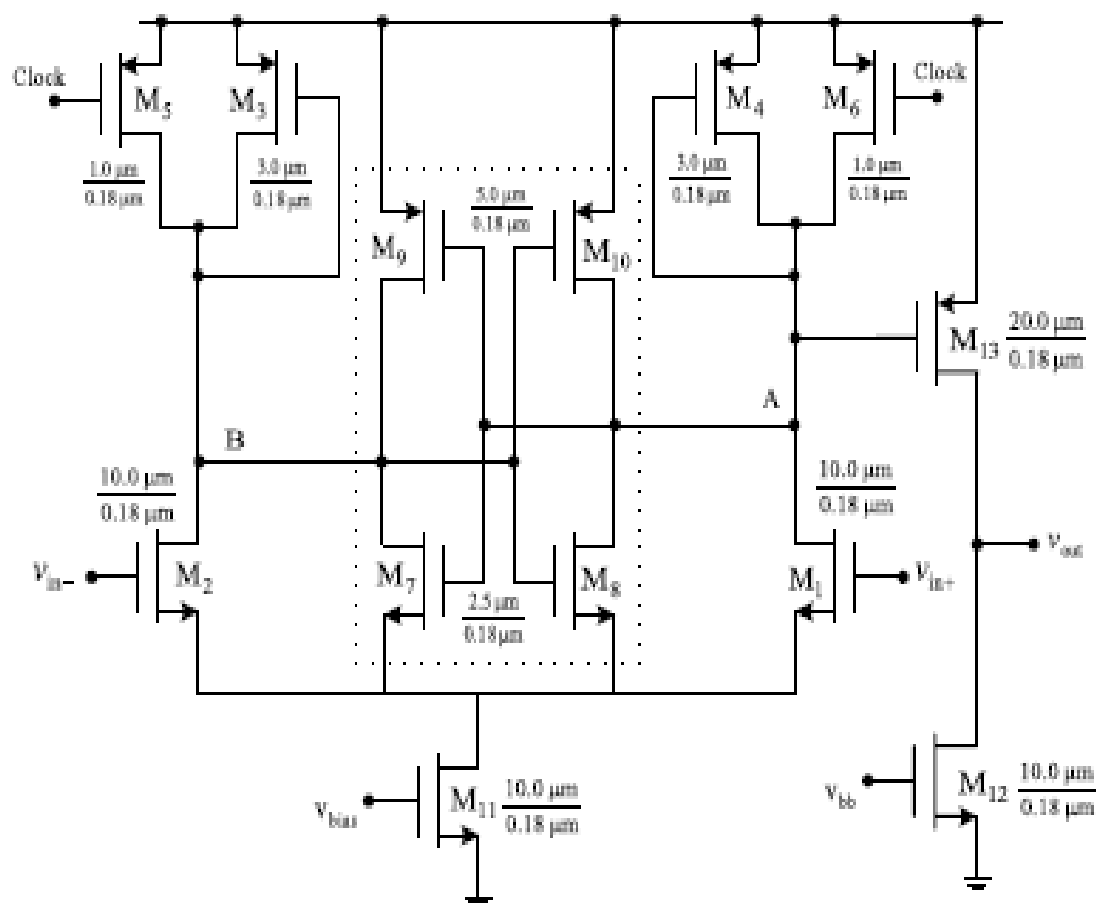gap between the two threshold voltages becomes wider, which increases the immunity to noise and disturbances.

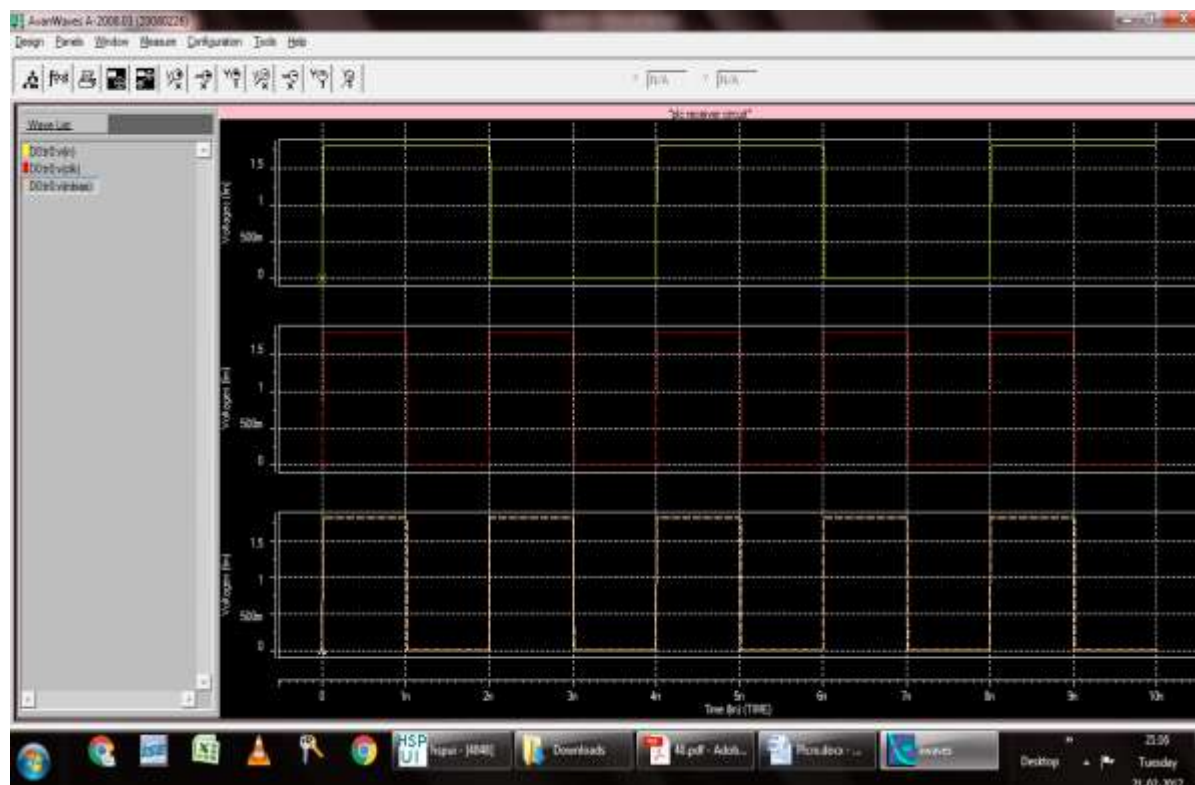**Fig 5.1: Logic restorer.**

6. SIMULATION RESULTS

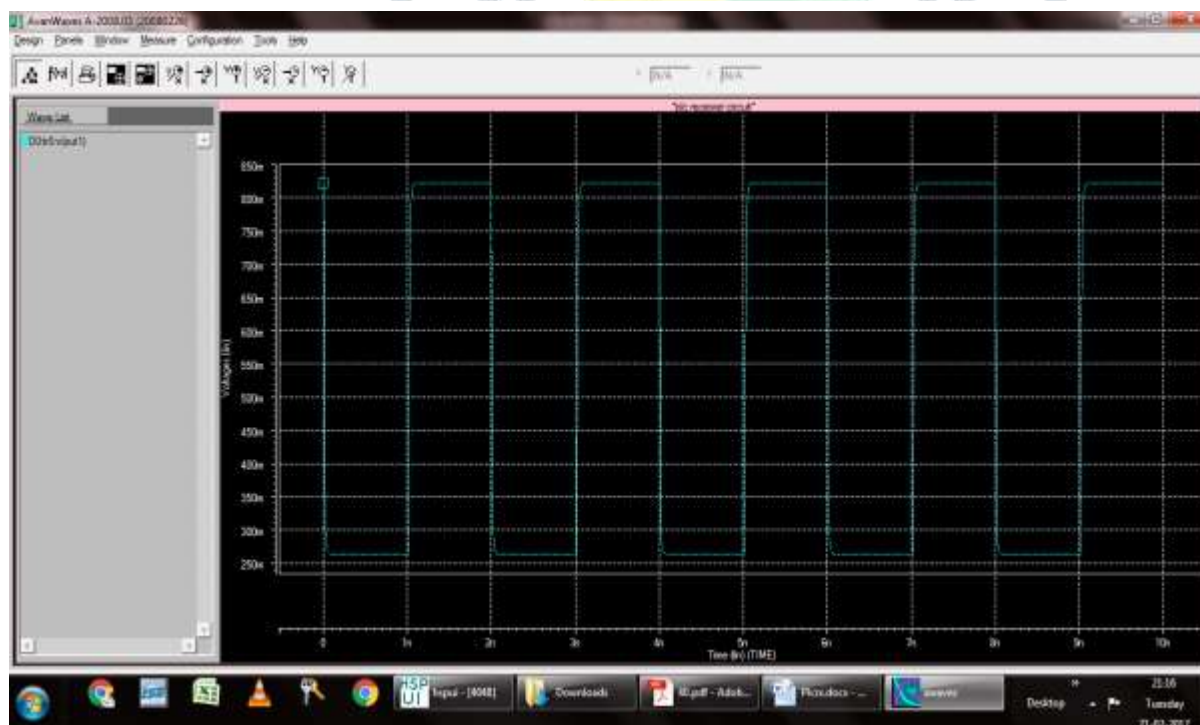
Fig 6.1: input clock & bias signals.
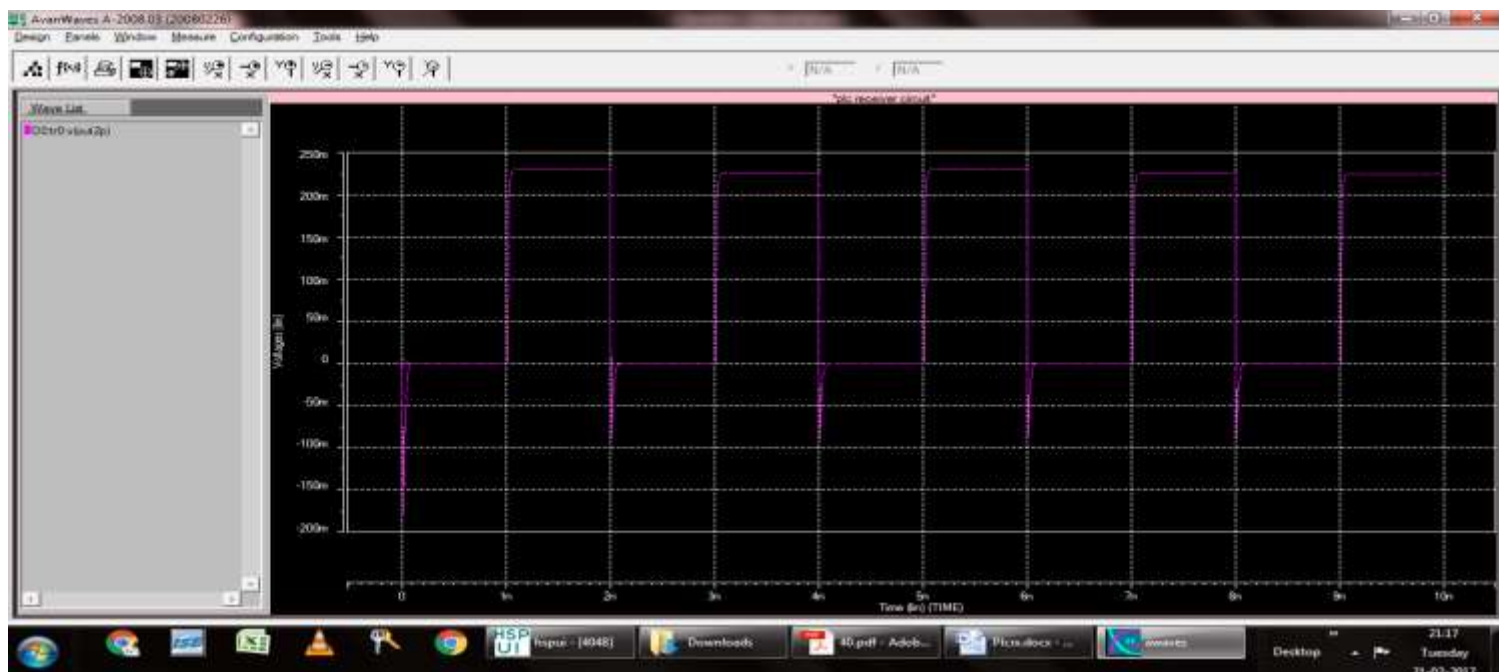

Fig 6.2: Level shifter.
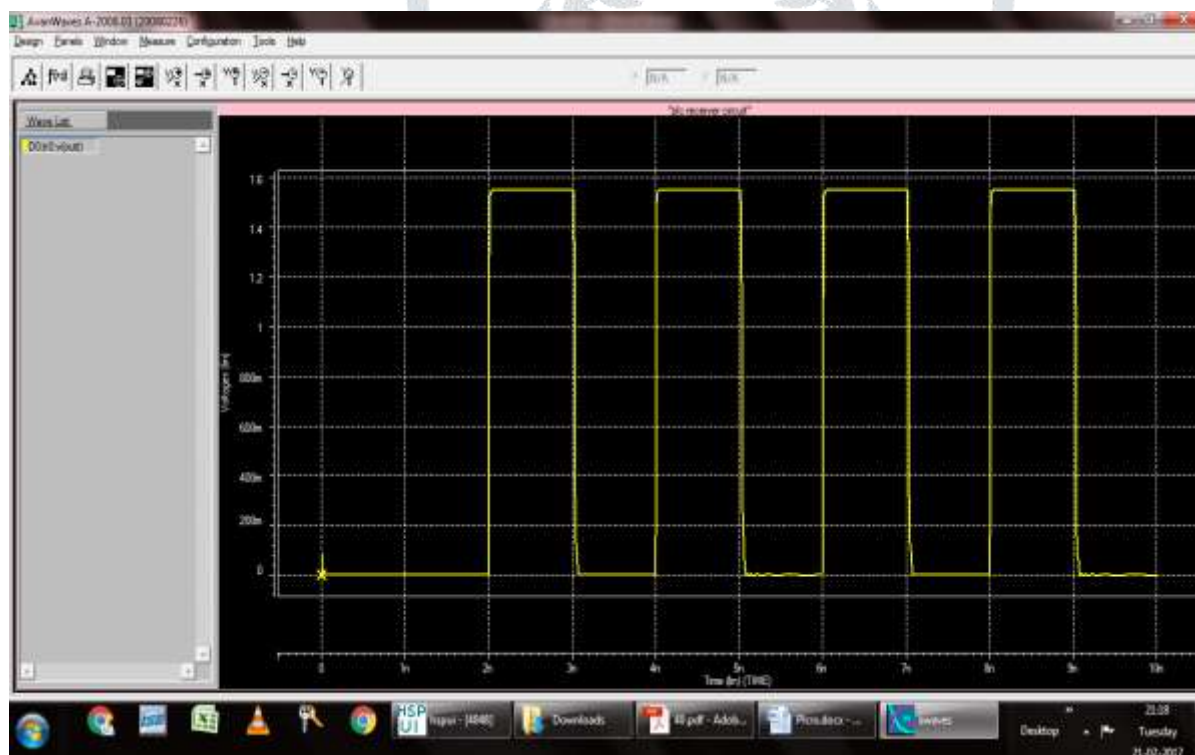
Fig 6.3: Signal extractor.

Fig 6.4: Logic restorer output (Final output).

CONCLUSION

A receiver for PLC at the IC level, which can be applicable to low data rate communications, such as scan design, system debugging, a8nd fault diagnosis, was investigated in this paper. The proposed PLC system adopts a binary ASK modulation scheme, and the PLC receiver consists of three building blocks. The level shifter shifts the dc level of the data signal to a half of the supply voltage. The signal extractor, based on a differential amplifier, removes the dc voltage from the data signal with the aid of a low-pass filter, which mitigates supply voltage fluctuations and droops. The logic restorer, based on a differential Schmitt trigger, extracts logic values from the data signal while improving the noise immunity of the receiver. The PLC receiver was designed to demonstrate the feasibility of a robust receiver as a proof of concept and fabricated in CMOS 0.18-μm technology. The measurements show that the PLC receiver can tolerate a supply voltage drop of 0.423 V or 23.5%. The power dissipation for the receiver is 3.2 mW under 1.8 V supply.

It requires a wide scope of research efforts to exploit the potential of the PLC in ICs fully. To point out a few, modeling of power pins, packages, and PDNs, channel characterization, modulation and multiple access schemes, SNR versus bit-error rates of a given system, design of PLC receivers and transmitters, and adverse impact of the data signals superimposed on power lines to the operation of digital circuits.

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