# Multi-level Inverter Controlled 3-phase Induction Motor

<sup>1</sup>Mr. Sanjay Kathar, <sup>2</sup>Dr. A. S. Bhalchandra <sup>1</sup>ME Student, <sup>2</sup>Professor

<sup>1</sup> Department of Electronics & Telecommunication Engineering, Government Engineering College Aurangabad (MS), India

<sup>2</sup> Department of Electronics & Telecommunication Engineering Government Engineering College Aurangabad (MS), India

*Abstract:* The paper reflects the use of three level diode clamped multi-level inverter to control the speed of an induction motor. This technique in addition with multi-carrier PWM control scheme is highly recommended to obtain high quality sinusoidal output voltage with minimum/reduced harmonic distortion. An open loop speed control can be achieved by using V/f method. This method can be implemented by change the supply voltage and frequency applied to the three phase induction motor at constant ratio. The proposed system is an effective replacement for the conventional method which produces high switching losses, results in poor drive performance. The simulation results reveal that the proposed circuit effectively controls the motor speed and enhances the drive performance through reduction in total harmonic distortion (THD).

# Index Terms – Induction Motor, Diode clamped multilevel inverter, Multicarrier PWM technique, V/f control

### I. INTRODUCTION

Majority of industrial drives use ac induction motor because these motors are rugged, reliable, and relatively inexpensive. Induction motors are mainly used for constant speed applications because of unavailability of the variable-frequency supply voltage [2]. But many applications need variable speed operations. Historically, mechanical gear systems were used to obtain variable speed. Recently, power electronics and control systems have matured to allow these components to be used for motor control in place of mechanical gears. These electronics not only control the motor's speed, but can improve the motor's dynamic and steady state characteristics. Adjustable speed ac machine system is equipped with an adjustable frequency drive that is a power electronic device for speed control of an electric machine. It controls the speed of the electric machine by converting the fixed voltage and frequency to adjustable values on the machine side. High power induction motor drives using classical three phase converters have the disadvantages of poor voltage and current qualities. To improve these values, the switching frequency has to be raised which causes additional switching losses. Another possibility is to put a motor input filter between the converter and motor, which causes additional weight. A further inconvenience is the limited voltage that can be applied to the induction motor determined by the blocking voltage of the semiconductor switches. The concept of multilevel inverter control has opened a new possibility that induction motors can be controlled to achieve dynamic performance equally as that of dc motors [2].

Recently many schemes have been developed to achieve multilevel voltage profile, particularly suitable for induction motor drive applications. The diode clamp method can be applied to higher level converters. As the number of level increases, the synthesized output waveform adds more steps, producing a staircase waveform. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels [7] Unfortunately, the number of the achievable levels is quite limited not only due to voltage unbalance problems but also due to voltage clamping requirement, circuit layout and packaging constraints. In this paper, a three-phase diode clamped multilevel inverter fed induction motor is described. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors [2]. The voltage across the switches has only half of the dc bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device [4]. The proposed inverter can reduce the harmonic contents by using multicarrier PWM technique. It generates motor currents of high quality. V/f is an efficient method for speed control in open loop. In this scheme, the speed of induction machine is controlled by the adjustable magnitude of stator voltages and its frequency in such a way that the air gap flux is always maintained at the desired value at the steady-state. Here the speed of an induction motor is precisely controlled by using three level diode clamped multilevel inverter. . The voltage source inverter produces an output voltage or a current with levels either zero or  $\pm$ Vdc. They are known as two level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various pulse width modulation strategies. In high- power and high voltage applications, these twolevel inverters have some limitations in operating at high frequency. mainly due to switching losses and constraints of device rating. The dc link voltage of a two-level Inverter is limited by voltage ratings of switching devices; the problematic series connection of switching devices is required to raise the dc link voltage.



Fig.1. Two level inverter.

By series connection, the maximum allowable switching frequency has to be more lowered; hence the harmonic reduction becomes more difficult. In addition, the two level inverters generate high frequency common-mode voltage within the motor windings which may result in motor and drive application problems. From the aspect of harmonic reduction and high dc link voltage level, three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage. A three level inverter will not generate common-mode voltages when the inverter output voltages are limited within certain of the available switching states. So the three level inverter topology is generally used in realizing the high performance, high voltage ac drive systems

#### **II. LITERATURE REVIEW**

History of multilevel inverters began in 1975 with Baker and Bannister. This first patent described a converter topology capable of producing multilevel voltage by connecting single phase inverter in series. Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly [1, 2, 3]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application. The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters [4]. More recent applications have been for power system converters for VAR compensation and stability enhancement [5], active filtering [6], high-voltage motor drive [3], high-voltage dc transmission [7], and most recently for medium voltage induction motor variable speed drives [8]. Many multilevel converter applications focus on industrial medium-voltage motor drives [3, 9], utility interface for renewable energy systems [10], flexible AC transmission system (FACTS) [11], and traction drive systems [12]. The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs) because the series connection allows reaching much higher voltages. However, the series connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased. The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in 1975 [14]. Separate DC-sourced full-bridge cells are placed in series to synthesize a staircase AC output voltage.

The term multilevel began with the three-level converter [15]. Subsequently, several multilevel converter topologies have been developed [16]. In 1981, diode-clamped multilevel inverter also called the Neutral-Point Clamped (NPC) inverter schemes were proposed [17]. In 1992, capacitor-clamped (or flying capacitor) multilevel inverters, [18] and in 1996, cascaded multilevel inverters were proposed [1], [19]. Although the cascade multilevel inverter was invented earlier, its application did not prevail until the mid-1990s. The advantages of cascade multilevel inverters were prominent for motor drives and utility applications. The cascade inverter has drawn great interest due to the great demand of medium-voltage high-power inverters. The cascade inverter is also used in regenerative-type motor drive applications [20, 21]. Recently, some new topologies of multilevel inverters have emerged. This includes generalized multilevel inverters [22], mixed multilevel. Inverters [23], hybrid multilevel inverters [24,25] and softswitched multilevel inverters [26]. These multilevel inverters can extend rated inverter voltage and power by increasing the number

of voltage levels. They can also increase equivalent switching frequency without the increase of actual switching frequency, thus reducing ripple component of inverter output voltage and electromagnetic interference effects.

#### **III. SYSTEM DEVELOPMENT**



The block schematic of multilevel inverter fed three phase induction motor is as shown in Fig The complete system will consist of two sections; a power circuit and a control circuit. The power section consists of a power rectifier, filter capacitor, and three phase diode clamped multilevel inverter. The motor is connected to the multilevel inverter. An ac input voltage is fed to a three phase diode bridge rectifier, in order to produce dc output voltage across a capacitor filter. A capacitor filter, removes the ripple contents present in the dc output voltage. The pure dc voltage is applied to the three phase multilevel inverter through capacitor filter. The multilevel inverter has 12 MOSFET switches that are controlled in order to generate an ac output voltage from the dc input voltage. The control circuit of the proposed system consists of three blocks namely microcontroller, optocoupler and gate driver circuit. The microcontroller is used for generating gating signals required to drive the power MOSFET switches present in the multilevel inverter. The voltage magnitude of the gate pulses generated by the microcontroller is normally 5V. To drive the power switches satisfactorily the opto- coupler and driver circuit are necessary in between the controller and multilevel inverter. The output ac voltage is obtained from the multilevel inverter can be controlled in both magnitude and frequency (V/f)open loop control). The controlled ac output voltage is fed to the induction motor drive. When the power switches are on, current flows from the dc bus to the motor winding. The motor windings are highly inductive in nature; they hold electric energy in the form of current. This current needs to be dissipated while switches are off. Diodes are connected across the switches give a path for the current to dissipate when the switches are off. These diodes are also called freewheeling diodes. The V/f control method permits the user to control the speed of an induction motor at different rates. For continuously variable speed operation, the output frequency of multilevel inverter must be varied. The applied voltage to the motor must also be varied in linear proportion to the supply frequency to maintain constant motor flux.



Fig 3. : Circuit diagram

The rated motor current is 0.6amp, 0.25hp and its rated voltage 440V ac and 1500 RPM. Our dc power supply is derived from single phase ac mains and hence gives 310V unregulated dc at the filter capacitor. Based on this, the high frequency, IRF 840 MOSFET has been used as a power switch in the inverter.

*A.* **D.C Power supply to inverter:** The supply to the inverter is provided by a bridge rectifier directly connects to single phase ac mains. Ripples in dc output are smoothened by using a filter capacitor. The bride rectifier diodes used are 6A4 power diodes each rated for PIV 400V and 6A current. The  $150\mu$ F smoothing capacitor has a voltage rating of 350V DC.

**B. 3-phase induction motor (option) 0.25 HP 1440 RPM:** The output received from the multi-level inverter is cascaded to the 3 phase induction motor. The 3 phase motor used has rating of 0.6 A, 0.25 HP, 1440 rpm.

# • Parameters: The various parameters used for performance analysis are,

- a. Current Waveform and magnitude
- b. Voltage waveform and magnitude
- c. Output Frequency
- d. Total Harmonics Distortion

#### **IV. EXPERIMENTAL RESULTS**

To produce a staircase-output voltage, consider one leg of the three-level inverter, as shown in Fig.. The steps to synthesize the three-level voltages are as follows.

- 1. For an output voltage level Vao=Vdc, turn on all upper-half switches A1 and A2.
- 2. For an output voltage level Vao=Vdc, turn on one upper switch A2 and one lower switch A1'
- 3. For an output voltage level Vao=0, turn on all lower half switches A1' and A2'

Fig. shows the phase voltage waveform of the three-level inverter. The m-level converter has an m-level output phase-leg voltage and a (2m-1)- level output line voltage.



# Fig 4. : Output Waveform

The most attractive features of multilevel inverters are as follows.

a) They can generate output voltages with extremely low distortion and lower dv/dt.

b) They draw input current with very low distortion.

c. They generate smaller common- mode (CM) voltage, thus reducing the stress in the motor bearings.

d They can operate with a lower switching frequency.

**Total Harmonic Distortion:** In order to determine the relative distortion due to harmonics on a power system, the term Total Harmonic Distortion (THD) has emerged. The THD is a measure of the amount of distorted harmonics that are impeded on the system voltage, expressed as a percentage of the fundamental. Both voltage and current waveform distortion are represented by THD.

$$THD = \sqrt{\frac{\text{sum of squares of amplitude of all harmonics}}{\text{Square of amplitude of fundamental}}} * 100$$
$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \times 100\%$$

Where, Vh is the RMS value of harmonic component h, V1 is the RMS value of the fundamental component of voltage. The total harmonics distortions are observed to be reduced up to 12%.

Total Harmonic Distortion (In %)						
VRY	VRN	3	5	7	9	Speed (RPM)
52	32	51.5	24.8	30.2	30.9	209
59	38	26.2	18	24.1	22.2	272
80	50	25.7	9	19.2	21.3	367
109	70	24.1	8.8	18.3	21	533
135	87	10.1	6.4	17.2	16.4	618
162	95	8.7	5.8	16.3	13.4	841
173	110	3	5.5	13.2	11.3	1022

Table 1: % THD details of 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup>, 9<sup>th</sup> harmonics.



Fig 5: Trends showing Reduction of THD



Fig 6: Practical set up for performance analysis of multilevel inverter using power quality analyzer



Fig 7: Practical output waveforms of multilevel inverter as obtained on "DRANETZ POWER VISA" power quality analyzer.

# V. HARDWARE RESULTS

- FCT: Frequency clock time waveform of VCO circuitry typically 250 KHz required to change 'D' of PWM IC.
- **RCT:** Real clock time waveform typically of 250 KHz which is applied to Schmitt trigger. It is a fixed amplitude/fixed frequency clock pulse.
- OCT/VCT: OCT has a fixed frequency of 275 KHz which is output of Schmitt trigger whereas VCT is voltage clock time is also a 475 KHz fixed frequency clock pulses from schitt trigger & goes to PWM IC.
- **PWM Output:** Figure indicates the waveform of PWM output at R<sup>+</sup> to B<sup>-</sup> before optocoupler indicating A ≈ 1V whereas figure 4.8 indicates the waveform of PWM output at R<sup>+</sup> to B<sup>-</sup> before optocoupler indicating A ≈ 6V. These RCT, OCT, VCT is treated as input to the PWM IC which indicates the output.

#### VI. Output



Fig 8. Output obtained on CRO

### **VII. CONCLUSION**

This paper provides study of three-level diode clamped inverter, which also known as neutral-point clamped (NPC) inverter. The proposed three level inverter essentially adds the attractive aspects of the traditional two level inverter such as less power components, simple working principle, & minimum conduction power loss to the main advantages of the multilevel inverter such as low THD% & high output voltage quality. The performance of the three-phase three-level twelve switch inverter has been explained and improved by employing PWM control scheme. The use of three-level inverters reduces the harmonic components of the output voltage compared with the two-level inverter at the same switching frequency. It needs no additional reactors or transformers to reduce the harmonic components.

#### REFERENCES

- [1] Brenden Peter McGrath, Donald Graheme Holmes, "Multicarrier PWM Strategies for Multilevel Inverters" IEEE Transactions on Industrial Electronics, vol. 49, no. 04, pp. 858-867, Aug 2012.
- [2] Congzhe Gao, Xinjian Jiang, Yongdong Li, "A DC link Voltage Self Balance Method for Diode Clamped Modular Multilevel Converter with Minimum numbers of Voltage Sources" IEEE Trans. on Power Electron.,vol.28,issue no.05, pp 2115-2139, May 2013.
- [3] Ritu Chaturvedi, "A Single Phase Diode Clamped Multilevel Inverter and its Switching Functions", International Journal of Innovative trends in Science, Pharmacy & Technology, vol. 01, pp. 63-66, 2014.
- [4] A.Naveen Kumar, Kiran Kumar Ch, R.H.Vardan & B.Basavaraja, "Multilevel Power Converters: A Survey", International Journal of Power System Operation and Energy Management, Vol-2, Issue-1,2 pp. 2231 – 4407.
- [5] D. D. Khairnar, V. M. Deshmukh, "Review study on Topologies of Multilevel Inverters", International journal of Innovative Research and Development, Vol. 03, Issue 05, May 2014, pp. 19-24.
- [6] Won-Sik Oh, Sang-Kyoo Han, Seong-Wook Choi and Gun-Woo Moon, "A Three Phase Three-level PWM Switched Voltage Source Inverter with Zero Neutral Point Potential", Journal of Power Electronics, Vol. 5, No. 3, pp. 224-232, July 2005.
- [7] M. Venu Madhav, K.S. Ravi Kumar, "MATLAB based Analysis and Simulation of Multilevel Inverters", International Journal of Computer Applications (0975 – 8887) Volume 39– No.4, pp. 17-19, Feb 2012.
- [8] G. Laxminarayana, K.pradeep, "Comparative Analysis of 3-, 5- and 7-Level Inverter Using Space Vector PWM", International Journal of Advanced Research in Electrical,
- [9] S. Krishnapriya, Unnikrishnan L, "Multilevel Inverter Fed induction motor Drives" International Journal of Research in Engineering & technology", IJRETVolume:04, Issue:09, September 2015.
- [10] Gaddafi Sani Shehu, Abdullaji Bala Kunya "A review of Multilevel Inverter Topology & Controlled Techniques". Journal of Automation and Control Engineering, Volume: 04, Issue: 3, June 2016.
- [11] C.R. Balamurugan, S.P.Natrajan, "A review on various Multilevel inverter topologies", Global Journal Of advanced Research, Volume 2, Issue:01, PP.142-153.