Design and Simulation of Different Topology of Low Power CMOS Full Adder

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Abstract: A fast and power-proficient CMOS full Adder (FA) assumes enter part in gadgets exchange particularly performing math tasks in microchips, digital signal processing (DSP) what's more, image processing. Full Adder (FA) is such a noteworthy component which contributes generously to the aggregate power utilization of the system. In this paper, topologies of CMOS Full Adder has been delineated which is then penniless down. The leakage power utilization has been done in the circuit utilizing diverse topologies, for example, 90nm and 45nm. By using Cadence tools, the designed CMOS

Full adder Topologies are compared in phrases of leakage power consumption and surface area. We planned and thought about 14T CMOS full adder, 12T CMOS full adder 10T full viper and 9T CMOS full adder as far as zone, power.

Key Words: CMOS, CMOS Full Adder, Leakage Power, Leakage Current, Area, Cadence.

1. Introduction

Power utilization is an imperative proficiency factor in outlining Very Large Scale Integrated (VLSI) Circuit. In addition, with the hazardous development of VLSI innovation the request and notoriety of compact gadgets has driving fashioners to take a stab at littler silicon territory, higher speed, longer battery life, less power utilization and greater dependability hardware circuits. The plan paradigm of a full adder (FA) cell includes transistor tallies which to a great extent influences the outline intricacy of many capacity units, for example, multiplier and algorithmic logic unit digital adder ALU)[1,2] The speed of the outline is restricted by size of the transistors, parasitic capacitance and deferral in the basic way. The driving capacity of a full snake is critical as they are for the most part utilized in course arrangement, where the yield of one gives the contribution to other. A few full viper circuits have been proposed focusing on configuration accents, for example, power, postponement and territory. Among those outlines with less transistor tally utilizing pass transistor rationale have been generally used to lessen control utilization [3,4].These designs can be divided into two types, the CMOS logic and the pass -transistor logic [5]. In this paper, we have given a concise depiction of the advancement of FA circuits as far as lesser power utilization, higher speed and lesser chip measure.
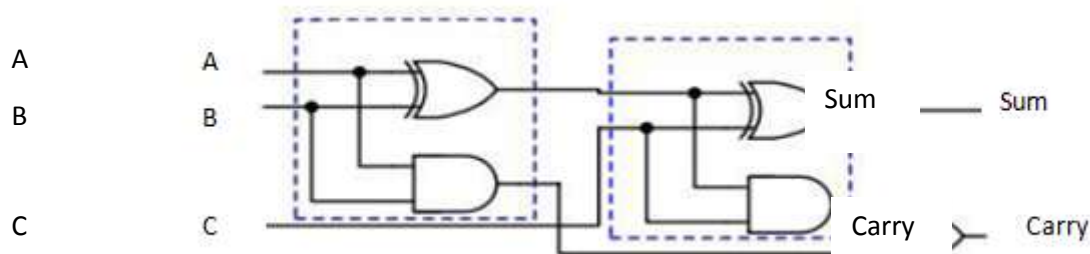

Fig1: Circuit diagram of full adder Circuit has three inputs A, B and C and two outputs sum and carry.

Energy efficient designs for portable devices like notebook Pc, mobile phones, tablets is the main research in electronic field. Diminishing area is one of the ways to achieving a design with less power. Binary adders placing a significant role in ALU operations. Recently plenty of adder circuits had been proposed. But the purpose of the design may vary. This paper mainly focuses on reducing power [6] and area of the circuit. Designer can design full adder in different techniques like C-CMOS, CPL, Transmission function and Transmission gate, GDI, and The 28 transistors Full adder design based on Complementary CMOS technique [7] is same like conventional PMOS and NMOS transistors. Presence of series of transistors make this FA has poor driving capability. And it occupies more area due to large number of transistor. Complementary Pass transistor logic (CPL) is a new significant plan system. The primary distinction between the Complementary CMOS and the CPL (Complementary pass transistor logic) [8] is that the pass transistor has an input in its source side. But in complementary CMOS power lines act as source input. CPL logic is more preferable than the CMOS logic but not than the C-CMOS, due to threshold voltage drop. Also this logic requires inverters in the output stage for getting enough drivability. A transmission gate adder designs uses complimentary properties of Pull- down and pull-up transistor. It has 20 transistors. Uses twice the number of transistor is the main defect of TGA compare to the principle pass-transistor logic. The Majority function based 4-transistor full adder [9] eradicates more time consuming primitive gates like XOR gate.

2. CMOS Full Adder

An adder is an digital electronic circuit that is utilized to perform expansion parallel numbers. FA is a blend circuit that performs expansion of three bits

Figure.2 Block Diagram of Full Adder

Think about a CMOS FA. This circuit has two operands, An and B, and an info convey, Cin. It creates the sum

$$SUM = A \oplus B \oplus Cin$$
$$CARRY = AB + BCin + ACin$$

3. COMPARATIVE ANALYSIS OF TOPOLOGIES OF FULL ADDER

I. 14T CMOS Full Adder

In the paper [10], the different existing FA circuits are been looked at, and in that it incorporates numerous circuits like CMOS Transmission Gate (TG), Pass Transistor Logic (PTL), Complementary Pass transistor Logic (CPL), Gate Diffusion Input (GDI), LPFA (Low Power Full Adder), GDI based Full Adder, and so forth. So the 14 Transistors using full adder schematic is shown in Figure.3 and Transient Response is shown in Figure.4
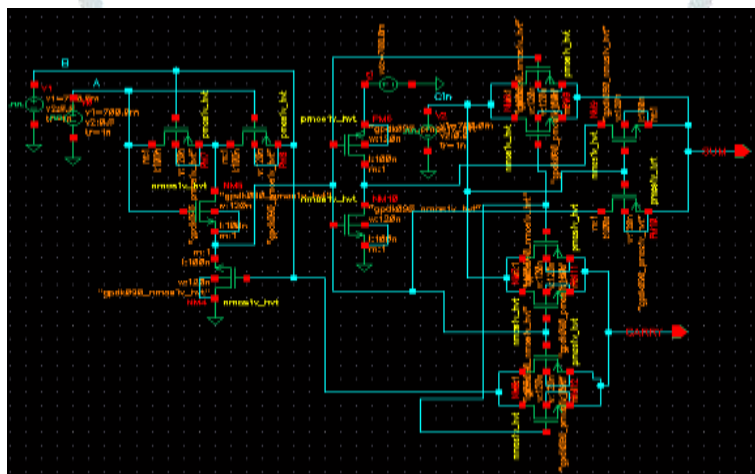

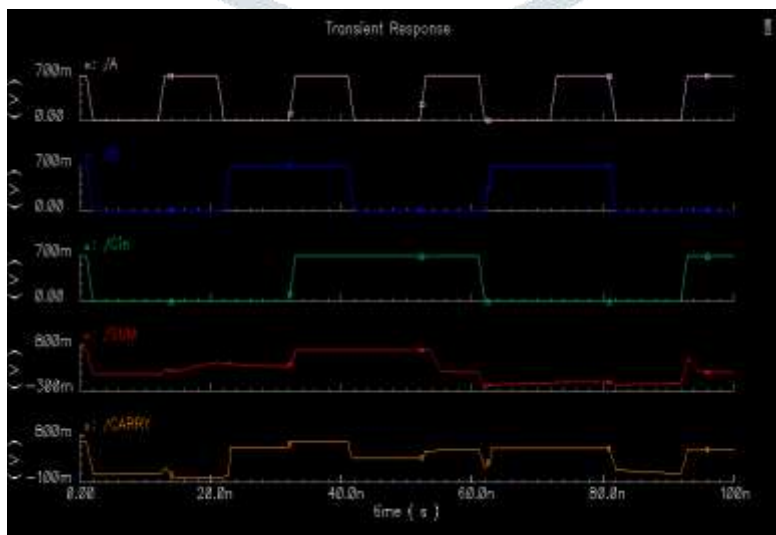Figure.3 Schematic of 14T CMOS Full Adder

Figure.4 Transient Response of 14T CMOS Full Adder

II.   12T CMOS Full Adder

In the paper [11], two new designs FA have been obtainable transistors XOR gates. Simulations of same were completed at various supply voltage switch one-sided connected to NMOS transistors and results indicated changes in control utilization of adder. So the FA with 12 Transistor was exhibited in that paper and we have picked and have taken the same and have been contrasted and different circuits and schematic 12T CMOS FA is shown in Figure.5 and Transient Response is revealed in Figure.6.
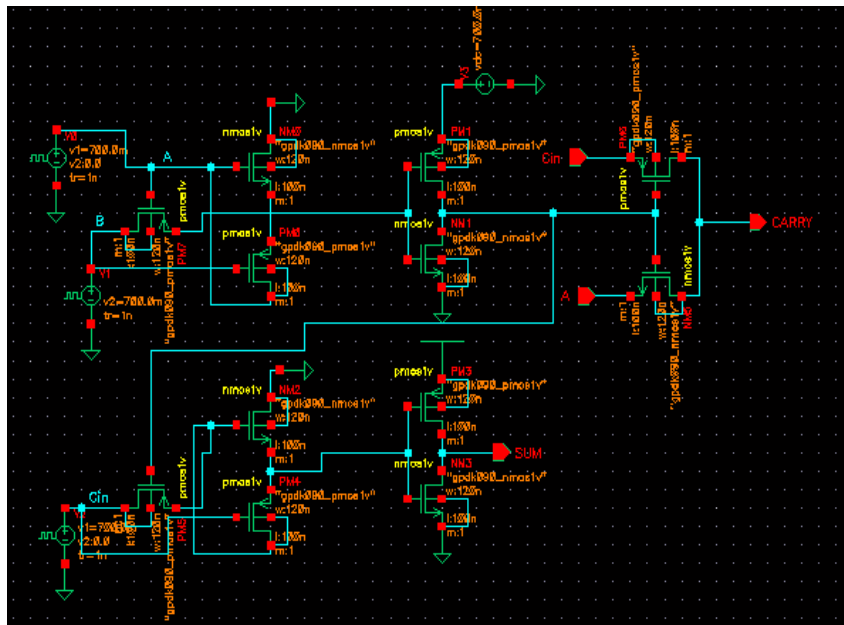

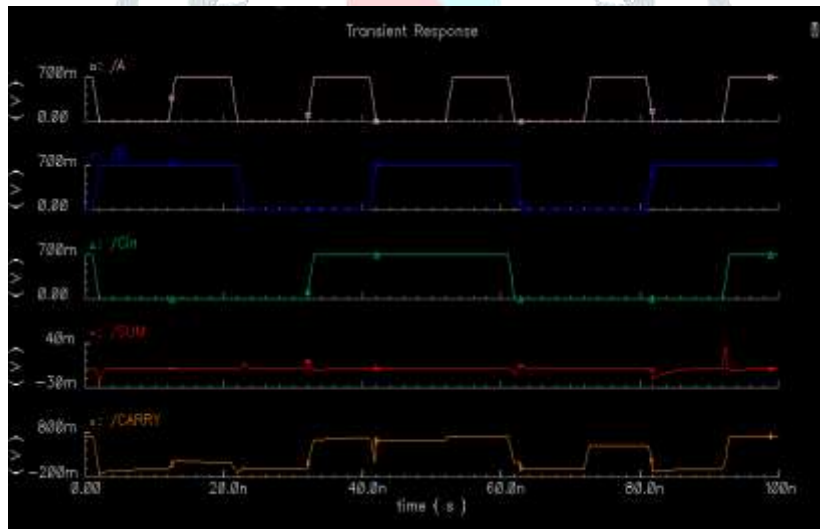
Figure.5 Schematic of 12T CMOS Full Adder

Figure.6 Transient Response of 12T CMOS Full Adder

III.   10T CMOS Full Adder

For the implementation of different 10 transistors CMOS FA circuits we required either 4 transistors XOR circuit or 4 transistor XNOR circuit and 2-to-I multiplexer. The schematic of 10T CMOS FA is appeared in figure 7 and the yield waveform is appeared in Figure 8.
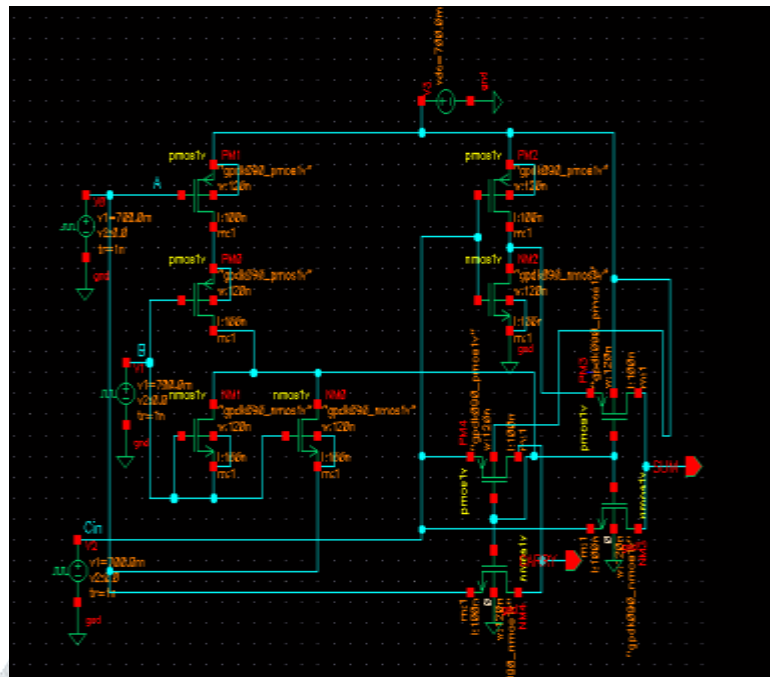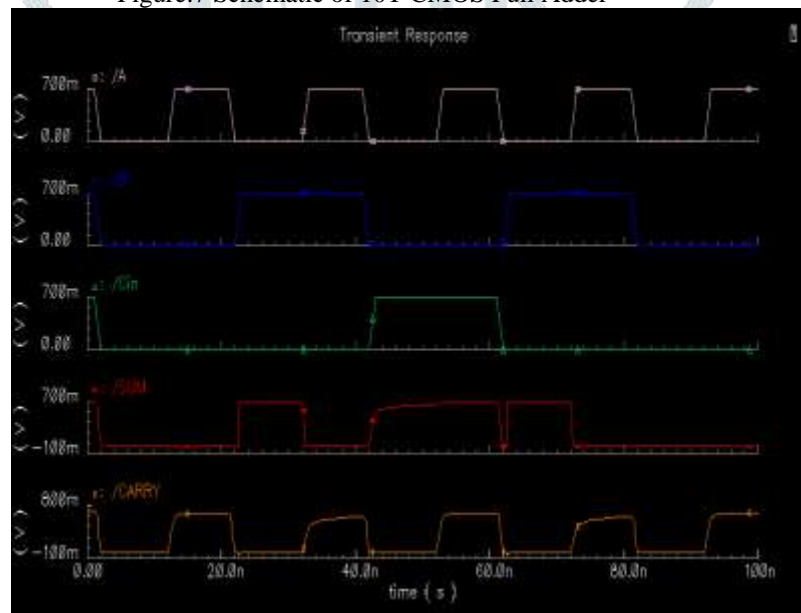
Figure.7 Schematic of 10T CMOS Full Adder

Figure.6 Transient Response of 10T CMOS Full Adder

IV.   9T CMOS Full Adder

In the paper [12], pre-format and post– design reenactments of another 9T FA cell at low voltages. The principle target of configuration was low power utilization and full voltage swing which was accomplished at low supply voltage. The proposed configuration demonstrated its predominance again existing snake as far as power utilization, power product delay (PDP), temperature maintainability and commotion resistance. So the FA with 9 transistor was displayed in that paper and we have picked and taken the same and has been contrasted it and different circuits and schematic 9T CMOS FA is shown in Figure.9 and Transient Response is given away in Figure.10.
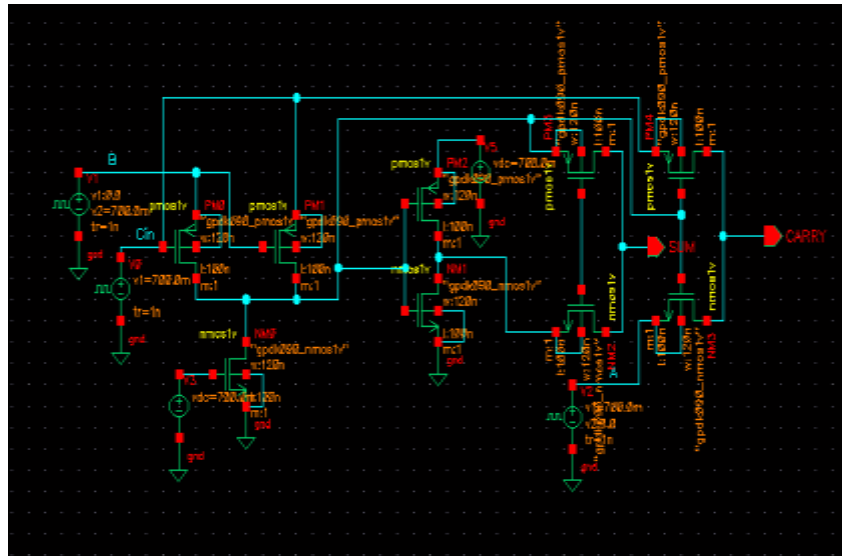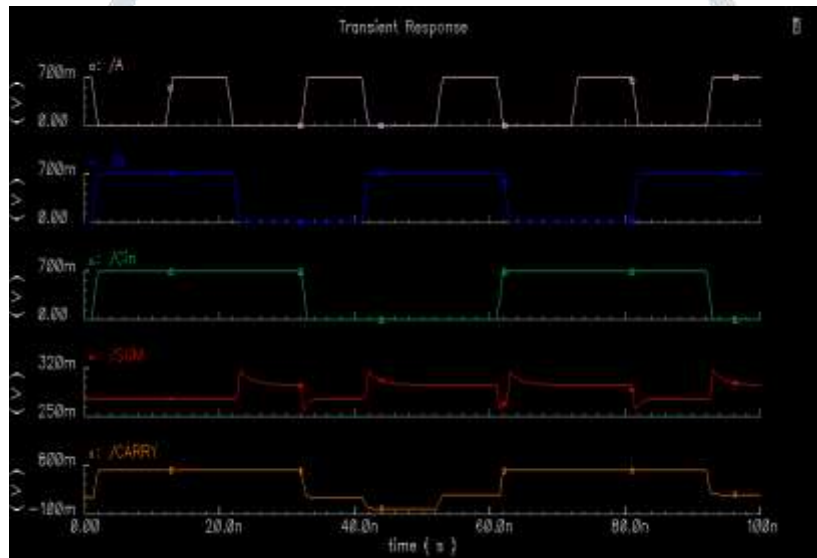
Figure.9 Schematic of 9T CMOS Full Adder

Figure.10 Transient Response of 9T CMOS Full Adder

4.   Simulation Result

Topologies of FA Simulation has been done on cadence tool using the 90nm and 45nm technology with a nominal supply voltage Vdd = 0.7 V. The gate leakage being the main predominant component at room temperature 27°C, distinct methods have utilized for decrease of intensity utilization and keeping up the execution of 14T CMOS Full Adder, 12T CMOS Full Adder, 10T CMOS FA and 9T CMOS Full Adder. Its comparative analysis of Topologies of CMOS FA the parameter like Leakage Current and leakage power is shown in below Table.1 respectively.

Comparative Analysis Result Summary of Topologies of CMOS Full Adder is shown below table 1 and table 2.

Table 1 Simulated Result Summary

Performance Parameter	14T CMOS Full Adder	12T CMOS Full Adder	10T CMOS Full Adder	9T CMOS Full Adder
Technology Used	90nm	90nm	90nm	90nm
Supply Voltage	0.7V	0.7V	0.7V	0.7V
Leakage Power	11.8μW	9.4μW	9.8nW	8.6nW
Leakage Current	13.6μA	8.7μA	8.6nA	7.9nA
Transistor count	14	12	10	9
Area Used	Large	Large	Less	Less

Table 2 Simulated Result Summary

Performance Parameter	14T CMOS Full Adder	12T CMOS Full Adder	10T CMOS Full Adder	9T CMOS Full Adder
Technology Used	45nm	45nm	45nm	45nm
Supply Voltage	0.7V	0.7V	0.7V	0.7V
Leakage Power	16.9nW	12.4nW	6.3nW	4.3nW
Leakage Current	14.5nA	11.5nA	7.8nA	6.4nA
Transistor count	14	12	10	9
Area Used	Large	Large	Less	Less

Conclusion

In this paper, topologies of CMOS Full Adder has been designed which is then analyzed. The leakage power consumption and Leakage current has been done in the circuit using different topologies. The designed CMOS Full adder Topologies are compared in phrases of leakage power, leakage current and surface area. We have planned and thought about 14T CMOS FA, 12T CMOS FA 10T FA and 9T CMOS FA regarding force and region. It eliminating diving capability problems present in other full adder modules, and it capture low power at 0.7V for it operation. From this correlation table 1and table 2, Topologies of CMOS full adder has minimal power utilization furthermore it is best as far as number of transistors required to design other full adder based combinational circuit. According to topologies, transistor count and power of 9T CMOS Full Adder is less and shows the better performance in comparison to other topologies of the CMOS Full Adder.

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