LEAKAGE CURRENT AND DELAY ANALYSIS IN DOIND-3, HIGH SPEED ACTIVE BODY BIASED AT 70NM TECHNOLOGY NODE

Seema chouhan
Asst. professor
Electronics & Telecommunication Engineering Department
IET-Devi Ahilya University, Indore-452017, Madhya Pradesh

Abstract: ***In VLSI memory circuits extensively used dynamic CMOS logic circuits. In comparison of static CMOS it has higher performance due to higher speed so it has less noise immunity and increased leakage power dissipation.***

Increase leakage current combine with reduced noise margin results in performance degradation of dynamic circuits. Design of dynamic circuit should be such that reduces leakage current and improve the noise margin.

In this paper active body biased DOIND-3 logic is proposed for domino logic which reduces the leakage current with minimum delay penalty. In this paper different Active body biased technique for DOIND approach namely DOIND-3 has been used to analyze different parameters.

Proposed DOIND-3 approach has maximum 84% improvement in leakage current among Domino and DOIND and DOIND-3 proposed technique as compare to domino logic circuit. Proposed DOIND-3 approach also has improvement in most of parameter as compare to all other approaches .In this paper effect of frequency variation in different circuits has been analyzed. All the parameter has been performed at 70 nm technology node using tanner EDA tool with supply voltage 0.9v.

Keywords- DOIND-3 Precharge, power dissipation, active body biased E, Domino logic and valuation.

INTRODUCTION

In the semiconductor industry has challenges to limits of traditional silicon CMOS scaling; the introduction of performance boosters such as novel materials and innovative device structures has become necessary for the future of CMOS scaling [11].

Low leakage current and noise immunity is big challenge for the new researchers. To improve the performance of portable systems and less power consumption in very high density VLSI chips result in quick and inventive growth of low power design. Higher power decay reduces the Battery life in battery operated applications and also reduces the reliability. The leakage Current increases drastically with each new technology inventions. In deep-submicron technologies Leakage power loss is a major problem because it drains the battery even when a system (Circuit) is completely idle. As scaling down the technology node, power supply and threshold voltage also roll down because power supply voltage and threshold voltage of MOS transistor is critical parameters to regulate the performance and switching speed of MOS devices.

In this paper domino logic Active Body Biased DOIND-3 (DOIND- **Do**mino logic with Clock and **IN**put **D**ependent transistors) Approach is used to analyze different parameter.

II. RELATED WORK

There are different techniques presented to control leakage current in domino logic circuits. When more than one transistor is turned OFF in series than sub threshold leakage current flowing through a stack of series transistors reduces [1]. This effect is known as stacking effect. When we increase the depth of stack more leakage current is observed. Width of Transistor (W) is replaced by two transistors by width of W/2 and this is called forced stacking effect.

INDEP approach [2] is the technique to reduce the leakage current in nanoscale circuit. In this approach used to extra inserted transistors between pull up and pull down networks that are basically input logic dependent methodology.

Leakage biased domino logic circuits [3] regulate the high speed with fine leakage reduction. This approach used to reduces fold steady state leakage current.

In the Lector Technique [4] two leakages control transistor (one PMOS and one NMOS) is introduce between pull-up and pull-down circuits within standard logic circuits. Here ensures that more than one of the LCTs operates in the near cut off region .The basic idea behind LECTOR approach is that "a state with more than one transistor OFF in a path from supply voltage to ground. Dual threshold voltage (DVT) DOIND Logic approach [5] low V_{th} transistor is chosen in critical path while high v_{th} transistors are chosen in noncritical path. In this methods DOIND transistors used in active and sleep mode while low V_{th} transistors and high V_{th} are used to reduce leakage current in the sleep mode.

A novel Leakage reduction DOIND Approach [5] for nanoscale Domino logic circuits uses Domino logic with clock and input dependent transistors. In this logic two transistors connected between precharge and pull down networks. All the body terminal of PMOS transistors connected to V_{dd} and Body terminal NMOS transistors connected to Gnd.

Sleep switches DVT DOIND logic circuit based buffer approach [8] reduce the subthreshold leakage current in both active and sleep mode of DOMINO Logic circuits. High v_{th} NMOS sleep switch is associated to dynamic mode and the procedure is commanded by extra sleep signal.

Active body biased DOIND-3 approach uses one active biased circuit ABC-3 into the DOIND Logic circuits [5]

III DYNAMIC LOGIC CIRCUITS

I. Domino Logic circuits

DOMINO logic circuits are shown in fig. 1. The operation of the circuits is follows in this manner when the clock signal is getting low; the domino logic circuit is in precharge phase. In the precharge phase, the node N1 is charged to Vdd thro MP1.Vout of the circuit is low which turn on the keeper transistor (MP2), when the clock signal is getting high signal, the whole circuit dig up into the evaluation phase. In this mode combinations of input from the pull down network dynamic node N1 is discharged to ground or remain high.

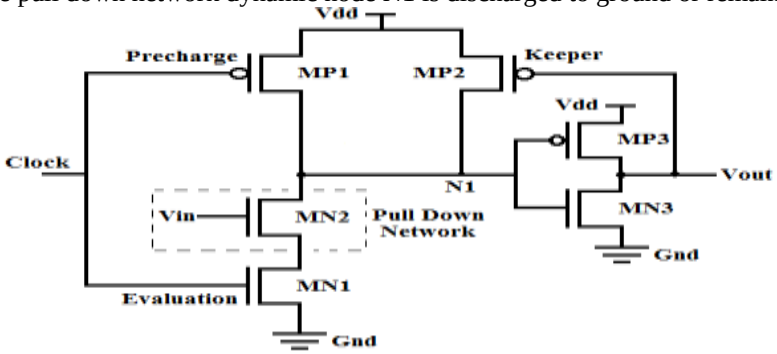


Fig.1: Domino Logic circuit

The inverter output voltage can also make one transition during the evaluation phase from 0 to 1.

Inverter input with output voltage and week keeper transistor are always used to avoid charge sharing and cascading problem. Performance degrades by adding keeper transistor. Big size of the keeper transistor enhances toughness at the cost of delay and power dissipation and small sized keeper is desired for high speed and low delay device. So here is agreement between delay and power to improve noise quality and leakage immunity.

DOIND Logic

In the **Do**mino logic with Clock and **IN**put **D**ependent transistors (DOIND) logic circuit is shown in fig.2. It has two transistors namely DOIND MP4 (PMOS) and MN4 (NMOS) connected between A and B terminals. Gate terminal of DOIND transistors (MP4 and MN4) are inputs V0, V_{IN} and V1 which are the one clock and three input logic dependent.

Body terminal of all PMOS transistors are connected to Vdd and Body terminal of all NMOS transistors are connected to Gnd. When the clock signal is low, then V0 should be 0 (low) so that MP4 and MP1 is turn on and the DOIND logic circuit comes in precharge phase, when the node N1 is charged to Vdd through MP1and MP4 with the clock signal it's in Precharge Phase. Output voltage of the circuit is low which turn on the keeper transistor that is MP2. When the clock signal is high, the circuit enters into the evaluation phase. In evaluation phase, when input Vin = 1 (high) then V1 should be 1 so that dynamic node N1 becomes 0 and when input Vin = 0 (low) then V1 should be 0 so that dynamic node N1 becomes 1.

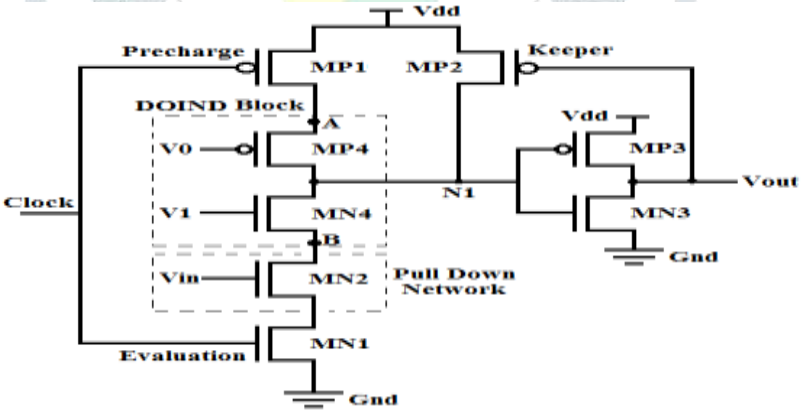


Fig.2: DOIND Logic circuit based buffer

IV. Adopting body biasing DOIND logic

In this paper we proposed DOIND-3 (**Do**mino logic with Clock and **IN**put **D**ependent transistor with **A**ctive **B**ody Biasing) ABC3. IN the static circuit's the body of SOI partially Depleted MOSFET biased to control the threshold dynamically.

III (a): DOIND-3 Technique

A proposed DOIND-3 logic circuit is shown in fig.3. Here two DOIND transistors MP4 (PMOS) and MN4 (NMOS) connected between A and B. Gate terminal of DOIND-3 transistors (MP4 and MN4) with voltage V0 and V1 which are clock and input logic dependent respectively. Body biasing transistor MP5 (PMOS) has connected in the body transistor MP4 (PMOS). Gate terminal of PMOS transistor MP5 connected to the source terminal of PMOS transistor MP4, Source terminal of PMOS transistor MP5 connected to the gate terminal of PMOS transistor MP4. Drain terminal of PMOS transistor MP5 connected to the Body of the PMOS transistor MP4. Body biasing transistor MN5 (NMOS) connected with the body terminal of Transistor MN4 (CMOS).

NMOS transistor MN5 biased with the NMOS transistor MN4. Gate terminal of NMOS transistor MN5 connected to the drain termina1 of the NMOS transistor MN4 and drain terminal to the gate terminal of the NMOS transistor MN4 and source terminal connected body

terminal of the NMOS transistor MN4. Body terminal nodes of all PMOS transistors are connected to the power supply V_{dd} while Body terminal of all NMOS transistors are connected to ground terminal (G_{nd}).

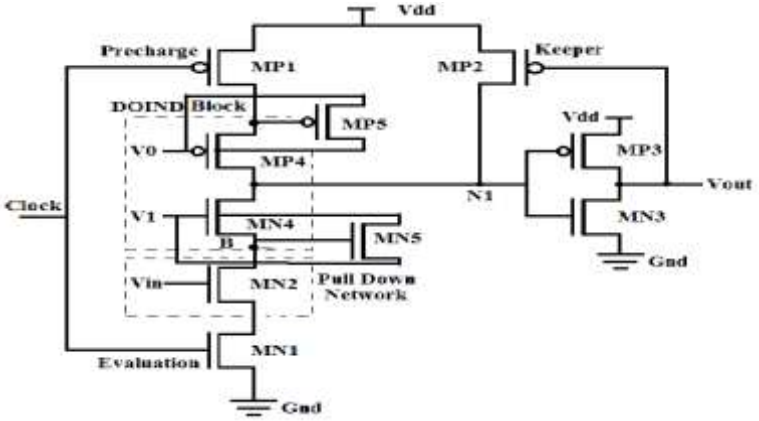


Fig: 3: DOIND-3 Logic circuit

The working operation of DOIND-3 logic circuit is in the following manner .When the clock signal is low, and then V0 should be 0 (low) so that MP1, MP4 and MP5 is turn on and the DOIND-3 logic circuit set in precharge phase. When the node N1 is charged to V_{dd} through MP1, MP4 and MP5 the logic circuit going to precharge phase. Output votage (Vout) of the circuit is low which turn ON the keeper transistor (MP2). When the clock signal is set to high or 1, the transistor (MN1) goes into the evaluation phase. In evaluation phase, when input V_{IN} = 1 (high) then V1 should be 1 so that dynamic node N1 becomes 0 and when input Vin = 0 (low) then V1 should be 0 so that dynamic node N1 becomes 1. Functional status of each transistor is given in table.

Table: III.(a): functional detail Table of DOIND-3 Logic:

Clock	**MN1**	**MP1**	**Input (Vin)**	**MN2**	**MP2**	**Clock**	**MN4**	**MP4**	**Input (Vin)**	**MN5**	**MP5**
Logic 0	OFF	ON	Logic 0	OFf	ON	Logic 0	OFF	ON	Logic 0	OFF	ON
Logic 0	OFF	ON	Logic 1	ON	ON	Logic 0	OFF	ON	Logic 1	OFF	ON
Logic 1	ON	OFF	Logic 0	OFf	ON	Logic 1	OFF	OFF	Logic 0	OFF	OFF
Logic 1	ON	OFF	Logic 1	ON	OFF	Logic 1	ON	OFF	Logic 1	ON	OFF

(a) Functional Table of DOIND-3 Logic

When clock signal going to low with input pulse 0, PMOS Transistor MP1, MP4, MP5 and keeper transistor MP2 turned ON and transistor NMOS MN1, MN2, MN4 and MN45 going to Evaluation phase. When clock signal getting a logic 0 with input pulse 1 , the transistor MP1 ,MP2, MP3 and MN2 going to ON and Transistor MN1 and MN4 is turned OFF.

1. Impact on Leakage Current

In the CMOS circuits power dissipation is the big obstacle and high leakage current regimes is becoming a significant contributor to the circuits as channel length, threshold and gate oxide thickness are reduced.

Therefore, the description and modelling of different leakage components is very extensive for estimation and reduction of leakage power, especially for low-power applications. Relation between leakage current and threshold voltage is given by [5]

$$I_{Leakage} = I_0 \frac{(Vgs-Vth)}{\eta Vt} (1\text{-}\exp \frac{-Vds}{Vt})$$

Where Vgs is gate to source voltage; I_0 is saturation current, and η is sub-threshold slope factor and V_t is drain to source voltage.

Table III.(b) .impact on leakage current

logic design	**Clk=0, Vin=0**	**Clk=0, Vin=1**	**Clk=1, Vin=0**	**Clk=1, Vin=1**	**Improve In %**
Domino	0.307	1.595	2.262	2.126	
DOIND	0.160	0.307	0.127	0.258	86%
DOIND-3	0.160	0.307	0.306	0.259	84%

Graph clearly indicate that DOIND logic show a 86% low leakage current than a DOMINO logic but Active body biased DOIND-3 has 84% low leakage current than DOMINO Logic.

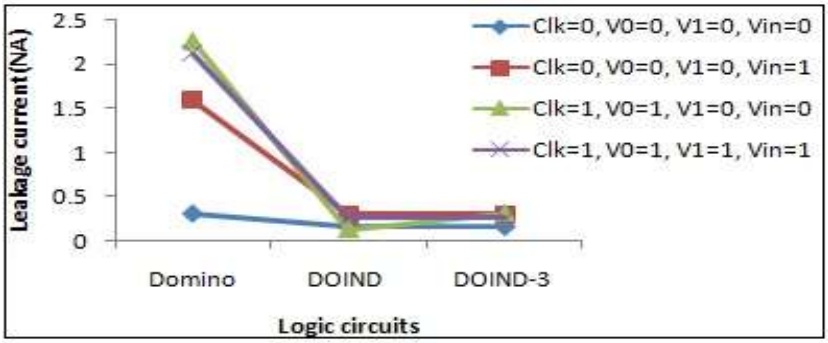


Fig.4: Leakage current for clock=0 and clock=1

2. Impact on Static Power :

Table :III(b) shows that DOIND-3 logic circuits has better in static power control with different input logic combinations with both clock=0 and clock=1. DOIND logic 86% better than Domino logic but DOIND-3 also 95% give the better performance than Domino logic.

Table III (c) : static power depends on the combination of Clock input and input voltage.

logic design	Clk=0, Vin=0	Clk= 0, Vin= 1	Cl k = 1, Vin= 0	Clk =1,Vin=1	% improve
Domino	0.2763	1.4356	2.036	1.913	
DOIND	0.1448	0.2762	0.115	0.232	86%
DOIND-3	0.00037	0.00042	0.157	0.118	95%

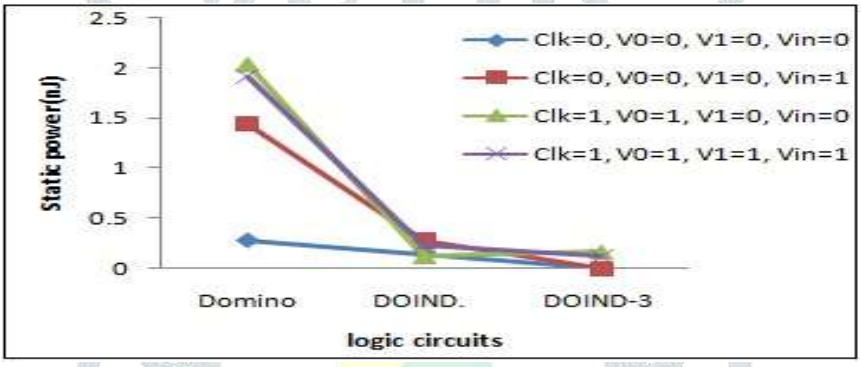


Fig.5 Static power for clock=0 and clock=1

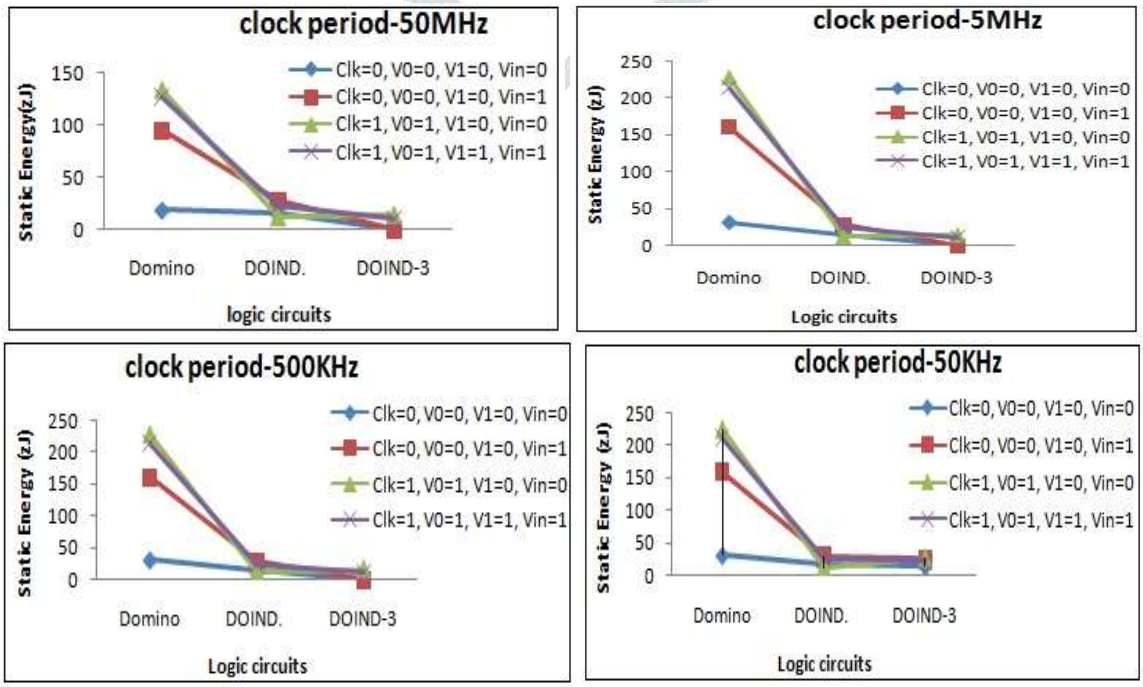
3 . Impact on Static Energy

Static energy element is directly proportional to Vdd [12] so static energy is represented as

$$E_{Static} = I_{Leakage} V_{dd} T_{delay}$$

Where T_{delay} is circuit delay and $I_{Leakage}$ is leakage current.

4. Static Energy at different frequency:-



DOIND-3 control the static Energy at 50MHz, 5MHz, 500 KHz and 50 KHz approximate 93%, 96%, 96% and 86% than Domino logic circuits.

4. Impact on Static PDP:

Static power delay product (PDP) is given by[9]

$PDP_{static} = E_{static} \times T_{delay}$

DOIND-3 logic have 93% better performance at the 50MHz but on remaining frequency at 5MHz, 500KHz and 50kHz it is no performed better than Domino and DOIND logic circuits.

5. Impact on Delay:

In most designs there will be many logic paths that do not require any conscious effort when it comes to speed. There will be usually a number of paths, known as the critical paths that needed attention to timing related details. These all process can be recognized by timing simulation, but most of the designers use a timing analyzer, which is a design tool that automatically searches the slowest paths in a logic design.

Table; 4.10: Delay at different clock frequency

	Clock frequency							
	50MHZ	**% improve**	**5MHZ**	**% improve**	**500KHZ**	**% improve**	**50KHZ**	**% improve**
Domino	65.68		111.6905		**500KHZ**	**% improve**	**50KHZ**	**% improve**
DOIND.	99.5	-51%	102.5	8%	111.6905		110	
DOIND-3	87.954	-34%	88.275	-719%	104.4	7%	104.5	5%

DOIND-3 logic has poor performance at the 5MHz frequency its aprrox -719%, and at the remaining frequencies 50MHz, 500KHz and 50Khz DOIND-3 gives a -34%, 13%, and 15% better improvement than Domino logic.

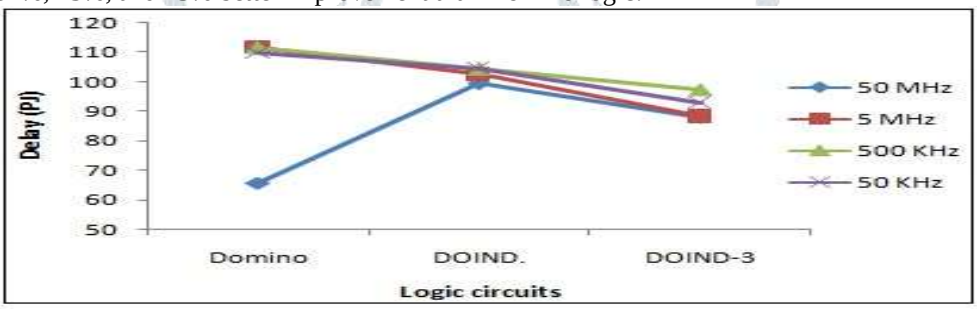


Fig.6. Delay at different clock frequency

6: impact on Dynamic Energy

When we used Dynamic power it is power consumed when the supply inputs are active. When supply inputs use ac activity, capacitances are going to charging when find positive pulse supply and discharging when it's getting negative pulse supply and the power increases as a result. Dynamic power consist of both the ac component and also static component.

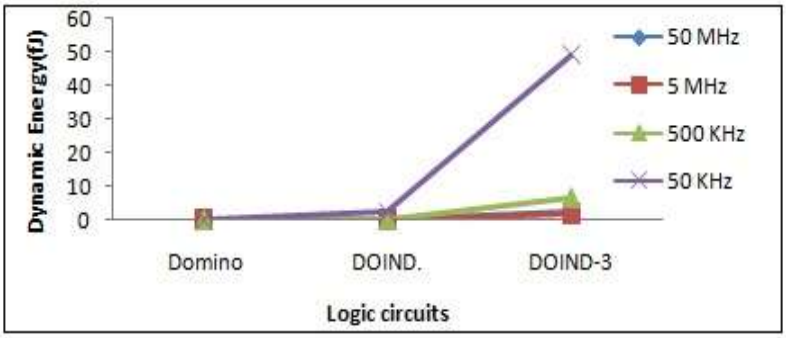


Fig.7 Delay at different clock frequency

DOIND-3 has a dynamic energy better performance at the 50MHz and 5MHz and it is 83% and 95% but it has degraded the performance at the 500 KHz and 50 KHz.

IV.SIMULATION RESULT

IN this paper all the parameter are tested with the EDA tanner for domino logic, DOIND and DOIND-3 approach with supply voltage 0.9V.

V.CONCLUSION AND FUTURE SCOPE

In VLSI design, Leakage power dissipation becomes major concern. In the portable device Leakage current drained the battery. Even the circuit is work in idle mode or while it is reset. Unnecessary power consumption is held without operating the device. This research paper represents the supplement of the work and future extension of the new technology.

This research work target on adoptive active body biased technology for DOIND approach. Proposed DOIND-3 has maximum average improvement in leakage current of 84% among all other circuits. All three circuits have been analysis at four different clock frequency 50 KHz, 500 KHz 5 MHz and50MHz respectively.

Leakage current, static power delay product (PDP), Static Energy, dynamic EDP, dynamic power and dynamic PDP of all the circuits are analyzed at all the four frequencies.

Here we use the 70nm technology node for analysis the circuits but it can be different node technology may be applied.

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