

High Speed Low Offset Low Kick Back Noise Dynamic Latch Comparator for ADC

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Abstract: This paper describes the implementation of 10 bit high speed low offset and low kickback noise dynamic latch comparator with preamplifier in 65nm CMOS technology. Dynamic latch comparator which uses a positive feedback mechanism to generate the analog input signal to a full scale digital level. Kick back noise and offset voltage are the parameter which effects its performance, these can be reduced by playing preamplifier before dynamic latch comparator. The simulations of preamplifier based dynamic latch comparator are performed at 6 GHZ maximum clock frequency, with power consumption of 3.24mw at 1.2v supply voltage and offset voltage is reduced to 1.4mv. Monte Carlo simulations are carried out with N no of runs (N=100) where standard deviation and mean values are obtained.

IndexTerms – ADC, CMOS, Kick Back Noise, Offset Voltage

I. INTRODUCTION

Analog signal is a continuous wave that keeps on changing over a time period. To convert the analog signals like voltage, current, temperature, pressure into digital i.e. binary signals, the most widely used electronic component is the analog to digital converter (ADC). In real time DSP applications high speed and low power consumption ADCs are used. According to the speed, different interfaces and degree of accuracy different types and classifications of ADCs are present. The most common types of ADCs are flash, successive approximation, and sigma-delta. The performance of the analog to digital converters with high speed of operation mostly depends on comparators. The basic operation in any analog to digital converter is comparison. This comparison operation is performed by comparators. A comparator consists of specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters [1].

The paper is organized as follows: section II describes about the existing methods and section III describes about the proposed methodology and the architecture and then follows the simulation results and the comparison table.

II. EXISTING METHOD

One of the architecture which is used to reduce kickback noise composed of dual differential amplifier in the input stage with current mirror load & output signals are mirrored to followed dynamic latch circuit even though it reduces the kickback noise to maximum extent but the offset voltage is not reduced and also this system is operating at frequency of 500 MHz [2].

Another Existing kickback noise reduction technique which uses MOS switches that are opened during the regeneration phase and this performs a sampling function thereby isolating input nodes thus eliminating kickback noise during that phase. However input nodes are still disturbed when switches close. So these cannot completely solve problem [3].

Use of neutralization technique, Firstly kickback noise is generated when the large voltage variations in the regeneration nodes are coupled through the parasitic capacitances of the transistors to the input. We need to add capacitances to neutralize and to cancel kickback noise. But just neutralization technique cannot solve problem it should be combined with other techniques to get more effective [4].

A fully differential amplifier which is base on Lewis-Gray dynamic comparator reduces offset voltage without preamplifier but it operates at speed of 50 MHz

2.1 Kick Back Noise

Kick back noise is the large voltage variations in the internal nodes are coupled to the input and disturbing the input voltage. To reduce this kick back noise and the offset voltage in the dynamic latch comparator preamplifier is used in the proposed method. Kick back noise uses a positive feedback mechanism to regenerate the analog input signal into a full scale digital level.

2.2 Offset Voltage

The differential input voltage that must be applied to an operational amplifier to return the zero frequency output voltage to zero volts, due to the mismatching at the input stage.

III. PROPOSED METHODOLOGY

3.1 INTRODUCTION

A latch comparator architecture containing preamplifier circuit with finite gain and a positive feedback and a regenerative latch is illustrated in the following figure 1. The working process of a latched comparator is divided into two stages. In tracking stage latch circuit is disabled and their input analog differential voltages are amplified by the preamplifier. In the latching stage while the preamplifier is disabled, the circuit generates the amplified differential signal into pair of full scale digital signals with positive feedback mechanism and latches them to output ends.

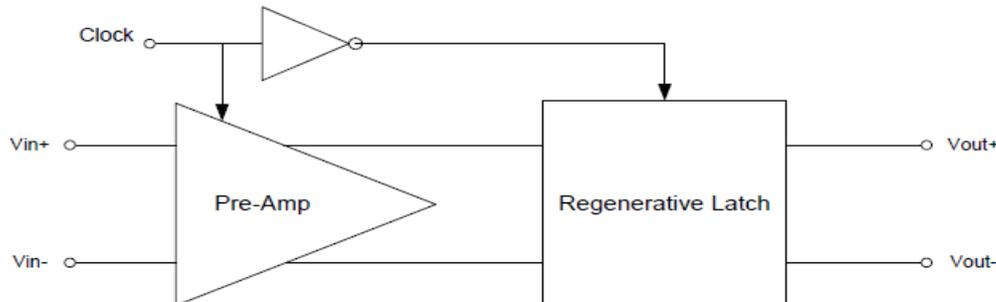


Fig 1: Typical Block Diagram of Comparator

3.2 ARCHITECTURE

Among the different architectures of comparators like Static comparator, class AB comparator, Dynamic latch comparator. Dynamic latch comparator is chosen because it eliminates the problem of static power consumption, introduction of two poles at intermediate node and in regeneration nodes and also the slow regeneration process that occurs with static comparator and the important feature with dynamic latch comparator is it is more power efficient and fastest comparator.

The limitation of these dynamic latch comparator is it generates more kickback noise and offset voltage, and it is also concluded that more power efficient and fastest comparator generates more kickback noise. These two parameters can be reduced by placing PREAMPLIFIER before dynamic latch comparator.

Several other techniques are used to reduce the kickback noise are placing MOS switches and isolating input nodes, but the input voltage are still disturbed when switches are closed. Neutralization technique is also used to reduce kickback noise by placing clocked capacitors. All these techniques cannot completely achieve a truly effective kickback noise and offset reduction. Preamplifier based dynamic latch comparator provides better results compared to that.

Proposed Dynamic latch comparator with preamplifier schematic is shown as below. It consists of three stages preamplifier, Dynamic latch comparator and SR latch. The proposed block diagram is shown in figure 2.

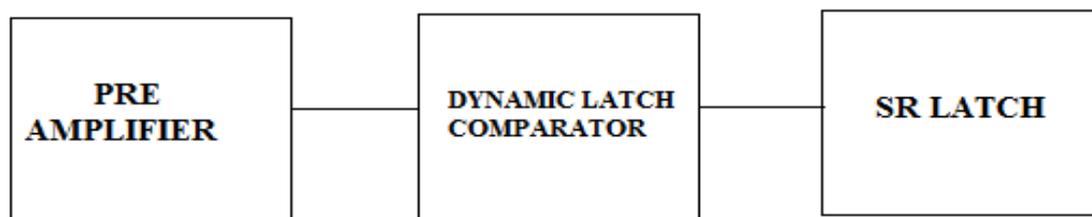


Fig 2: Block diagram of Dynamic Latch Comparator with Pre Amplifier

3.2.1 PREAMPLIFIER

The first block in the above figure is Preamplifier, Preamplifier stage is used to decrease the offset voltage and it can also amplify a small input voltage difference to large output voltage it improves the comparator sensitivity and isolates the input of comparator from switching noise often called kickback noise. Thus this large output voltage overcome offset voltage which in turn reduce kickback noise.

Differential amplifier is used as a Preamplifier with resistive load 10kohms with wide bandwidth and relatively small gain to achieve high speed. Differential amplifier which provides effective input stage in the high gain amplifier is one of the most essential circuit inventions. Differential amplifier since it is used in high performance analog and mixed signal circuits it has become the most important choice.

Differential signal voltage is measured between two nodes which have equal and opposite signal with respect to fixed potential where as single ended voltages are measured with respect to fixed potential i.e., common mode (CM) level as shown in the fig 3.

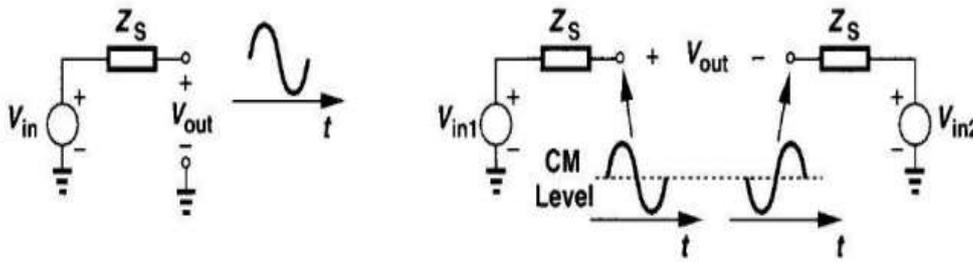


Fig 3: Single Ended and Differential Signals

In terms of differential and common mode, output voltage is given as

$$\begin{aligned}
 V_{OUT} &= A_{VD}V_{ID} \pm A_{VC}V_{IC} \\
 &= A_{VD}(V_1-V_2) \pm A_{VC}(V_1+V_2)/2 \quad (1)
 \end{aligned}$$

Where A_{VD} is the differential mode voltage gain and A_{VC} is the common mode voltage gain.

3.2.2 DYNAMIC LATCH COMPARATOR

Dynamic latch comparator which is fastest and power efficient comparator in which the current only flows during regeneration, whereas other comparators have supply current in the reset phase and after regeneration finishes. Dynamic latch comparator consists of two cross coupled CMOS inverters used for regeneration.

OPERATION

Consider N-type latch comparator circuit as shown in the figure 4. When the clock signal is low reset transistors M7 and M8 are ON and charge the output nodes as well as the output nodes of input transistor to supply voltage, current source transistor Mtail will be OFF. Thus no current flows during reset phase. When the clock signal is high the reset transistors disabled Mtail transistor will be ON. The cross coupled inverters receive different amount of current depending on the input voltage and start to regenerate the comparator output when they receive input drain voltage V_d of M1 & M2 discharge VDD to ground once V_d drops below $V_{DD}-V_{TH}$, NMOS transistor of inverter is turned ON output starts discharge and positive feedback is activated. This positive feedback of LATCH is used to determine which of the inputs signal is larger which is received from preamplifier stage of comparator and extremely amplifier difference this difference is send to the output stage. Once the output voltage is $V_{DD}-V_{TH}$, PMOS of other inverter is ON and output voltage is regenerated and after regenerated one of the output is 1 and other is 0.

Drain nodes voltage variations produce kickback noise that is eliminated by placing preamplifier

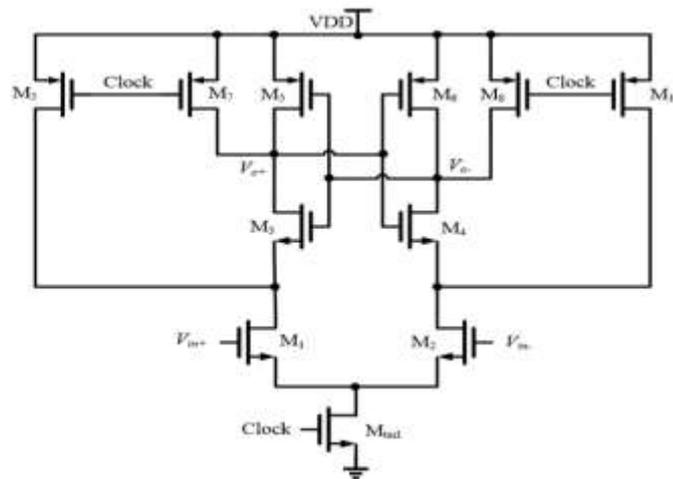


Fig 4: N-type latch comparator circuit

Before preamplifier dynamic latch comparator is operating at a clock frequency of 1GHZ initially, and then by increasing the (W/L values) currents in dynamic latch comparator transistors we achieve speed up to 3GHZ.

Table 1: Showing Different (W/L) Multiplier Values for Different Frequencies

S NO	CLOCK FREQUENCY	MULTIPLIER VALUES	
		Differential amplifier(120/4) (W/L)	Inverter (120/1) (W/L)
1	1GHZ	2	1
2	2GHZ	4	1
3	2.5GHZ	6	2
4	3GHZ	8	4
5	3.5GHZ	10	6

IV. SIMULATION RESULTS

The below table 2 shows the increase in clock frequency from 3.5GHZ to 6 GHZ the corresponding offset voltage also increased from 2mv to 7 mv.

Table 2: Offset Voltage with Increase in Clock Frequency

S.NO	CLOCK FREQUENCY	OFFSET VOLTAGE 1
1	3.5GHZ	2mv
2	4GHZ	3mv
3	5GHZ	4mv
4	6GHZ	7mv

To reduce the offset the same speed is maintained at 6GHZ and by increasing the W/L of differential amplifier the offset is reduced from 4.3 mv to 1.3mv and is shown in below table 3

Table 3: Offset Voltage with Increase in W/L Values

SNO	DIFFERENTIAL AMPLIFIER (W/L) m	OFFSET VALUES
1	2	4.3mv
2	6	1.8mv
3	8	1.6mv
4	10	1.5mv
5	14	1.3mv

The transient analysis of the offset voltage is shown in below figure 5. The input to the amplifier is the ramp input and the offset voltage for the positive level is shown with and without preamplifier. The positive slope offset is 1.4mv.

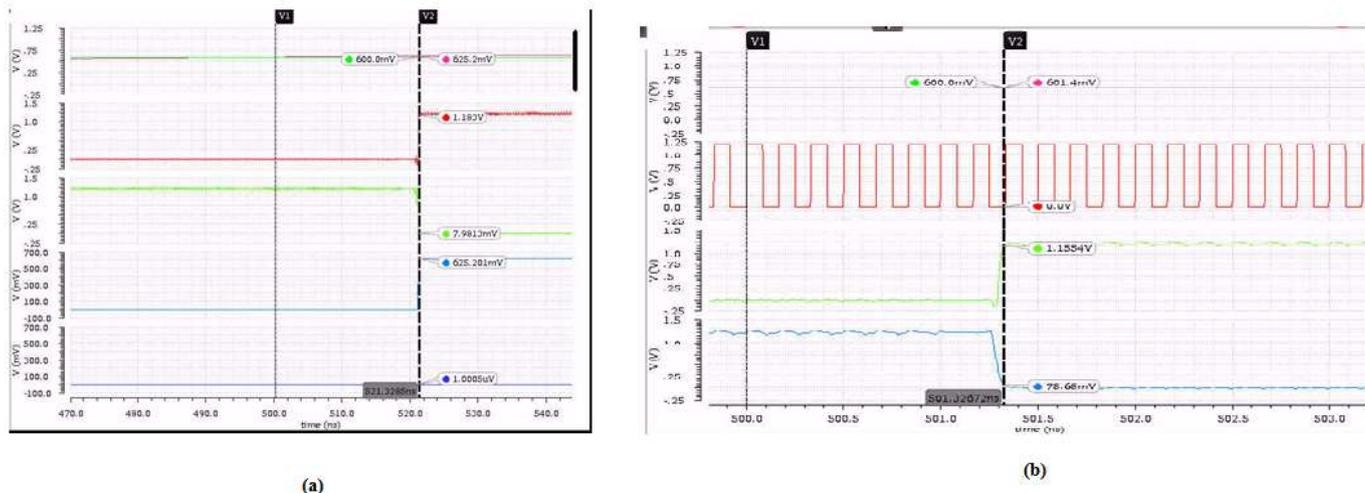


Fig 5: Transient Analysis (a) Offset Voltage without Preamplifier (b) Offset Voltage with Preamplifier

By the addition of preamplifier kickback noise is also reduced. The comparison of the kickback noises with and without preamplifier as shown in the following figures.

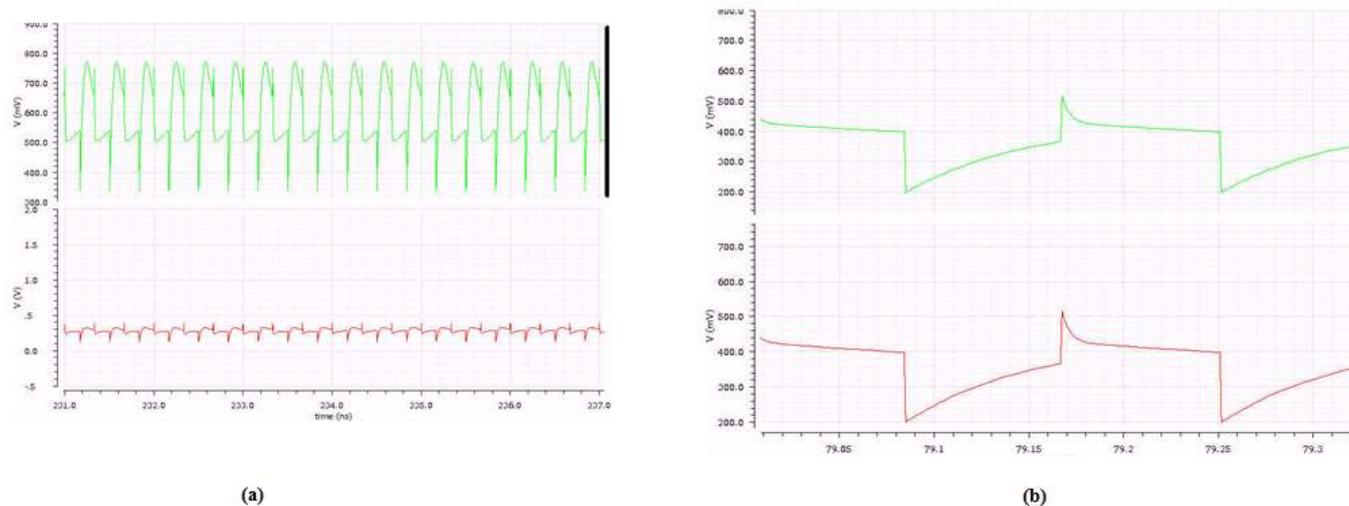


Fig 6: Kick Back Noise (a) Without Preamplifier (b) With Preamplifier

Monte Carlo simulations are carried out with N no of runs (N=100) fig 7 shows histogram plots and calculated standard deviation and mean values. Monte Carlo simulations are computerized mathematical technique –possible outcomes and the probabilities and are used to calculate offset at different runs & mean and standard deviations of complete runs.

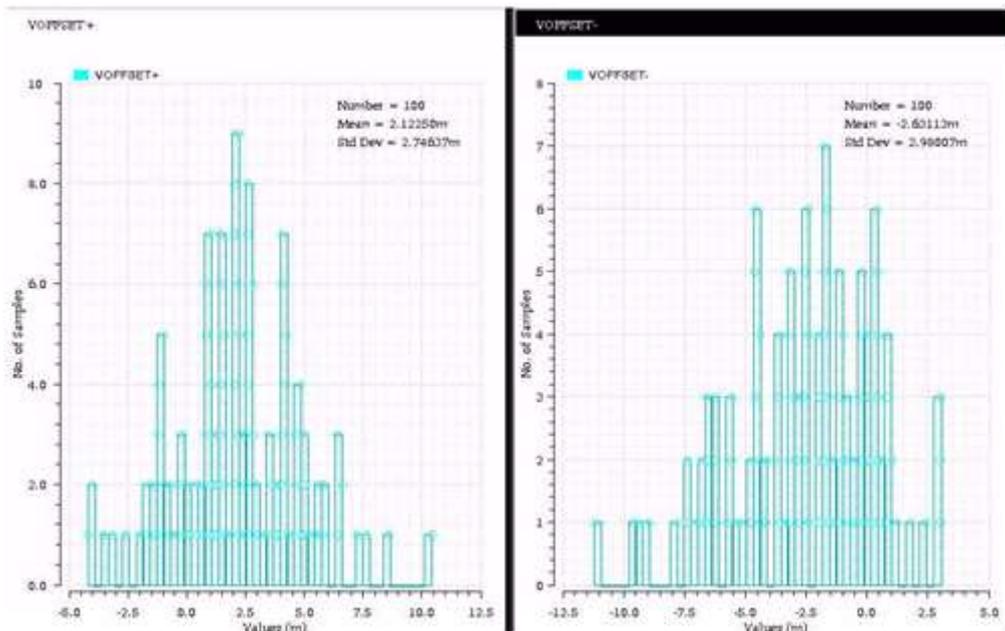


Fig 7: Offset Voltage for 100 runs

CONCLUSION

This paper proposed an improved comparator with low offset voltage and low kick back noise and therefore high speed is achieved to 6GHZ and offset voltage is reduced to 1.4mV and kickback noise is reduced to maximum extent. The project has been successfully simulated using the cadence tool and the results are shown using the Monte Carlo simulation for 100 runs.

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