Simulation of Bridgeless Converter in Total Harmonic Reduction by using Fractional Order PID Controller

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Abstract: Generally our computer loads and systems are found in industries commercial and residential units. The nature of loads may destroy the line current wave forms and supply voltage wave forms. With these loads consisting of poor power quality and slow dynamic response, more total harmonic distortions. The voltage controller in the SMPS consist of PI controller, with the effect is that it has high starting over shoot, sensitivity to control the gain and sluggish response to sudden change in the system to reduce the difficulty level here is used to non isolated bridgeless buck-boost single ended primary inductance converter in discontinuous conduction mode at input side of SMPS. With fractional order PID controller at PFC and continuous space voltage regulation. The SEPIC with FOPID controller is provided constant output voltage for load changing and input voltage varies. The output of SMPS gets different output voltages and it multiplies dc to dc converter maintain the single output voltage and varies with all other output voltages. The design in simulation of bridgeless converter in total harmonic reduction by using FOPID controller can be verified.

Keywords: FOPID controller, SEPIC, half bridge dc to dc converter, SMPS, THD, Improved power quality, computer power supply.

I INTRODUCTION

There are many electronic components and devices are powered for their service. In this we have to use ac to dc rectifier in which we are using diode bridge rectifier and large electrolyte capacitor and inductor is used. The absorbing and delivering capability of changing inductor and capacitor will create a problem. For sudden change in current and voltage the capacitor and inductor values will produce harmonic current against the international power standard limit.

Modern ac to dc converter:

By using the modern ac to dc converter which improves the voltage regulation and efficiency. With the help of these converters it is inconvenient to power factor correction and harmonic current reduction at point of common coupling. Our electronic devices or components are most affected by power disturbance. To reduce the power quality problem we are using single and two stage power conversion.

Single stage power conversion:

Two stage power conversion:

By using two stage power conversion good efficiency and good regulation and dynamic response. It avoids the second harmonic component of current in single stage. So with that advantage we can reduce the large value of electronic components like inductor and capacitor. More number of front end converters are used to provide PFC and output voltage regulation. Generally boost converter is used to electronic devices power supply maintenance but boost converters cannot be employed for voltage less than 300 volts for input supply 230 volts ac. To operate the electronic devices in regular manner we use the boost converter

Controllers:

The voltage controllers are used in SEPIC device and isolated half bridge dc to dc converter. This voltage controllers operating at independent to each other. In this we can be implemented PI voltage controller. The PI controller is also called as a reset controller. Due to this converter zero error occurs at output at load changes it can be reset easily. By using this PI controller type of the system increases, accuracy improved and final error decreases. This voltage controller is used to PFC and voltage regulation and THD within permissible limit. By using PI controller in PFC and THD it has to provide steady state response improved and error is reduced. With this PI controller the band width of the signal is reduced and rise time increases and system speed decreases and over all transient response of system is sluggish in nature. To improve the performance of the controller in this paper we have to introduce the fractional order PID voltage controller

II SMPS DESIGNING AND WORKING PRINCIPLE

In this proposed converter it is divided mainly in to two parts. One is the Bridgeless front end ac to dc converter and another is multi output dc–dc converter. Converters are
operated in two modes of operation as continuous conduction mode and discontinuous conduction mode. By using the continuous conduction mode of operation it has required two voltages and one current measurement are required. So the cost of the equipment is high and design of controller is large. To mitigate the problem of continuous conduction mode we can implement discontinuous conduction mode of operation principle. With the implementation of DCM of operation the converter is required is only one voltage measurement.

**SMPS Design:**

The proposed system consists of four regulated dc output voltages at the input side two SEPIC are used with FOPID voltage controller and eliminated by diode bridge rectifier. these two SEPICs will be divided into two groups as upper converter and lower converter. The positive half cycle the upper converter will be operated and the negative half cycle lower converter is operated. To operate the converters 20 kHz frequency is taken as reference for both. In DCM mode of operation the output value of inductor is measurable. The input voltage and load parameters will vary in preferable manner to maintain the constant output voltage. The output voltage (V_pfc) in SEPIC is sensing and compare with reference (V_{ref}) from which voltage error is obtained. This voltage error is again compared with FOPID voltage controller output is compared with PWM pulses by voltage comparator. It consists of two switching conditions. If V_{cc} is greater than S_t then V_{cc} is positive and upper switch S_p is turned on and another is V_{cc} is less than S_t then V_{cc} is negative and lower switch S_n is turned on. The width of the PWM pulses can be varied accordingly to maintain the constant output dc voltage. The regulated V_pfc voltage is maintained constant and given input to isolated half bridge dc to dc converter. In this front end converter a multi winding high frequency transformer is used for isolation purpose. Generally high frequency transformer the conduction losses are more. To reduce the conduction losses the central tapped winding is used. One closed loop is required to maintain the secondary winding voltages are constant. The highest voltage produced by HFT is taken as measurable value or control unit.

![Schematic diagram of fractional order PID voltage controller based SMPS.](image1)

![Fig: 2 positive voltage operation of FOPID voltage controller](image2)

![Fig: 3 operating modes FOPID voltage controller in the upper convetor operation](image3)

In dc–dc half bridge converter one FOPID voltage is used and compared with reference voltage(V_{ref}). The output of voltage controller is again fed to voltage comparator with reference of PWM pulses S1 and S2. In continuous conduction mode of operation there is dead time between ON and OFF switches otherwise there is occurrence of shoot through fault. To regulate dc output voltages the load changes, duty cycle and output voltage changes.

**Working Principle:**

1) **SEPIC operating principle:**

The operating principle of SEPIC is divided in to two cycles. The upper converter of SEPIC is operated at positive half cycle of input voltage and lower converter of SEPIC is operated at negative half cycle if input voltage. For one PWM switching signal the operation of SEPIC will be described as three modes of DCM operation. In the first mode of operation the switch S_p turns ON the primary inductance L_{p1} starts storing the energy and diode d_{p1} completes the current path. in second mode of operation switches S_p is turns OFF and diode d_{p2} starts conduction and current in the output inductor L_{p2} starts decreasing to zero. In the last mode of operation the output inductor current remains zero in next input switching cycle.

2) **Isolated DC to DC half bridge converter:**

In the DC to DC converter one half cycle is same as other half cycle so two switches are turned ON and OFF.
regularly for one switching cycle. For one half cycle the upper switch s1 is ON. The upper diodes ON secondary side $D_{o1}, D_{o3}, D_{o5}$ starts conduction. The inductors I all secondary winding start storing energy. When the highest value of current reaches to inductor its will the turn OFF by switch S1. For maintain the constant output voltage all the filter capacitor discharges through loads. For the second half cycle of PWM period the lower switch is ON the upper switch is OFF. The secondary diodes $D_{o2}, D_{o4}, D_{o6}, D_{o8}$ are turned ON to free wheel the inductor capacity. The net voltage across HFT becomes zero because of secondary winding current is cancel to core flux

III PLAN OF PROPOSED BRIDGELESS CONVERTER BASED SMPS SYSTEM

The format of proposed bridgeless converter based totally completely SMPS is portrayed within the accompanying diploma.

A. Plan of Proposed SMPS System

The layout for the excellent half cycle worked PFC converter is finished best here. The terrible half of cycle toiled converter is imprinted likewise. The widespread voltage $V_{acav}$ is figured as,

$$V_{acav} = \frac{V_{ac}2\sqrt{2}}{\pi} = \frac{2\sqrt{2} \times 220V}{3.14} = 198V$$

The commitment cycle (D) of the PFC expense embellish converter is bestowed in light of the fact that the degree of its yield dc voltage to the entire of yield dc voltage and information voltage.

$$D = \frac{V_{PFC}}{V_{PFC} + V_{acav}} = \frac{300V}{300V + 198V} = 0.6$$

Not with standing accumulation in the insights voltage from 170v to 270v, the yield voltage is prepared aside standard at 300v. Thusly, the commitment cycles for supply voltages of 170v, 220v and 270v are figured as, $D_{170v}=0.66$, $D_{220v}=0.552$. As a broadened path as issues. The gigantic of will cycle D of the PFC converter is taken obviously tons significantly under $D_{220v}$ for unpracticed manipulate during DCM assignment. Accordingly, it’s far pondered as O.25 for the commercial business Enterprise of the PFC converter.

The certainties inductor price is registered for the same vintage swell of 40% of facts draining trouble.

$$L_{p1} = \frac{D \times V_{acav}}{f \times (i_{in\_ripple})} = \frac{0.25 \times 1.98V}{20kHz \times 0.58A} = 4.35mH$$

Where, f is the changing over repeat of the PFC converter. The squeezing conduction parameter is given as,

$$K_a < \frac{1}{2\left(\frac{V_{PFC} + n}{V_{ac}}\right)^2} = \frac{1}{2\left(\frac{300V}{311V}\right)^2} = 0.129$$

Where, n is taken as 1 for the non-separated PFC converter. To innovative creations the PFC converter in DCM, the conduction parameter need to be taken widely a whole parcel significantly not as much as $K_a$ for capable control. Therefore, it’s far settled on as 0.08

$$L_{eq} = \frac{\pi \times 291.2 \times 0.08}{2 \times 20kHz} = 225\mu H$$

The comparable estimation of inductance of the PFC converter is given as,

$$L_{p2} = \frac{L_{p1} L_{eq}}{L_{p1} - L_{eq}} = \frac{4.31mH \times 225\mu H}{4.31mH - 225\mu H} = 237\mu H$$

The determined on price of yield inductor is one hundred $\mu H$ to assure DCM state of affairs in all strolling times of statistics voltages, load and institution spirit PF hobby at a low enter voltage.

The middle of the road capacitor charge is foreseen as

$$C_p = \frac{1}{\pi \times \left(W_p L_{p1} + L_{p2}\right) \times 0.08}$$

$$= \frac{1}{2 \times \pi \times \left(93300\mu H\times (4.3mH + 0.1mH)\right)} = 0.18\mu F$$

Wherein, $w_p$ is the recurrence ($w_p = 2\pi f$). And $F_p$ is taken into consideration as 2000Hz ($F_p > F_t$). A capacitor cost of 0.22$\mu F$ is determined for the hardware execution. An L-C get out is attached on the input viewpoint to mitigate better call for sounds. The finest fee of the capacitor is as,

$$C_{ac} = \frac{L_{p1} \times \pi \times 0.08}{2 \times 314 \times 311V} = 391nF$$

The channel capacitor charge is picked to such a sum, to the point that it’s far parcels eminently a mess not as much as $C_{ac}$. Along these lines, a 330$nF$ capacitor is picked in apparatus execution.

The channel inductor $L_{ac}$ is figured for directing over the top demand sounds near five kHz repeat.

$$L_{ac} = \frac{1}{\pi^2 \times f^2 \times C_{ac}} = \frac{1}{4 \times (3.14 \times 5 \times 10^3)^2 \times 330 \times 10^{-12}} = 3.07mH$$

A 3.1$mH$ inductor is decided for re-enactment and exploratory gadget.

The facts capacitors of the removed 1/2 of interface dc-dc converter pass approximately due to the fact the yield Get out capacitors for the PFC converter. Along those follows, the arrangement of the capacitor is essential to dispose of the second one request symphonies feature notwithstanding give most extreme over the top quality to that range while enter voltage falls. This is greatest plausible legitimate for PC more one of a kind substances in disposition of Truth the
rating of the capacitor influences the estimations and the rate of the general SMPS.

The light to determine the capacitor to lessen $2^{nd}$ engineer symphonious is as,

$$\frac{c_1}{2} = \frac{c_2}{2} = \frac{i_{pf}c}{2w\Delta v_{pf}c}$$

$$\frac{1.06}{2 \times 314 \times 6} = 0.28mH \quad (10)$$

The preserve-up ability might be surveyed as

$$t_{hold\text{-}up} = \frac{(V_{PFcm}^2 - V_{PFcmin}^2)}{2P_0} \quad (11)$$

Where, $t_{hold\text{-}up}$ is the theft time of the capacitor, $P_0$ is the maximum yield control, $VPFCm$ is the lowest yield voltage ($2\%$ swell is considered) and $VPFCmin$ is the beside the point voltage at which the yield voltage holds course.

Fittingly, to preserve up 10ms preserve up time, the required capacitance is selected as,

$$C = \frac{2t_{hold\text{-}up}P_0}{(V_{PFcm}^2 - V_{PFcmin}^2)} = \frac{2 \times 10ms \times 320W}{(294V)^2 - (260V)^2} = 0.339mF \quad (12)$$

Two capacitors are related in amusement activity plan. Along those follows, the price of $c_1 = c_2 = 0.679 \text{ mF}$. The settled on charge of the capacitors is 0.6mF every to meet each the times. The rely of inductance for the optional bending with most stunning score is avowed transforming into ideal here, on the equivalent time on the grounds that the estimation for rest of the aide windings stays square with. The inductance $L_{01}$ is passed on as,

$$L_{01} = \frac{12\nu(0.5 - 0.4)}{60kHz \times 0.625} = 0.032mH \quad (13)$$

Basically, the inductances for the opposite discretionary windings are figured as 9.5μH, 6.8 μH and 1.5 mH.

### IV FRACTIONAL ORDER PID CONTROLLER

A proportional-integral-derivative or PID controller is a kind of feedback control loop mechanism that is widely used in industrial control systems. The PID controller has a good stability, therefore it can be applied to improve the performance of many control systems. In addition, it is easy implementing and has low cost. There are several attempts to enhance the classical PID controller; one of these attempts is the Fractional Order PID controller or (FOPID). The FOPID controller has five parameters instead of the three as in the classical PID controller. The additional two parameters represent the fractional orders of derivative and integral which give this modified controller More flexibility. By using the fractional order PID controller percentage of over shoot decreases, settling time decreases and integral of square error and obolute of square are within permissible limit raising the transient time decreases.

The Transfer function of Integer PID controller is given by:

$$G_c(s) = k_p + k_i s^{-1} + k_d s \quad (14)$$

![Fig.4 Block diagram of Fractional order PID Controller](image)

The transfer function of FOPID controller in continuous mode is given by:

$$G_c(s) = k_p + T_i s^{-\lambda} + T_d s^{-\mu},(\lambda,\mu > 0) \quad (15)$$

A point to plane analysis of FOPID controller is shown in the fig.(6). The extension in PID give more flexibility for designing the controllers and gives the accurate results.

![Fig.5 Point to plane analysis of FOPID](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PI</th>
<th>FOPID</th>
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<tbody>
<tr>
<td>$K_p$</td>
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<td>0.0001</td>
</tr>
<tr>
<td>$K_d$</td>
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<tr>
<td>$K_i$</td>
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### V RESULTS

In the results, the conventional PI controller and the proposed FOPID controller are compared with full load and
load changing condition. The FOPID controller is adapted at voltage controller. With this FOPID Controller, the test results of THD is reduced and compared with PI controller.

The Input current is shown in fig.6. The harmonic order for PI and FOPID controller for full load condition are shown in fig.7 and fig.8. The harmonic order for PI and FOPID controller for load changing condition are shown in fig.9 and fig.10. The comparison of PI and FOPID are presented in table.2

VI CONCLUSION

A Bridgeless non isolated SEPIC based FOPID voltage controller has been proposed here to reduce the total harmonic distortion compared with conventional SEPIC based PI voltage controller. voltage regulation and efficiency are improved with this power quality improvement is occurred and operating satisfactorily wide variation of input voltage and load.

REFERENCES


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