Fuzzy logic based transformer-less inverter with PV Negative Terminal and Grid Neutral point

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Abstract:

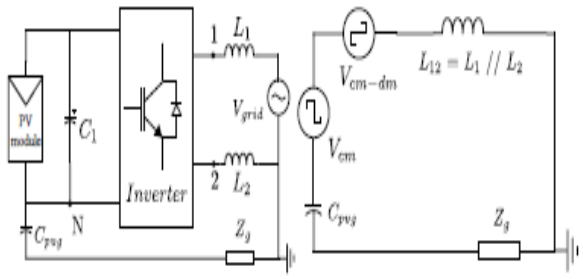
For the sheltered activity of transformer a mess significantly less network associated PV inverters, the issue of normal mode (CM) spillage bleeding edge wishes to be tended to warily. In this paper, a solitary staggered transformer parts substantially less inverter topology is proposed which unmistakably disposes of CM spillage contemporary through interfacing lattice autonomous factor promptly to the PV terrible terminal, consequently bypassing the PV stray capacitance. It gives a low-value arrangement which incorporates just four quality switches, capacitors and an unmarried get out inductor. When contrasted with 1/2 connect topologies, with this inverter no less than 27% and most extreme of a hundred% more yield voltage is gotten for the equivalent DC interface voltage. The proposed inverter is broke down in component and its changing example to produce staggered yield even as keeping the capacitor voltage is alluded to. Recreations and examinations results certify the achievability and proper generally speaking execution of the proposed inverter.

Index Terms —Multilevel inverter, transformer less inverter, common mode current, photovoltaic (PV) system.

I. INTRODUCTION

In an era where there is growing concern over climate change, higher oil prices and sustainability of energy from nonrenewable sources, many countries globally are adopting new regulations to promote clean and renewable energy. This has led to a first-rate boom of hobby in photovoltaic (PV) power systems. There has been amazing drop in the rate of PV modules in the remaining decade, consequently the reduction of manufacturing costs of PV inverters turns into a need. PV inverters that lease an isolation transformer, are bulky and tough to put in. Although thru employing a excessive frequency transformer along a DC-DC converter can lessen the scale of the inverter, it reduces the overall overall performance due to the leakage in the immoderate frequency transformer. As the call indicates, the transformer less inverters are without the cumbersome isolation transformer which now not only makes them compact however additionally makes them cheaper and especially green. Therefore, the popularity of transformer less PV inverters is growing each day. However, as there may be no galvanic isolation between the PV panel and the grid,

it is able to bring about the waft of commonplace mode leakage currents through the PV panel parasitic capacitance [1], [2]. This can compromise the safety of the consumer operating the inverter. In [3], it is mentioned that this leakage capacitance value depends on various factors; such as surface of cells, module frame, distance between cells, PV panel and frame structure, humidity and dust covering the PV panel and weather conditions. Typical values of this parasitic capacitance lies between 10-150 nF [2], [4].



(a) transformer less inverter (b) common mode circuit

Fig. 1: Common mode equivalent circuit of a generalized transformer less inverter [4] The magnitude of these leakage currents between the panel terminals and ground depends mostly on the value of thisStray capacitance and the amplitude And frequency Content material of the not unusual-mode voltage variations which are present at the PV panel terminals [4]. Common mode equal circuit of a generalized transformer less Inverter is shownin Fig. 1. Where Vcm and Vcm-dm is given by (1) and (2) respectively.

$$V_{cm} = {V_{1N} + V_{2N}}/{2} \quad (1)$$

$$V_{cm-dm} = (V_{1N} - V_{2N}) {L_2 - L_1}/{2(L_2 + L_1)} \quad (2)$$

Based on this circuit it is evident that there exists two rules to eliminate leakage current [6].

- Symmetrical inverter topologies with zero Vcm-dm and constant Vcm. (invalid for half -bridge topologies)
- Matching circuit parameters to ensure sum of Vcm and Vcm-dm is zero (invalid for full -bridge topologies)

Therefore, from (1) and (2) it is Glaring that, the 1/2-bridge family of inverters with , 3 or greater output voltage stages are without fluctuating CM voltage. These consist of the NPC inverter [3], ANPC inverter [7], [8], Co-power NPC

inverter [9] etc. Their number one drawback is the want of excessive input Voltages, which calls for both a preceding growth dc-dc level or a big PV string. On the other hand the entire-bridge topology calls for half of of the input voltage demanded by using the 1/2-bridge topology. However, the entire bridge need to be modulated with bipolar SPWM to keep away from a varying common-mode voltage.As compared to the bipolar SPWM, the unipolar SPWM reveals advanced performance in terms of the output modern-day ripple, switching losses, smaller filter out size and no internal reactive energy. Despite of such advantages, it can't be without delay Employed in complete bridge transformer less PV inverters for the purpose that common mode voltage oscillates at switching frequency which in the long run ends in high ground leakage streams. To hinder the CM advanced way at some point or another of the freewheeling length, more switches are embedded into the entire extension inverter both at the DC or AC side. In this way, the ones finish connect inverters can be moreover sorted as DC decoupling based absolutely inverters and AC decoupling principally based inverters as

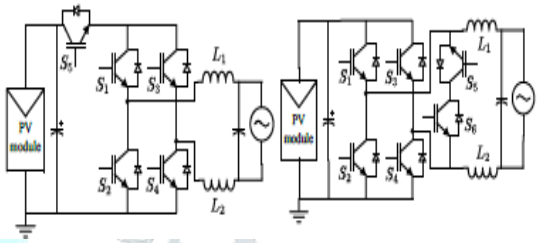
Characterized in [10]. Nonetheless, in those topologies decoupling is fragmented due to the variable intersection capacitance of the quality changes primary to the stream of CM ebbs and flows [6]. To also diminish CM streams, a few topologies cinch the not surprising mode voltage to half of the DC hyperlink voltage at some phase in freewheeling length [11], [12]. In spite of the fact that the dynamic clasping based absolutely completely topologies can effectively decrease CM streams, they require DC connect capacitors and a couple of more noteworthy switches for bracing reason, in this manner building up the aggregate charge of the inverter. Another technique contracted to evacuate CM contemporary is to immediately associate PV horrendous terminal and the network free point [13], [14]. In the ones topologies the horrible yield voltage is created by methods for the virtual DC transport, wherein the vitality is exchanged from the genuine transport to the computerized one. These topologies can create 3-level yield voltage while adjusted with unipolar SPWM. Toin addition reduce the filter length and to accumulate immoderate power transfer abilities, multilevel inverters may be hired. A determined on few present topologies utilizing DC/AC decoupling, clipping and ground association are tried in Fig. 2. This paper proposes a novel staggered transformer less portion of scaffold topology which hire ground connection among PV bad terminal and grid unbiased element, thereby completely casting off CM leakage contemporary. In spite of the fact that being a half scaffold basically based topology, the proposed inverter is destitute from the need of inordinate info voltages. In this way, the gifts of the fullbridge and half of-connect based absolutely arrangements are mixed by and large.

The proposed inverter additionally can offer responsive power help to the matrix showing up as a network component controller [15].

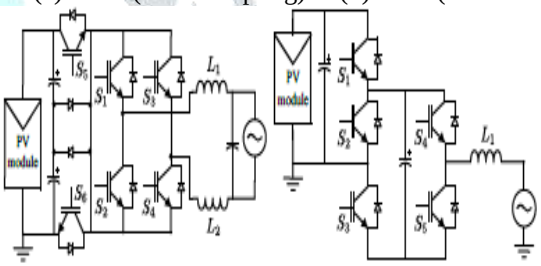
In this paper, the proposed staggered topology is dissected and its different methods of task are characterized in detail for 3 organize activity. Reenactment results for these modes are given, which delineates its most extreme vitality factor (MPP) observing generally speaking execution and Low voltage encounter through (LVRT) usefulness. The module capacitor estimate is anticipated and control technique to save its coveted voltage for the term of these modes is portrayed. The changing example to procure 5 level yield voltage is provided and the inverter activity is learned with the guide of a reproduction working out. A short balance is made with the current transformer less inverter topologies which features its capability to adapt to their inadequacies identified with various key inconveniences. At long last, the inverter task is tentatively affirmed which substantiate the reenactment outcomes consequently Confirming the possibility and exact execution of the proposedinverter.

II. PROPOSED TOPOLOGY

We have mentioned numerous transformer less inverter topologies which deal with the problem of leakage present day. It can be seen that, to restoration this trouble the inverter topologies need to



(a) H5 (Dc decoupling) (b)Heric (Ac decoupling)



(b) FB-DCBP Inverter (CLAMPED) (d)Virtual DC based

Either segregate the PV board from the network amid freewheeling period or brace The respect midpoint of the DC delivering or make utilization of ground relationship with direct interface the PV terrible terminal to the framework unprejudiced point. One of the topology that make utilization of floor association in perspective of the idea of virtual DC conveyance is proposed in [14]. Here the PV poor terminal andthe matrix nonpartisan are specifically associated in this manner dispensing with the spillage current issue. Be that as it may, to value the virtual DC conveyance, two capacitors with unequal voltages are related in parallel. Gigantic deviation in the capacitor voltages can provoke high switch streams. Along these lines, this inverter topology Is conflictingfor excessive strength frameworks. Likewise, this inverter topology can't give staggered yield voltage. Subsequently, Any other staggered transformer less inverter topology in light of the Idea of digital DC transport is proposed on this paper.

A. A 3-level transformer less inverter topology

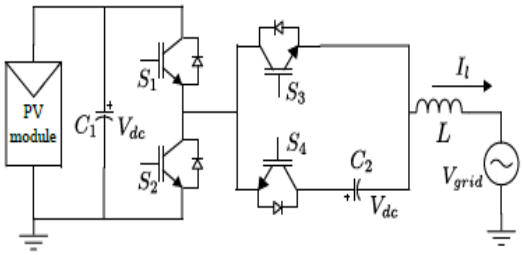


Fig: Proposed inverter topology

A essential three level shape of proposed inverter topology is regarded in Fig. Three. The proposed inverter topology is a H4 topology comprising of half extensions with switches S1, S2 and capacitor C1 shaping one half scaffold and switches S3, S4 and capacitor C2 framing the alternative half extension. The Parasitic capacitance of the PV board is straightforwardly skirted with the aid of utilizing floor affiliation among PV negative terminal and lattice unbiased point. This can be checked by looking at the proposed inverter with the summed up transformer less inverter appeared in Fig. 1. In the proposed topology, V2N = 0 & L2 = 0.

$$V_{cm} = {}^{V_{1N}}/_{2} \,\&\, V_{cm-dm} = -{}^{V_{1N}}/_{2} \quad (3)$$

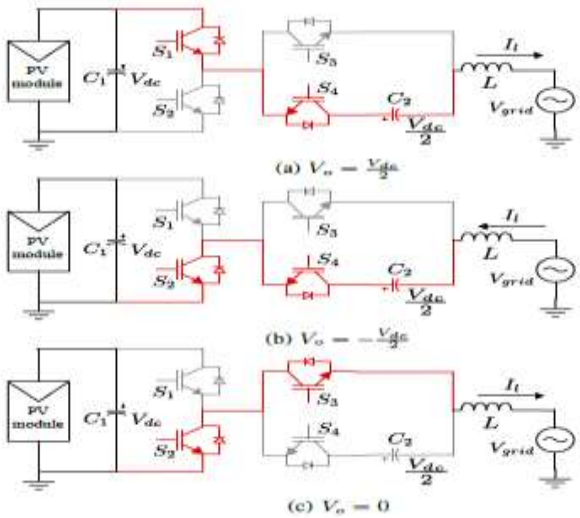


Fig. 4: Inverter switching states in Mode 1

From the above equation it is evident that, the sum of Vcm and Vcm-dm is zero. Therefore, leakage current in the proposed topology is always equal to zero.The proposed 3-level transformer less inverter is first of its kind which disposes of the CM spillage current with under five power switches. This inverter topology can be operated in two modes.In Mode 1 the capacitor C2 is charged to Vdc=2 and in Mode 2 the capacitor C2 is charged to Vdc. These modes of operation are described in the following section.

B. Mode 1

In Mode 1 the proposed topology can give 3 level voltage output consisting of Vdc2 , 0, - Vdc 2. at the point when switch S1 and S4 are ON, the yield voltage is Vdc 2 . at the point when switch S2 and S4 are ON, the yield voltage is – Vdc 2 and when switch S2 and S3 are ON, the yield voltage is 0.The inverter switching states for Mode 1 are shown in Fig. 4. The capacitor C2 is naturally balanced as the inverter supplies sinusoidal current to the grid. The most extreme yield voltage is equivalent to the voltage crosswise over capacitor C2 which is Vdc2 . In this way the DC connect voltage is double the voltage crosswise over C2. The inverter is reproduced with DC connect voltage of 800V.The simulation result for output voltage Vo, capacitor voltage Vc, and Grid current IL is shown in Fig. 5.

C. Mode 2

When the inverter operates in Mode 1, its operation is similar to any half bridge based inverter like the NPC inverter. An inherent issue associated with half bridge topologies is the requirement of higher DC link voltage. This increases

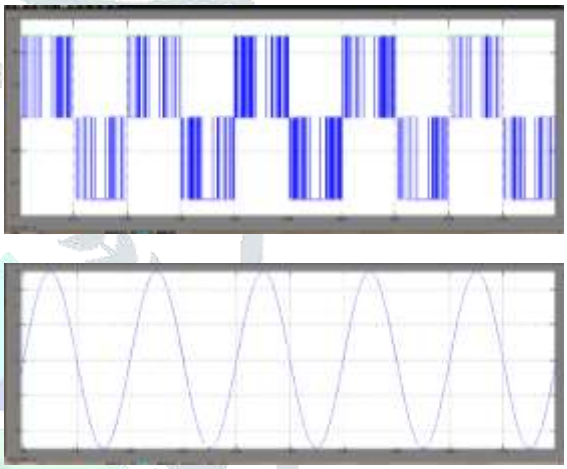


Fig. 5: Simulation results of the 3-level inverter in Mode 1

The voltage rating of the switches and in the long run the overall inverter price. In Mode 2 the voltage throughout capacitor C2 is stored identical because the DC hyperlink voltage Vdc. Consequently, the voltage rating of the switches in Mode 2 is half of that in Mode 1.The yield voltages acquired when the inverter is worked in Mode 2 are Vdc, 0, -Vdc. The inverter switching states for Mode 2 are Shown in Fig. 8.

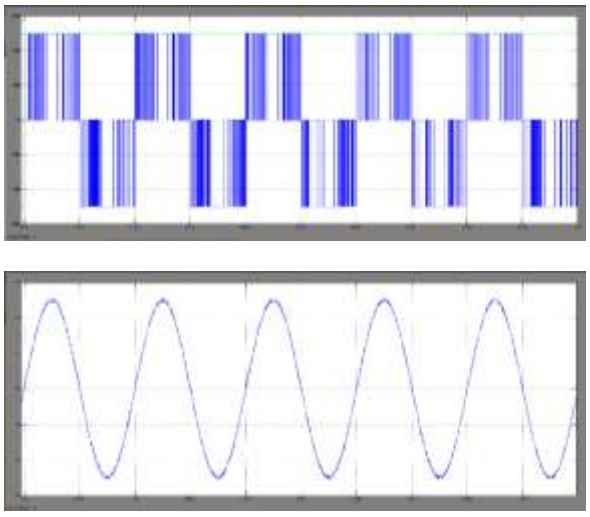


Fig. 6: Simulation results of the 3-level inverter in Mode 2

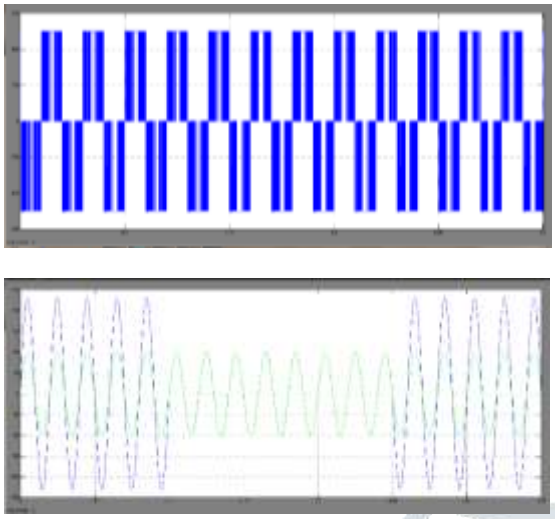


Fig. 7: LVRT capability of the proposed inverter

As opposed to Mode 1, when the inverter is operating inMode 2, the capacitor C2 is not naturally balanced. However, it can be seen from Table I that there are redundancy states when
The inverter output is zero. Therefore, to balance the capacitor, it can be charged or discharged or bypassed during one of these zero states. For example, let's consider the inverter to

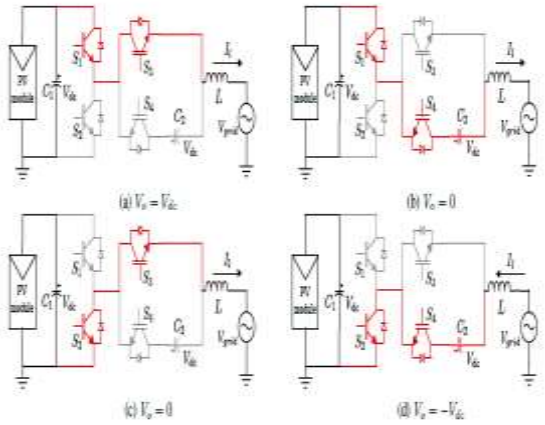


Fig. 8: Inverter switching states in Mode 2

be operating at unity power factor (UPF), then C2 is chargedduring zero state of the positive half current cycle by turning on S1 and S4 as shown in Fig. 8b . During the -Vdc state, C2 discharges as the current is negative. Therefore, to maintain the net charge C2 is bypassed during zero state of the negative half current cycle by turning on S2 and S3. This asymmetric operation of the inverter limits the maximum achievable modulation index, which is derived in the following section. The inverter is simulated in PSCAD 4.5.2 and the results for output voltage and current is shown in Fig. 6. Incremental conductance algorithm is used to track the maximum power
point (MPP). To exhibit MPP following abilities of the proposed inverter, sun based irradiance was fluctuated from 1000 W=m2 to 800 W=m2 and after that to 1200 W=m2. It very well may be found in Fig. 9, that the PV voltage (Vpv) takes after the MPP reference voltage (Vmppref). Another imperative component of the proposed inverter is the capacity to infuse responsive power into the framework, therebymaking it LVRT capable. To verify this, the grid rms voltage is suddenly changed from 230V to 100V. During this period, the inverterinjects reactive power into the grid with constant currentamplitude as seen in Fig. 7.High and zero states respectively over one carrier cycle. Let m,Ip, _ be modulation index, load current amplitude and phase angle respectively.

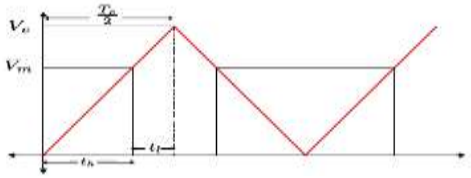


Fig. 10: Pulse width modulation

From Fig. 10. the time durations the and tl are calculated as:

$$2t_h = {}^{V_m}/_{V_c}\, T_c = [m \sin\theta] T_c (4)$$

$$2t_l = \left(1 - {}^{V_m}/_{V_C}\right) = (1 - m \sin\theta) T_c \quad (5)$$

Therefore Qc and Qd can be calculated as:

$$Q_c = \int_{\phi}^{\pi} I_p(1 - m\sin\theta)\sin(\theta-\phi)d\theta + \int_{\pi}^{\pi+\phi} I_p \sin(\theta-\phi)d\theta$$

$$\therefore Q_c = 2 - \frac{m}{2}[\sin\phi + \pi\cos\phi - \phi\cos\phi] \quad (6)$$

$$Q_d = \int_{\pi+\phi}^{2\pi} m I_p \sin\theta \sin(\theta-\phi)\, d\theta$$

$$\therefore Q_d = \frac{m}{2}[\sin\phi + \pi\cos\phi - \phi\cos\phi] \quad (7)$$

To ensure that the voltage across capacitor C2 is Vdc,

$$Q_c \geqslant Q_d$$

$$\therefore 2 \geqslant m[\sin\phi + (\pi - \phi)\cos\phi]$$

$$\therefore m \leqslant \frac{2}{\sin\phi + (\pi - \phi)\cos\phi} \quad (8)$$

From (8) it is evident that the inverter modulation index is afunction of inverter power factor. A graph of modulation index versus phase is shown in Fig. 11.

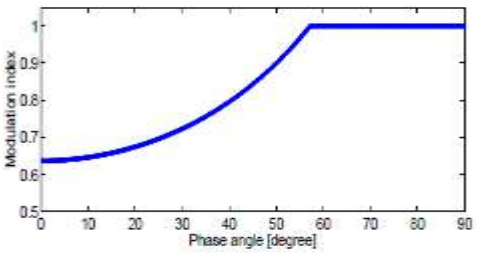


Fig. 11: Modulation index vs phase

When the inverter is operating at UPF the maximum modulationindex that can be achieved in mode 2 is 2 _ (_ 0:637) whereas as in Mode 1 it is only 0.5. The modulation index of 1 can be achieved when the inverter is operating at non UPF. Thus in Mode 2, a minimum 27% and maximum

100% more output voltage is obtained as compared to Mode 1 and in other half bridge topologies like NPC inverter. From (8) it is clear that the maximum modulation index can range for 0.637 for UPF operation to 1 at a power factor of 0.5 lag/lead.

E. Control strategy

The inverter is operated in current control mode. The block diagram of control strategy is shown in Fig. 12. The reference current Iref is obtained via MPPT. Incremental conductancealgorithm is used for MPPT calculation. Proportional Resonant(PR) control is used to control the grid current [16]. Transfer function of PR control is given in (9)

$$G_{c(S)} = K_P + K_I \frac{S}{S^2 + W^2} \qquad (9)$$

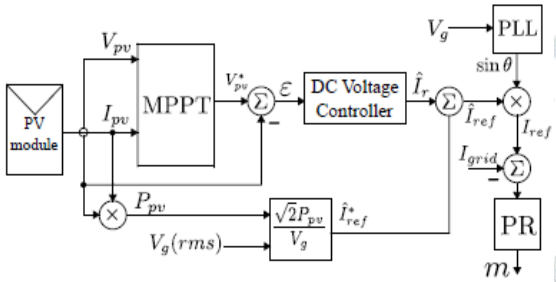


Fig. 12: Current control for proposed inverter

The output of PR controller is the modulation index 'm' andit acts as an input to sine triangle PWM block. In Mode 1, the control is straightforward due to the natural balancing of the
capacitor voltage. Therefore, the gate pulses of the switches can be obtained directly from SPWM as shown in Fig. 13a. However, to maintain the capacitor voltage in Mode 2, the estimated output voltage level is checked via SPWM and the control flow as described in Fig. 13b is followed to obtain the gate pulses of the switches. The recharging of capacitor C2

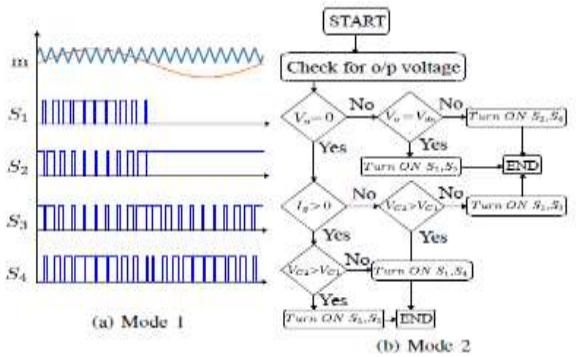
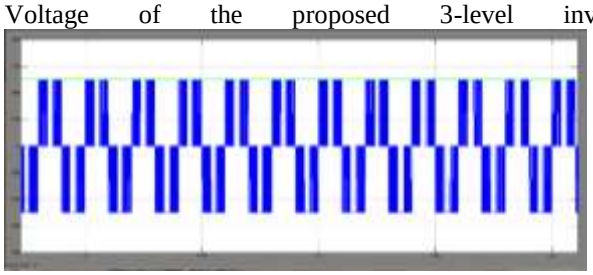


Fig. 13: Control procedure to keep up the capacitor Voltage of the proposed 3-level inverter.



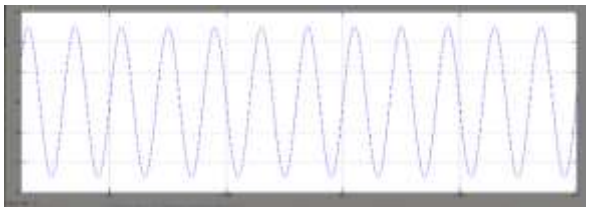


Fig. 14: Precharging of the module capacitor C2

CM spillage current with under seven power switches. Is appeared in Fig. 14. The capacitor C2 is pre-charged to. Halfthe rated voltage and it is further charged to Vdcby applying control strategy as described in Fig. 13b.

F. 5-level transformer less inverter topology

The proposed topology is modular, consequently with the aid of adding any other half-bridge module to the proposed 3-level topology, a 5 stage transformer less inverter topology is gotten, which is seemed in Fig. 15. The proposed five-stage topology is first of its type staggered inverter which wipes out the CM spillage modern-day with below seven electricity switches.Switching states of the inverter are shown in Table II. When the inverter output is Vdc the module capacitors are bypassed. As the current fed

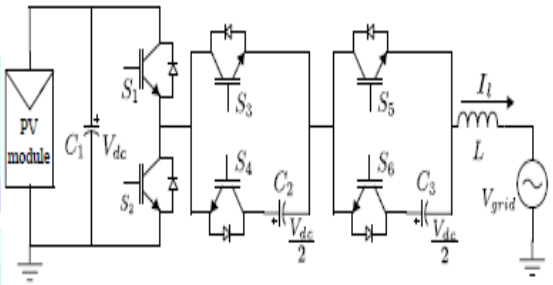


Fig. 15: 5-level transformer less inverter topology

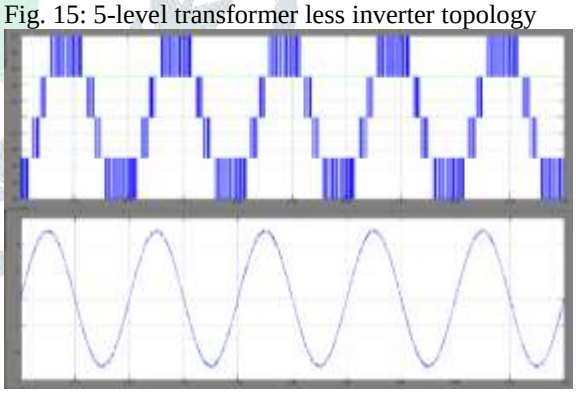


Fig. 16: Simulation results of the 5-level inverter in Mode 2

to the grid is symmetric, the charged gained by the modulecapacitors during inverter state of Vdc2 is lost during □Vdc2 stateand vice-versa. However, when the output is □Vdc, the charging or discharging of the capacitors depends upon the grid current. Therefore to maintain the module capacitor voltage to Vdc2 , it can be charged or discharged or bypassed accordingly
during one of the zero states. This control procedure is like the proposed 3-level topology, henceforth the condition determined in (8) remains constant notwithstanding for the proposed 5-level topology.

To verify the inverter operation it is simulated in Mode 2and simulation results are appeared in Fig. 16. It very well may be seen that the voltage over the module capacitor is half of the DC connect voltage, subsequently additionally decreasing the voltage rating of the switches. The proposed inverter can be stretched out to give nlevel yield by including fittingno of half bridge modules.

III. ESTIMATION OF THE MODULE CAPACITANCE

A grid connected PV inverter is supposed to operate atUPF. Keeping in mind the end goal to accomplish unit control factor, the yield voltage and current ought to have a similar stage. Accordingly, the yield controlis communicated as in (10).

$$P_{out(t)} = \sqrt{2}V_{g.}\sin(\omega t)\sqrt{2}.\frac{P_{pv}}{V_g}.\sin(\omega t) \qquad (10)$$

Where Pout(t) is the momentary power; Ppv is the dc control from the info PV boards; Vg is the rms matrix voltage. In this way, the yield control is streamlined as in (11)

$$P_{out}(t) = 2P_{pv}sin^2(\omega t) = P_{pv}(1-\cos(2\omega t)) \quad (11)$$

As the vitality put away in the capacitor is the essential of the yield control more than one half cycle, the voltage swell commitment of the twofold recurrence part of the yield control is zero.Therefore, the energy stored in the capacitor is calculated as given below:

$$\int P_{out}\,(t)\,dt = \frac{1}{2}C(u_{maz} - u_{min}) = Cu\delta u \qquad (12)$$

Thus, the capacitance is obtained as given below:

$$C = \frac{\pi P_{pv}}{\omega u \delta u} = \frac{P_{pv}}{2fu\delta u} \qquad (13)$$

Where u is the nominal capacitor voltage and _u is the allowed ripple. From 13, it is obvious the capacitance prerequisite of the proposed inverter is bigger than that of customary transformer less inverters, for example, H5, Heric, and FB-DCBP, and so forth. Be that as it may, the capacitor estimate is practically identical to half scaffold based inverters preferred NPC inverter. In NPC inverter, amid the advantageous half of cycle the excellent capacitor elements potential to the matrix and the base capacitor resources capability to the lattice inside the poor 1/2 cycle. Likewise, in our proposed topology throughout the poor 1/2 cycle, the capacitor C2 elements power to the grid and vice versa.Another factor that needs to be considered is while sizing the module capacitor is its rms current rating. However, as compared to half bridge based inverters the proposed inverter exhibits better DC link utilization as the
input voltage requirement for the proposed inverter in Mode II is in the range of Vdc to 1.57Vdc as opposed to NPC inverter which needs a DC link voltage of 2Vdc. The main advantage
of the proposed converter is that it completely eliminates common mode leakage currents. Such elimination of common mode current is possible only with half bridge inverters like the NPC inverter, while the other standard full transformer less converter topologies like, H5, Heric, and FB-DCBP, etc., are not able to completely eliminate the leakage current and can
only limit it to certain extent.

IV. LOSSES AND EFFICIENCY ASSESSMENT

USP of transformer less grid connected PV inverters is its high efficiency and low cost. Several transformer less inverters have been proposed in literature with their efficiencies ranging from 95% to 99%. However, the circuit parameters and thesemiconductor devices used to measure the efficiency of these inverters vary from one inverter to another. For example, a topology employing SiC devices or Highly efficient CoolMOSwould present an efficiency improvement of over 1% but at a higher cost of the inverter. In this way, to have a reasonable and precise productivity correlation of the proposed inverter with the regular transformerlessinverters,it is necessary to evaluate their losses and efficiency for the same circuit parameters and devices. Also efficiencies at different load conditions needs to be evaluated so as to calculate and compare weighted efficiency of these topologies. The total loss is the summation of semiconductor conduction loss, device switching loss, ESR loss in the DC link capacitors, Inductor copper and core loss and other constant snubber and stray losses. In order to calculate device conduction loss, the first order voltage drop models of the devices is used.

$$IGBT: V_{ce} = V_t + i(t).R_{ce} \qquad (14)$$

$$Diode: V_{ak} = V_f + i(t).R_d \qquad (15)$$

whereVce is the IGBT collector emitter voltage drop, Vt is the IGBT identical voltage drop at no heap, Rce is the IGBT on opposition, Vak is the diode anode cathode voltage drop, Vf is the diode comparable voltage drop at no heap, and Rd is diode on obstruction; i(t) is the heap current and expressed as

$$i(t) = I_L.\sin(\omega t) \qquad (16)$$

where IL is the amplitude of the load current. The duty ratiosfor active and zero stage is given by (17) and (18) respectively. where, m is the inverter modulation index and ! is the grid
frequency.

$$Da(t) = m.sin(\omega t) \qquad (17)$$

$$Dz(t) = 1 - m.sin(\omega t) \qquad (18)$$

$$P_{loss} = \frac{1}{2\pi}\int_0^{\pi} v(t)i(t)D(t)\;\; d\omega t \qquad (19)$$

Substituting (14), (15), (16), (17) and (18) in (19), we get,active stage and zero stage conduction loss for IGBT and diode is as given below

$$P_{active_{IGBT}} = \frac{I_L V_t}{2} + \frac{2mI_L^2 R_{ce}}{3\pi} \quad (20)$$

$$P_{active_{diode}} = \frac{I_L V_f}{2} + \frac{2mI_L^2 R_d}{3\pi} \quad (21)$$

$$P_{zero_{IGBT}} = \frac{I_L V_t}{\pi} - \frac{I_L V_t m}{2} + \frac{I_L^2 R_{ce}}{4} - \frac{2mI_L^2 R_{ce}}{3\pi} \quad (22)$$

$$P_{zero_{diode}} = \frac{I_L V_f}{\pi} - \frac{I_L V_f m}{2} + \frac{I_L^2 R_d}{4} - \frac{2mI_L^2 R_d}{3\pi} \quad (23)$$

Therefore, total conduction loss for the proposed inverter isgiven by (24)

$$P_{cond} = \frac{4I_L V_t}{\pi} + mI_L^2 R_{ce} \quad (24)$$

Switching loss for IGBT is given by (25), where Eon andEoff is the energy lost during turn on and turn off transitions, fsw is the switching frequency and Vswis the voltage across the switch.

$$P_{sw} \propto f_{sw} V_{sw} (E_{on} + Eoff) \quad (25)$$

ESR loss of the capacitor is given by (26).

$$ESR_{loss} = \frac{1}{T} \int_0^T i(t)^2 Da(t)\ ESR\ dt \quad (26)$$

For loss calculation IGBT characteristics of IKW20N60H3operating at 15 kHZ is considered. Fig. 17 shows the efficiency curves as acapacity of yield intensity of the proposed inverter

When contrasted with normal transformer much less PV inverter topologies.

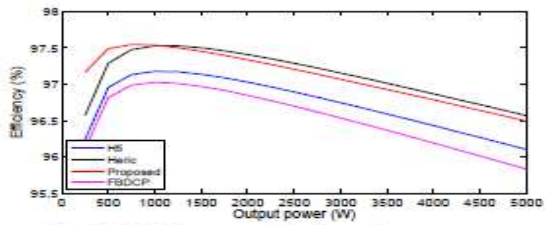


Fig. 17: Efficiency as a function of output power

From Fig. 17, it can be seen that the efficiency of the proposed inverter is better than that of H5 inverter and FBDCBP inverter, this is because of the fact that,in the proposed inverter only two switches conduct at a time as opposed to 3 and 4 switches in H5 and FB-DCBP inverter respectively. Due to the presence of series capacitor, the proposed inverter has a larger ESR loss as compared to these inverters. However, the proposed inverter has a better overall efficiency as it has only four switches, of which, only two switches conduct at a time, thereby reducing the total switch conduction loss. The Heric inverter consists of two symmetrical inductors, which

results in higher constant losses. Therefore, at low power, the proposed inverter has better efficiency than that of Hericinverter. However, at rated power, Heric inverter has better

efficiency as it has lower switching loss as compared to the proposed inverter. The weighted CEC efficiency of proposed and Heric inverter is 97.04% and 97.1% respectively.

V. COMPARATIVE ANALYSIS

As explained previously, the problem of leakage contemporary can be tackled both via separating the PV panel from the grid or clamping it to midpoint of the DC bus or by employing ground connection between the PV panel and grid neutral. Although half bridge based topologies like the NPC inverter, Flyingcapacitor (FC) inverter etcrequire higher DC link voltage, theoretically they have topological advantage of no inherent leakage current over the full bridge based inverters. However,a slight unbalance of DC link split capacitor voltages canlead to leakage current with significant DC injection into the grid [17]. Therefore, equalizing of DC link split capacitor voltages is of utmost importance. This can be achieved by using addition power electronic circuitry [18], which adds to the inverter cost. In case of decoupling based topologies extra switches are needed to isolate the PV panel from the grid during the freewheeling period. This can cause higher conduction loss as in the case of H5 inverter. Although the PV panel is decoupled from the grid, even then, there Is a few leakage present day due to the non idealities of the electricity switches. To similarly reduce the leakage present day some topologies like the one in [12] have been proposed which rent energetic clamping at some stage in the freewheeling duration. Here, as the not unusual mode voltage is constantly clamped to 1/2 of the DC hyperlink voltage, there is no switching frequency leakage cutting-edge. However, the common mode voltage consists of grid frequency component

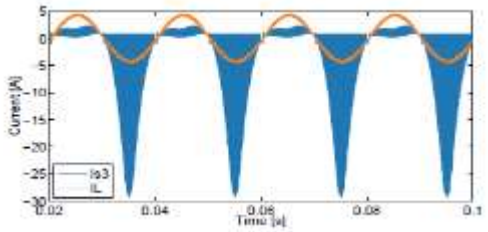


Fig. 18: Current stress on switch S3 in virtual-DC based inverter [19]

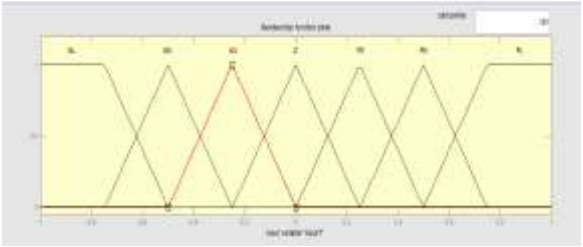
superimposed on the clamped DC voltage. Thus the leakagecurrent is not completely eliminated and it depends upon the filter inductance, load current and the grid voltage. Even in these topologies, the split capacitor voltages are to be maintained constant. A drift in the DC link midpoint voltage can cause the unbalanced capacitor voltages to exceed their individual voltage rating, thereby compromising the safety of whole inverter.

A transformer less inverter based on the concept of virtual DC bus was proposed in [14], which is shown in Fig. 2d. Here the CM leakage current is completely eliminated by connecting the PV negative terminal to grid neutral point. Although this topology exhibits excellent common mode characteristics it can inject only very low power into the grid. This is due to the switched capacitor technique used to maintain the voltage across the virtual DC link. Large deviation in this voltage can lead to very high switch currents. To observe this, this inverter topology is simulated with same parameters as mentioned in [14]. Fig. 18 shows the current stress on switch S3 due to the switched capacitor action. It can be seen that for a grid current of 5A peak, the

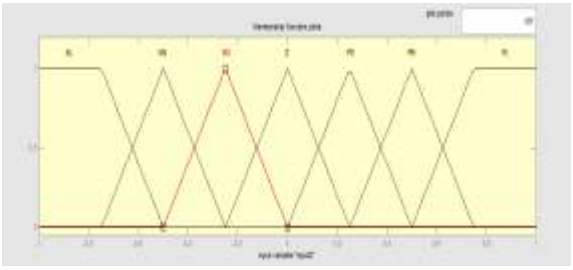
switched capacitor current can be as high as 30A. Therefore, it is evident that this topology is suitable onlyfor very low power application which makes it impracticalfor grid connection. The proposed inverter can completely eliminate CM leakage current with significantly lower current stress on the power switches, thereby lowering their current rating as compared to [14]. Moreover, the inverter can be easily extended to get multilevel output which can further
reduce the filter size requirement. As compared to all othertransformer less topologies, the proposed inverter requires least number of switches for its operation at desired voltage levels.
As explained previously, the proposed inverter has the ability to inject reactive power into the grid thereby making it LVRT capable. In [20], various transformer less inverters were investigated for LVRT capability. It was observed that the FB-DCBP inverter performed satisfactory during LVRT operation for Vg >0.5 p.u. However, the leakage current during LVRT operation was substantial due to varying common mode voltage. This can further deteriorate the grid stability. Proposed inverter is devoid of such issue as it employs direct connection between
the grid neutral and PV panel. Therefore, the proposed inverter can be an exciting alternative to the current transformer less inverter topologies. In order to get better understanding of Type equation here. the performance of proposed inverter, a brief comparison on the basis of key items such as number of capacitors required, number of power switches, number of clamping diodes, Max number of switches conducting per switching cycle, total switch voltage stress, peak switch current stress, output voltage levels, number of filter inductors required, switching, conduction and ESR losses,

Simulation results by using fuzzy controller:

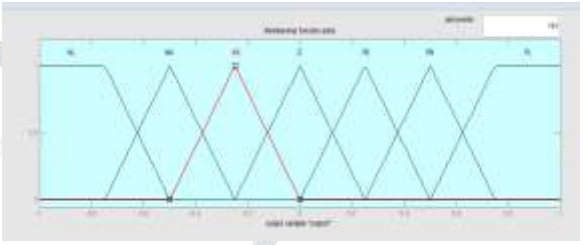
Fuzzy rule is a sort of many-regarded justification in which reality estimations of elements may be any bona fide number some place in the scope of 0 and 1. By separate, in Boolean method of reasoning, reality estimations of components may simply be 0 or 1. Fluffy basis has been contacted manage the possibility of partial truth, where reality regard may go between absolutely apparent and completely false. Moreover, when semantic factors are utilized, these degrees might be overseen by particular capacities.



Membership function for error in input-1



Membership function for change in error input-2



Membership function for output

The 3 variables of the FLC, the mistake, the alternate in error and the output, have 5 triangle membership features for each. The fundamental fuzzy units of membership features for the variables are as proven inside the Figs.8. The fuzzy factors are communicated by semantic factors „positive enormous (PB)", ", „positive little (PS)", „zero (Z)", „negative little (NS)",", „negative huge (NB)", for every one of the three factors.A lead inside the govern base can be communicated in the shape: If (e is NB) and (de is NB), at that factor (album is Z). The tenets are set in view of the facts of the framework and the operating of the framework. The administer base alters the obligation cycle for the PWM of the inverter as in keeping with the modifications within the contribution of the FLC. The amount of ideas can be set as desired. The quantities of guidelines are 49 for the 7 enrollment elements of the blunder and the adjustment in mistake (contributions of the FLC).

$e/\Delta e$	NS	Z	PS	NM	PM	NL	PL
NS	NM	NS	Z	NL	PS	NL	PM
Z	NS	Z	PS	NM	PM	NL	PL
PS	Z	PS	PM	NS	PL	NM	PL
NM	NL	NM	NS	NL	Z	NL	PS
PM	PS	PM	PL	Z	PL	NS	PL
NL	NL	NL	NM	NL	NS	NL	Z
PL	PM	PL	PL	PS	PL	Z	PL

SIMULATION RESULTS:

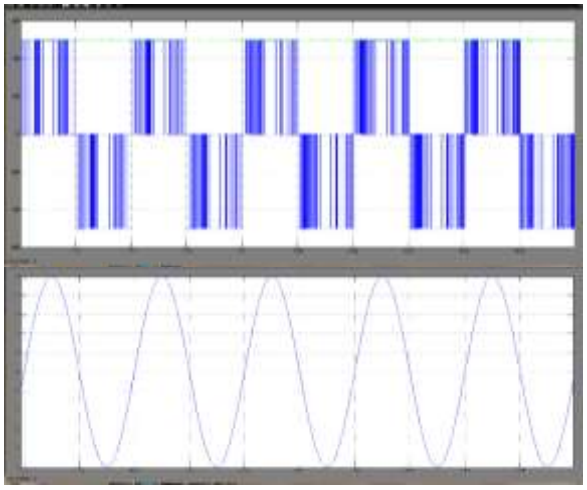


Fig. 5: Simulation results of the 3-level inverter in Mode 1

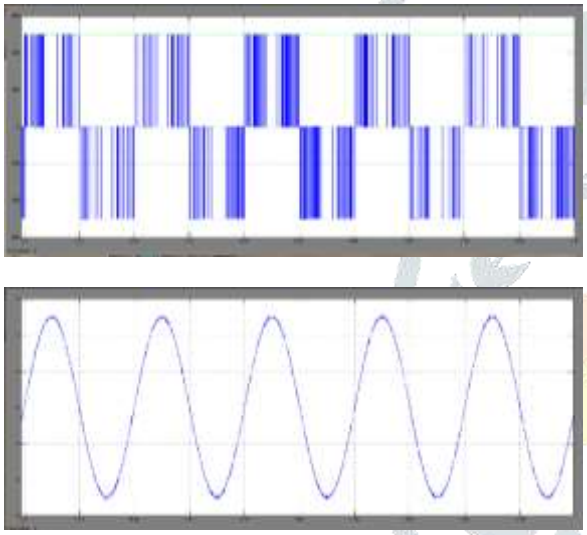


Fig. 6: Simulation results of the 3-level inverter in Mode 2

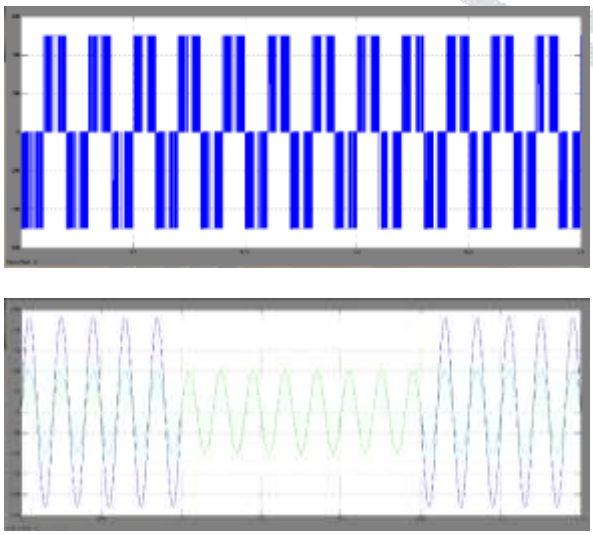


Fig. 7: LVRT capability of the proposed inverter

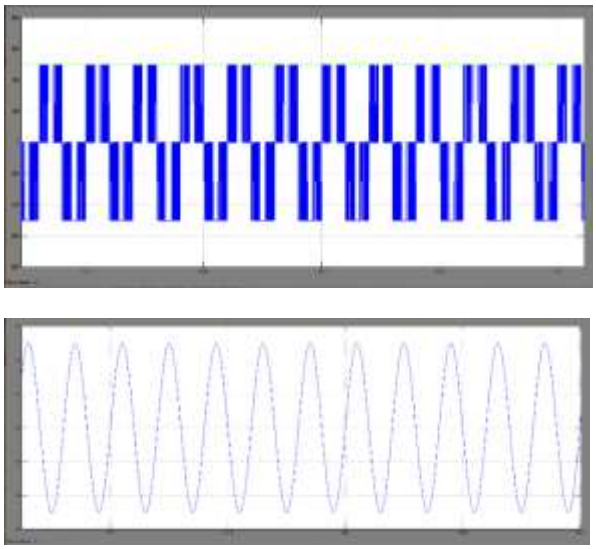


Fig. 14: Precharging of the module capacitor C2

PI CONTROLLER:

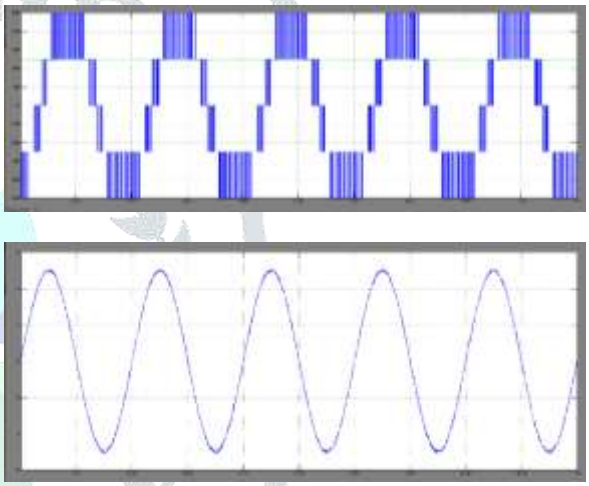


Fig. 16: Simulation results of the 5-level inverter in Mode 2

FUZZY CONTROLLER:

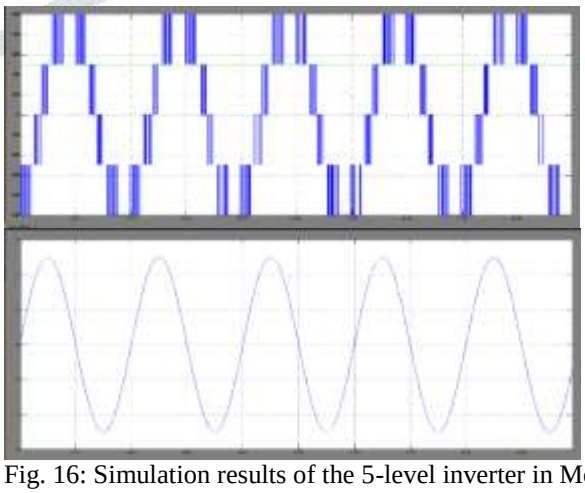


Fig. 16: Simulation results of the 5-level inverter in Mode 2

CONCLUSION

An amazed transformer less PV network related inverter is presented in this paper. The statute properties of proposed transformer considerably less inverter are dense as takes after: 1) Complete stop of CM spillage present day by methods for influencing utilization of ground association with keep away from the PV to stray capacitance. 2) The proposed inverter is estimated in nature and from now on might be strongly connected with get n-level yield by utilizing, for example, legitimate wide assortment of 1/2 augmentation modules. Three) The proposed 3-arrange topology is first of its compose inverter which takes out the CM spillage contemporary with under five vitality switches. 4) The proposed five-degree topology is first of its kind stunned inverter which discards the CM spillage present day with underneath seven vitality switches. 5) As looked at half of platform topologies, no less than 27% and best of a hundred% more yield voltage is gotten for a comparative DC interface voltage. As needs be, the proposed topology might be a less expensive differentiating decision to NPC inverter based topologies. 6) It can convey responsive power help to the framework, which makes it LVRT gifted. 7) It gives a great specific response. Eight) The capacitance need of the proposed inverter is greater than that of ordinary finish augmentation transformer substantially less inverters, as a case, H5, Heric, and FB-DCBP, et cetera 9) Multilevel voltage yield upgrades contemporary THD, nearby those lines reducing channel degree essential With wonderful execution in murdering the CM exhibit, amazed yield voltage and diminishing control equipment value stipulations, the proposed inverter gives an invigorating stunned differentiating decision to the standard transformer less matrix related PV inverters.

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