IMPLEMENTATION OF GNRFET BASED 8-BIT MODIFIED BOOTH MULTIPLIER

Ganesh Kumar M. T[1], Sandeep Malik[2], Madan H. R[3], Dr. Ravish Aradhya H.V[4]
[1]Research Scholar, [2]Assistant Professor, [3]Project Manager, Tarento Technologies, [4]Professor & Associate Dean E&C Dept., RVCE
[1]*Department of Electronics and Communication Engineering,*
[1]*Raffles University, Neermana, Alwar (Raj)-301 705, India.*

Abstract: Multiplication is one of the main operations in the Digital Signal Processors (DSP), so are the image and video processing applications. Hence the performance of CPU is mainly dependent on the optimum multiplier design. The advanced devices like finFET, CNTFETs and GNRFETs promise better solution. GNRFET based designs are considered as a promising technology and guarantee the improved performance in terms of power dissipation, figure of merit, noise margin and area.
8-bit array multiplier and modified Booth multipliers are implemented using GNRFET based technologies in the proposed work. Obtained results are compared with CMOS based multiplier designs. The results infer that GNRFET based modified Booth multiplier offers better performance than CMOS based multiplier designs.

Key words - **Booth Algorithm, Figure of Merit, GNRFETs, Optimum multiplier.**

I. INTRODUCTION

The advent of silicon MOSFET in 1960[1] led to a tremendous advancement in semiconductor industry. With the invention of CMOS in 1965, Dr. Gordon Moore predicted that the number of transistors in a chip double every 18 months[2]. The success of Moore's law is attributed to the scaling theory by Dr. Robert Dennard in 1974[3], which is the theoretical basis to reduce the size of the transistors. As the process technology entered the nanometre regime, short channel effects started to persist and leakage current increased, leading to increased power consumption. At the same time, the sale of portable devices and the battery-operated devices increased, which made power consumption to be one of the major design concerns in the design of electronic systems[4]. Research was done to find techniques to design systems which dissipate low power and to determine an alternative device to conventional CMOS technology.

1.1 Advanced Devices

Various concepts on all hierarchical levels have been proposed to decrease active losses in static CMOS circuits. Active losses are described by $P_T = \alpha C V_{DD}^2$, where V_{DD} is the power supply, C is the capacitance of the circuit, α is the activity factor. V_{DD} scaling is the technique employed to decrease power consumption in circuits as it is the most effective way to decrease active losses. V_{DD} scaling reduces the active losses in the circuit, but at the expense of increased delay. The capacitance is determined by the intrinsic capacitance of the devices in the applied technology, and the parasitic capacitances due to inter-connect. The parasitic capacitance can be minimized by compact layout of integrated circuits. Activity can be decreased by avoiding unnecessary switching losses due to glitching[5].

Devices beyond CMOS like FinFETs and CNTFETs (Carbon Nano tube FET) came to being in the 14nm process technology and less, as a measure to avoid the trade-off between area and power consumption [6]. However, GNRFET has been proven to be a potential replacement to conventional CMOS technology. Graphene is a two-dimensional sheet of Carbon atoms having a honeycomb lattice. Graphene is intrinsically having zero band-gap between the valance-band and conduction-band, making it a conducting material[7]. The 2D Graphene sheets are patterned into 1D ribbons to induce a band gap in the Graphene structure. These ribbons are called Graphene Nano-Ribbons (GNR). The band-gap is inversely proportional to the width of the GNR. The GNR forms the channel material in GNRFET and has many advantages like high carrier mobility and low gate-tunnelling current resulting in a low-power device [8, 9].

II. INTRODUCTION TO MULTIPLIERS

Multipliers play a pivotal role in many high-performance systems such as Microprocessor, FIR filters, Digital Processors, etc. In its early stage, multiplication algorithms were proposed by Burton and Noaks in the year 1968, by Hoffman in the year 1986 and by Guilt and De Mori in the year 1969 for positive numbers. In the year of 1973 and 1979, Baugh-Wooley and Hwang proposed multiplication algorithm for numbers in two's complement form. Multiplication is hardware intensive and the main criteria of interest are higher speed, lower cost and lower power. With development in technology, several researchers have tried multipliers which provide design targets such as low power consumption, increased speed, and regularity of layout or combination of them in one multiplier. This helps making them suitable for achieving compact high speed and low power implementation. The performance of a

system is generally controlled by the performance of the multiplier as the multiplier takes more time to process the data and complete the operation in a digital system[10]. Furthermore, multiplier is normally the most area consuming element in the system. Therefore, optimizing its speed and area are the key design factors. However, area and speed are generally the conflicting constraints improving speed which results mostly in large area. With ever increasing applications in portable equipment and mobile communications, the demand for high performance, low-power VLSI systems is gradually increasing[10]. Digital signal processors and application specific integrated circuits depend on the efficient implementation of arithmetic circuits (adder and multiplier) to execute dedicated algorithm such as convolution, correlation and filtering.

Multiplier being a hardware intensive and time-consuming critical application, Booth multiplier found to be more effective algorithms for the low power and fast processing applications.

The advancement of technology is resulting in the reduced transistor size. The reduction in the transistor size is mainly due to the shrinking of transistor resulting in the reduction of the chip area. Reduced transistor size is very much required to support mobile applications. The shrinking of CMOS transistors beyond 45nm directly affects the performance of the MOS transistor due to the short channel effects, increased leakage currents and power dissipation. This resulted in the advancement of technology with new devices, low power designs and fast processing technologies [11].

III. GNR FIELD EFFECT TRANSISTOR (GNRFET)

The channel material in a transistor can be a bilayer graphene or micron - wide graphene sheet or a GNR, thereby giving a wide variety of graphene transistors. Graphene transistors that contain GNR as their channel material are termed as GNR Field Effect Transistors (GNRFETs).

GNRFETs have two variants namely, Schottky barrier (SB) - type and Metal Oxide Semiconductor (MOS) - type[10]. The former uses metal contacts and graphene channel while in the latter, the reservoirs are doped with acceptor and donor impurities. SB-type GNRFETs have lower I_{on}/I_{off} ratio compared to MOS-type GNRFETs, thus making MOS-type superior in device performance. Depending upon the doping material, there are two types of MOS-type GNRFETs, namely N-type and P-type. N-type GNRFETs and P-type GNRFETs are obtained by doping with donor and acceptor impurities respectively[12].

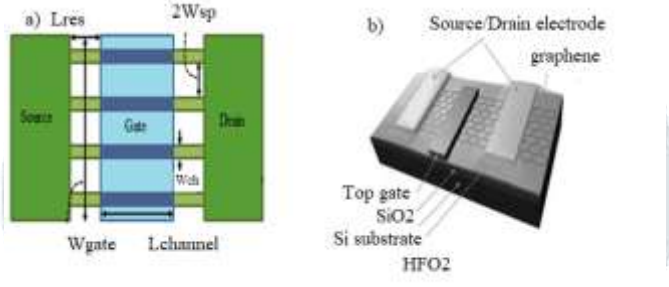


Fig 3.1: (a) Top view of GNRFET (b) side view of GNRFET [10]

The structure of MOS-type GNRFET is as shown in Fig 3.1. In a single GNRFET, to increase the drive strength, multiple graphene ribbons with armchair chirality are connected in parallel. GNRs under the gate are un-doped, while those between the wide contacts and gate are doped heavily with a f_{dop}, doping fraction. The un-doped (intrinsic) part is called channel while the doped parts are called reservoirs. Channel length is L_{ch}, reservoir length is L_{res}, ribbon width is W_{ch}, gate width is W_{gate} and ribbon spacing is $2W_{sp}$ [12].

In order to reduce the number of metal-graphene contacts, multiple layers of metal are used on top of the single graphene layer. Gates are located on the first layer of metal while drains, channels and sources on the layer of graphene. Logic gates are connected with each other on metal layer and connections within each logic gate are made on the layer of graphene without vias. Both Zigzag and armchair GNRs serve as good conductors above 20nm width and hence can be used as local interconnect for routing on the graphene layer. Since the input to the logic gate is on the metal layer and the output (drain/source) is on the layer of graphene, the use of metal-graphene vias cannot be avoided [32].

IV. BOOTH MULTIPLIER

The modified Booth recoding algorithm is the most frequently used method to generate partial products [14,15]. This algorithm allows for the reduction of the number of partial products to be compressed in a carry-save adder tree. Thus the compression speed can be enhanced. This Booth–Mac Sorley algorithm is simply called the Booth algorithm, and the two-bit recoding using this algorithm scans a triplet of bits to reduce the number of partial products by roughly one half. The 2-bit recoding means that the multiplier is divided into groups of two bits, and the algorithm is applied to this group of divided bits. The Booth algorithm is implemented into two steps: Booth encoding and Booth selecting. The Booth encoding step is to generate one of the five values from the adjacent three bits. The Booth selector generates a partial product bit by utilizing the output signals [14].

One advantage of the Booth multiplier is, it reduces the number of partial product, thus make it extensively used in multiplier with long operands [14,15]. The main disadvantage of Booth multiplier is the complexity of the circuit to generate a partial product bit in the Booth encoding.

4.1 Modified Booth Algorithm using pipeline technique

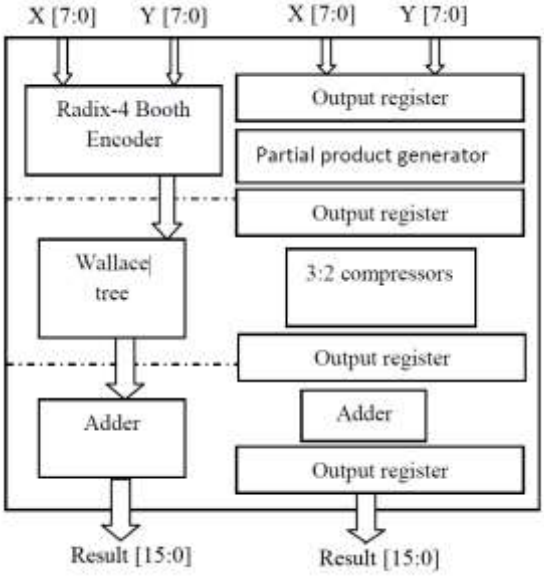


Fig. 4.1: Modified Booth Algorithm using pipeline technique

Pipeline technique is an effective design for binary multiplication using modified booth multiplier[15]. The block diagram of the modified Booth multiplier is shown in the Fig. 4.1. It increases the computing speed by combining the concept of parallel processing and pipelining into a single concept. The data flows synchronously across the array between neighbors, usually with different data flowing in different directions.

V. IMPLEMENTATION

5.1 Array Multipliers

Conventional 8-bit array multiplier has been designed and simulated using CMOS and GNRFETs. The schematic diagram of the conventional 8-bit array multiplier design is shown below in the Fig. 5.1.

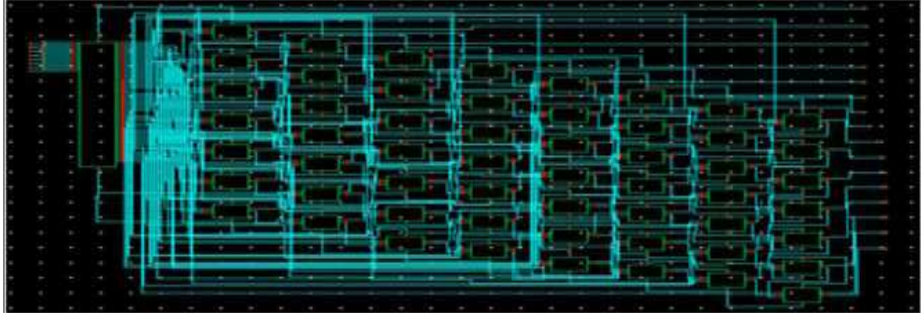


Fig. 5.1: Schematic diagram of conventional 8-bit array multiplier

The corresponding waveform of the designed 8-bit array multiplier is shown in the Fig. 5.2.

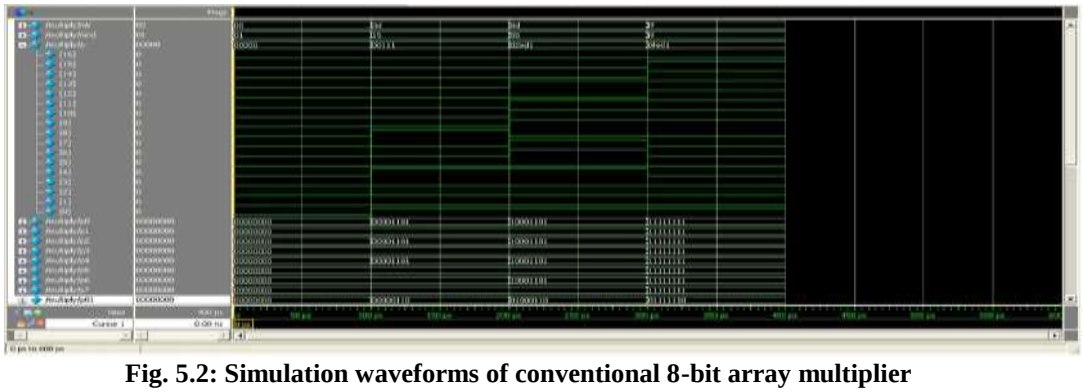


Fig. 5.2: Simulation waveforms of conventional 8-bit array multiplier

5.2 Modified Booth Multipliers

Modified Booth multipliers are designed and simulated using CMOS and GNRFET based devices. The schematic and the waveforms of the 8-bit modified booth multiplier has been shown in the Fig. 5.3 and Fig. 5.4 respectively.

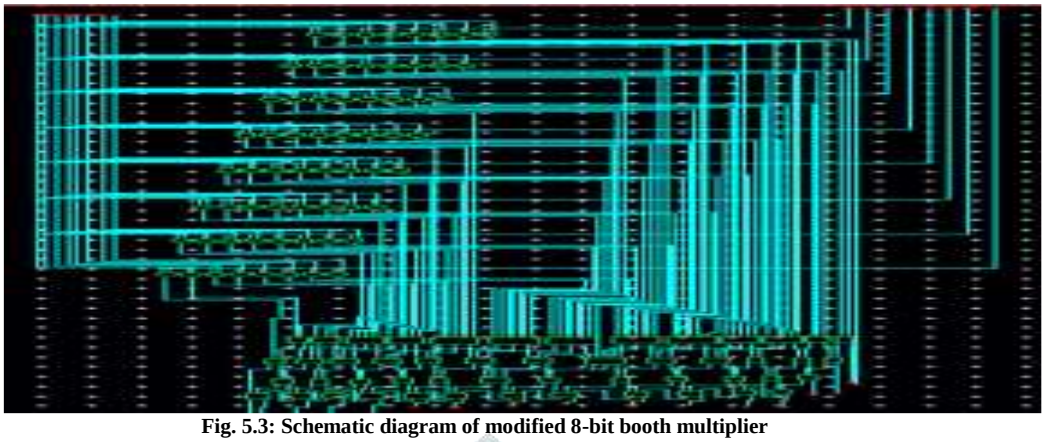


Fig. 5.3: Schematic diagram of modified 8-bit booth multiplier

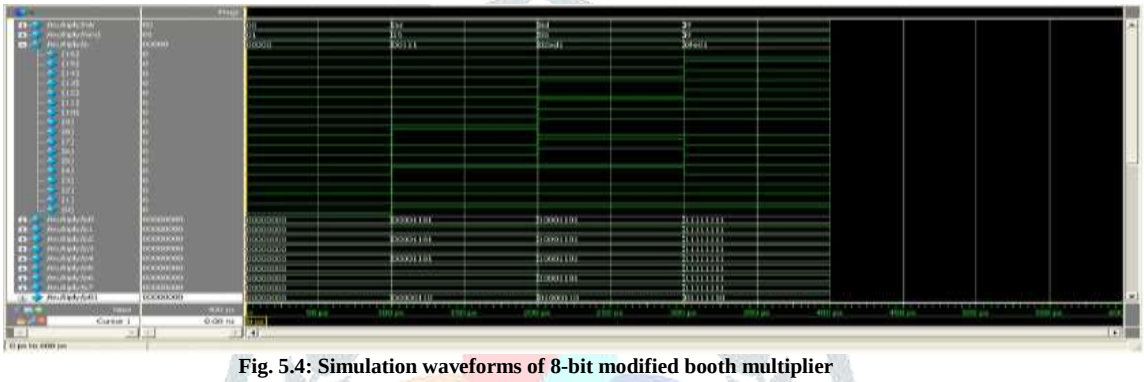


Fig. 5.4: Simulation waveforms of 8-bit modified booth multiplier

VI. RESULT ANALYSIS

CMOS technology based and GNRFET technology based 8-bit array multiplier and modified Booth multiplier have been implemented successfully. For both the designs, the all-important performance parameters namely the total power dissipation, propagation delay (critical) and power delay product are observed and recorded.

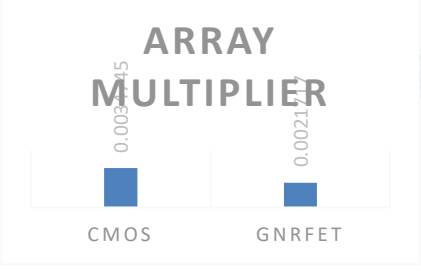


Table 5.1: Power Dissipation of Array multipliers

Power Dissipation (w)	CMOS	GNRFET
Array Multiplier	0.0034745	0.0021717

Figure 5.1: Power dissipation of 8-bit Array multiplier

The CMOS technology based and GNRFET technology based 8-bit array multipliers results are recorded as indicated in Fig 5.1. The obtained result indicates that the 8-bit array multipliers using CMOS and GNRFET based technology dissipates 3.47mW and 2.17mW respectively, indicated in Table 5.1. This clearly implies that GNRFET based 8-bit array multiplier dissipates 62.5% lesser power as compared to CMOS based 8-bit multiplier.

CMOS and GNRFET based modified Booth multipliers have been simulated and recorded as indicated in Fig 5.2. The obtained results indicate that the 8-bit modified Booth multipliers using CMOS and GNRFET based technology dissipate 218.71µW and 65.35µW respectively, indicated in Table 5.2. This clearly implies that GNRFET based 8-bit array multiplier dissipates lesser power as compared to CMOS based 8-bit.

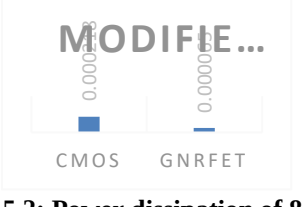


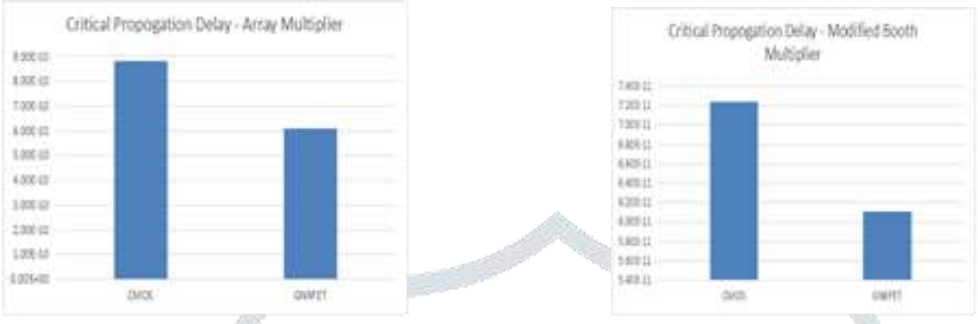
Table 5.2: Power Dissipation of modified Booth multiplier

Power Dissipation (w)	CMOS	GNRFET
Modified Booth Multiplier	0.00021871	0.000065351

Figure 5.2: Power dissipation of 8-bit Modified Booth multiplier

GNRFET based multiplier dissipates lesser power as compared to CMOS based multiplier due to Graphene characteristics such as low gate capacitance, tunneling current and low V_{dd}. CMOS based designs serves as a reference design to compare the performance parameters of multipliers. CMOS based multipliers employ the traditional switching operation with a constant power supply and hence dissipates more power as compared to GNRFET based multipliers.

Critical propagation delay of 8-bit array multiplier designs have been computed for both the designs. Figure 5.3a and 5.3b shows the critical propagation delay of 8-bit array multipliers and modified booth multiplier designs respectively. The simulation result in Fig 5.3 shows that the GNRFET based designs offer reduced propagation delay in comparison to CMOS based multiplier designs. The results are recorded in Table 5.3.



(a) **(b)**

Figure 5.3: Critical propagation delay of various multiplier designs

Table 5.3: Critical propagation delay of array multipliers

Delay (s)	CMOS	GNRFET
Array Multiplier	8.82E-10	6.08E-10
Modified booth Multiplier	7.24E-11	6.11E-11

The Power-Delay product is computed for both the array multiplier and modified Booth multiplier. The results are shown in Fig 8. GNRFET based multipliers offer reduced propagation delay and dissipate lesser power as compared to CMOS based multiplier designs. GNRFET based multiplier designs offer reduced Delay as compared to CMOS based designs.

Power-Delay product is computed for both the array multiplier and modified Booth multiplier. The results are shown in Fig 5.4a and Fig. 5.4b respectively. GNRFET based multipliers offer reduced propagation delay and dissipate lesser power as compared to CMOS based multiplier designs; indicated in Table 5.4. GNRFET based multiplier designs offer reduced Power Delay Product (PDP) as compared to CMOS based designs.

(a) **(b)**

Figure 5.4: Power delay product comparison of GNRFET and CMOS based 8-bit array multiplier

The comparison of the power Delay Product of the array multiplier and modified booth multipliers designed using CMOS and GNRFETs have been tabulated in table 5.4 and plotted in Fig. 5.5. The results clearly imply that the PDP of GNRFET based multiplier designs are negligible as compared to the CMOS based designs and the GNRFET based modified booth multiplier offers least PDP as compared to the other three multiplier designs.

Figure 5.5: PDP of multiplier designs

Table 5.4: PDP of CMOS and GNRFET based Array multiplier and modified Booth multipliers

PDP (WS)	CMOS	GNRFET
Array Multiplier	3.06E-12	1.32E-12
Modified Booth Multiplier	1.58252E-14	3.99549E-15

VII. CONCLUSION AND FUTURE ENHANCEMENT

CMOS and GNRFET based 8-bit array multiplier and modified Booth multiplier have been designed and simulated. The power dissipation, delay and Power-delay product have been computed for both the designs. GNRFET based modified booth multiplier offers low power dissipation, less propagation delay and reduced PDP as compared to the CMOS designs.

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