Integrated Optical Receiver Implementation using CMOS Technology

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Abstract:

In circuits and systems for short distance communications optical receivers with monolithically integrated photo detectors can be used. In this the entire optical receiver can be implemented in standard CMOS technology. Not only save the extra overhead and cost during assembly for multichip solutions, but also ground bounce issues, ESD problems, and parasitic associated with bond pads and bond wires can also be eliminated. CMOS technology uses a combination of spatially modulated light (SML) detector, Transimpedance amplifier, differential gain stage, Post amplifier and an analog equalizer while designing a optical receiver. A transimpedance amplifier is operated with 3.3v supply, while the rest of the circuit blocks are powered with 1.8v supply. These different circuits are implemented using a TOP Spice tool and PSpice tool and compared the results.

Key words: CMOS integrated circuits, negative miller capacitance, transimpedance amplifier (TIA), Electrostatic Discharge (ESD), photo detector, equalizers.

1. Introduction

Optical receivers have been proposed for transmission data rates ranging from a few hundreds of Mbit/s to few Gbit/s over distances of the order of 10 to 1000m. The wide spread penetration of fiber networks in to homes and business will require a low cost and high reliability while transmitting the data bits A Numerous high performance GaAs [1] receivers have been demonstrated in the past few years, based on the combination of metal-semiconductor–metal(MSM) photo detector with transimpedance amplifiers this causes high cost due to high technologies on the other hand, CMOS technology [2] is more attractive than GaAs because of its low cost and potential for very large scale integration.

However the optical receiver with monolithically integrated photo detector can be used for communication systems. In this paper various key features of the photo detector, like process compatibility, large band width, high responsitivity and low operating voltage can be achieved with p-i-n Photo detector [3]. The band width of photo detector, built on bulk silicon is severely degraded. This occurs because most of the photons are absorbed in the undepleted region of semiconductor, where the photo generated carries are not subjected to the electric field generated by the surface electrodes. The minority carriers diffuse with in the neutral bulk and eventually, part of them may be collected by the electrodes the time gap dependent on the slow diffusion effect, resulting in a degradation of photo detector speed performance.

To improve performance of photo detector it is implemented in CMOs technology as photo detector with SML detector[4] which consists of a row of photo detector alternatively covered and uncovered with a light blocking metals. The SML photo detector is capable of high speed operation with smaller responsivity [5].when equalization has also been applied to solve this problem. The equalizer circuit is as shown in the figure (1).

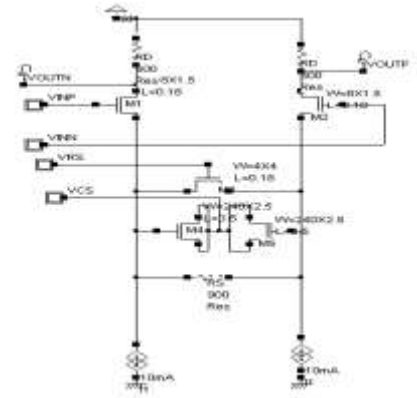

fig1: Schematic of Equalizer

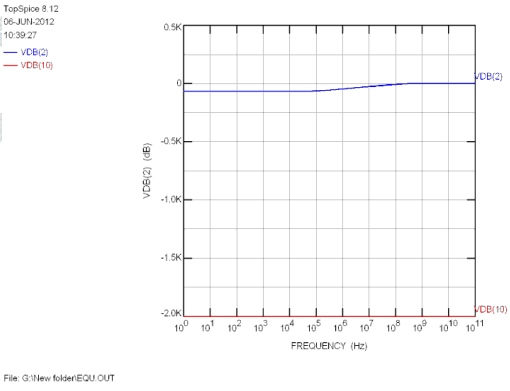

fig 2: Equalizer frequency response

The frequency response of the photodetector with equalizer circuit is as shown fig (2).And it was selected for the receiver integration in this design.

II. Integrated Optical Receiver:

The architecture of the optical receiver is as shown in fig (3). This integrates an on chip SML detector [6], a

Transimpedance amplifier, differential gain stage, post amplifier and output buffer on a single chip.

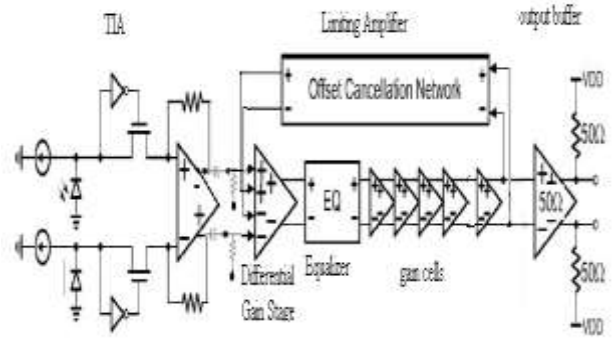

fig 3: Optical receiver block diagram

The entire optical receiver front end begins with the SML detector that converts the incident optical power into two currents. When the subtraction of these two signals is performed, the signal due to slow diffusive carriers from the substrate can be removed, and the bandwidth of the photodetector can be improved. A differential TIA [7] converts the two currents from the photodiodes into two voltages. The photodiodes are dc coupled to the TIA to avoid the extra parasitic capacitance due to ac coupling. A supply voltage of 3.3 V was used in the TIA to provide a high reverse-bias voltage for the photodiodes so that large photodetector bandwidth and responsivity can be achieved simultaneously. AC coupling with a cutoff frequency of 100 kHz was used to connect the TIA to the rest of the circuit blocks that operate from a 1.8-V supply. A differential gain stage follows the ac coupling to further improve common-mode rejection. An equalizer and a post amplifier (PA) follow to further remove Intersymbol Interference (ISI) and increase the signal swing, respectively. For testing purposes, an output buffer was used to drive the signal to the oscilloscope [8].

1. Transimpedance amplifier:

Fig (4) illustrates the circuit schematic of the Transimpedance amplifier with SML detector. It consists two differential amplifier are (M1, M2, M5) & (M3, M4, M6) cascaded.

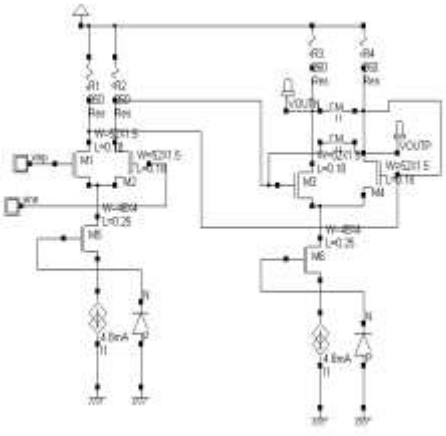

fig 4: Schematic of Transimpedance amplifier

Here the transistor size is specified as N_f x W_f/L where N_f, W_f &L represents the number of fingers, finger width and the finger length respectively. In this TIA we give input voltages less than 1.8v&here we give input voltages less than 1.8v& supply is 3.3v.here we use a negative miller capacitance [9] is employed to improve the pole frequency and to increase the overall TIA band width and also it reduces the parasitic capacitances between the two cascaded stages.

Frequency response curves:

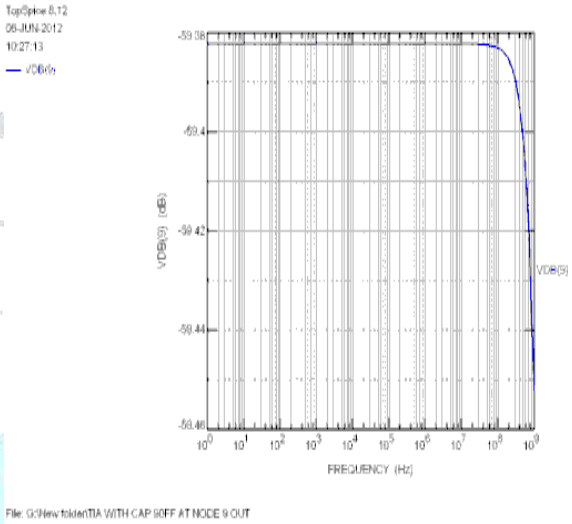

Fig: a frequency response TIA with 90fF capacitor

Here the frequency response curves are as shown for TIA with 90fF, without and with 150fF capacitors respectively.

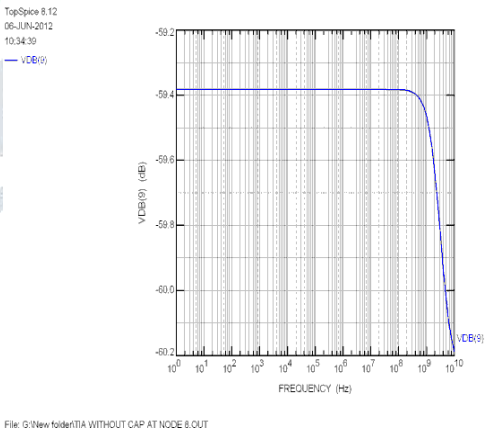

Fig: b frequency response TIA without capacitor

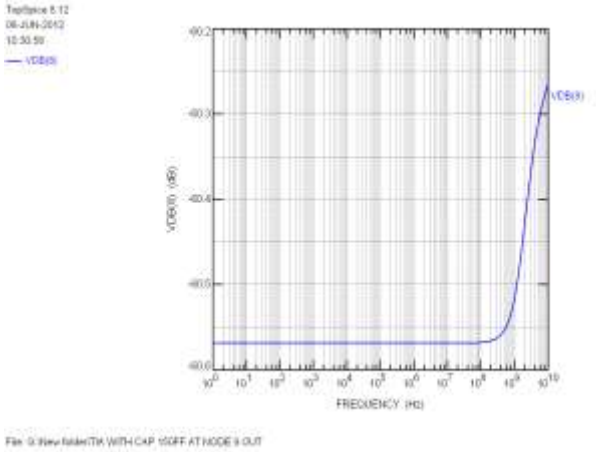

Fig: c frequency response TIA with 150fF capacitor

2. 2.AC Coupling:

AC-coupling is used to change the common-mode voltage level when interconnecting different physical layers [10]. A simple example is shown in Figure

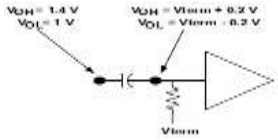

Fig 5: ac coupling circuit

Since the TIA is the only block using a 3.3-V supply, ac coupling provides a shift down in the common-mode voltage going into the subsequent stage. The values of R_{ac} and C_{ac} were chosen so that the cutoff frequency is 100 kHz, which is low enough to pass the lowest frequency content of a 2^{31}-1 pattern at 3–5 Gbits/s. To reduce the load on the TIA, a combination of lower C_{ac} and higher R_{ac} were used, as shown in Fig.5

3. 3.Differential Gain stage:

The architecture of differential gain stage is as shown in fig (6)

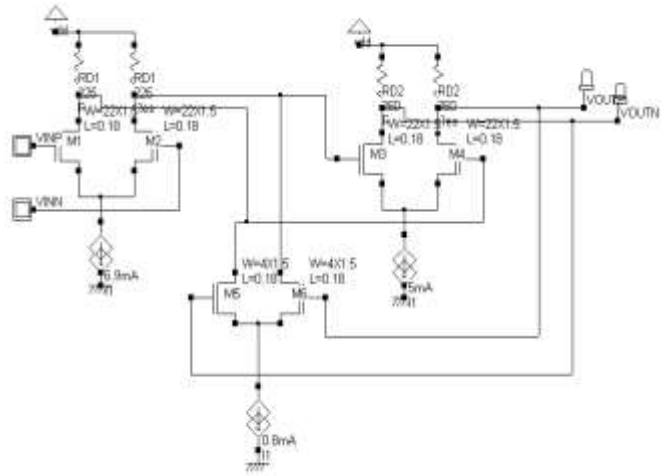

Fig: 6: Schematic Differential gain stage

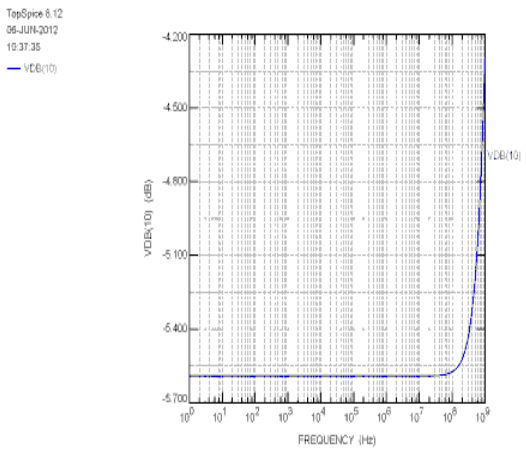

fig:7:frequency respose of the differential gain stage

Mainly this circuit is based on Cherry-Hooper amplifier [11] with active feedback to achieve high gain bandwidth. The transfer function for the output and input of the differential gain stage is as given in equation (1)

$$\frac{V_{out}}{V_{in}}(S)=\frac{A_{vo}\,w_n^2}{s^2+2\zeta w_n s+w_n^2} \qquad \ldots\ldots\ldots\ldots \quad (1)$$

M1 and M3 are used for lower power consumption and also a gain cell is provided for the equalizer to work properly.

4. Limiting Amplifier:

Mainly the limiting amplifier is used for amplify the signal coming from equalizer which is composed of a chain of 5 gain cells and an offset cancellation circuit. The gain bandwidth equation is as shown below

$$GBW=w_c X\left[\frac{1}{2^{\frac{1}{n}}-1}\right]^{\frac{1}{4}} X\, A_c^{\frac{1}{n}} \qquad \ldots\ldots\ldots\ldots\ldots (2)$$

The limiting amplifier circuit and corresponding frequency responses as shown in fig(7),fig(8) respectively

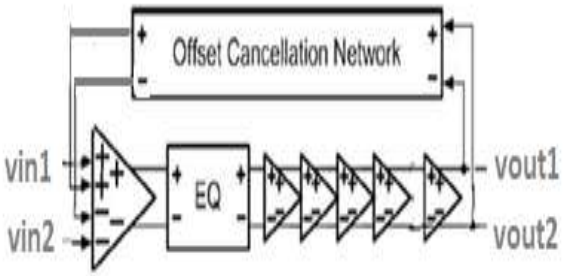

fig: 7: Schematic Limiting amplifier

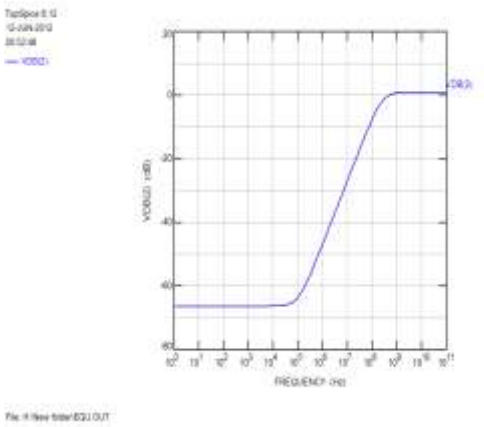

fig:8:frequency respose of the limiting amplifier

5. Double frequency output buffer:

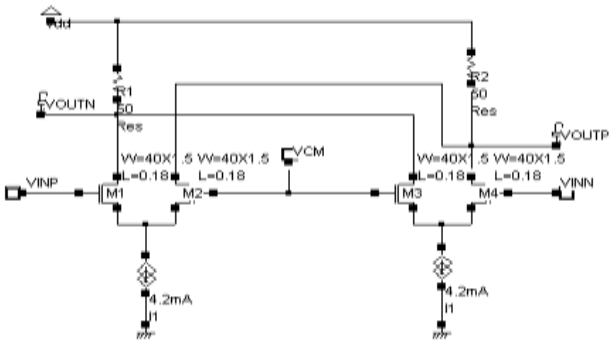

Fig:9 schematic of output buffer

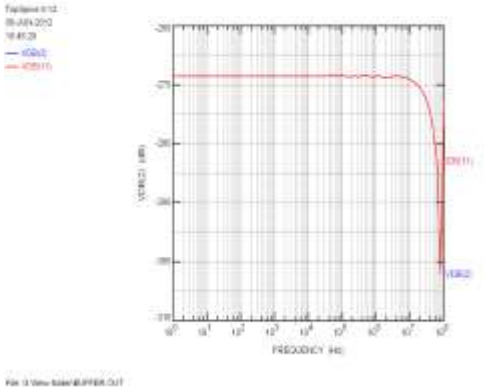

fig:10:frequency respose of the output buffer

This circuit is used to half the input capacitance as the signal goes through the limiting baud rate can be improved .the frequency response for the output buffer is as shown in fig(10)

VI. Measurement Results:

The Optical receiver may implement a poly six-metal 0.18**µ**m CMOS technology. It includes Photodetector, Transimpedance amplifier, AC coupling, differential gain stage, Equalizer, Post amplifier and Output buffer. Here a power meter and a multimeter were used to measure the input optical power and the output current in order to determine the dc responsivity of the photodetector. With an input power 500 W, the currents coming from both the exposed and covered photodiodes were 64.4 and 38.5 A, respectively, when the reverse-bias voltage was set to 2 V. This leads to a net responsivity of 0.052 A/W. The net responsivity of the photodetector was also measured at other reverse-bias voltages, and the result is shown in Fig.23 As expected, the net responsivity increases with the reverse-bias voltage since increasing the reverse-bias voltage increases the width of the depletion region in the photodiode. For a fixed optical power, this causes more carriers to be captured by the electric field in the depletion region, resulting in less recombination of electron–hole pairs, thus translating to a higher responsivity.

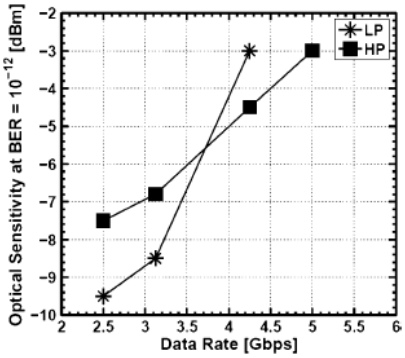

Fig 11: optical sensitivity with BER of less than10^{-12} for Different data rates with different modes

Fig. 11 shows the optical sensitivity with a BER of less than10^{-12} at different data rates in both modes. The sensitivity is better in the LP mode at lower data rates because an increased TIA bandwidth in the HS mode leads to a higher total integrated noise. Therefore, while the HS mode is suitable for higher data rates, the LP mode is preferred for data rates below 4.25 Gbits/s from both power consumption and sensitivity perspectives.

VII.CONCLUSION

By combining an SML detector and an equalizer in a monolithically integrated photodetector, a maximum data rate can be achieved. It is the fastest photodetector integrated in a standard CMOS technology using standard supplies at or below 3.3 V. A low-noise TIA with high bandwidth and high transimpedance gain has also been proposed. By employing a negative Miller capacitance, the bandwidth of the TIA can be extended while keeping a flat frequency response. it used a very high supply voltage of 13.9 V to reverse-bias Moreover, since the TIA and PA were not integrated on chip with the photodetector, an external TIA was used for testing. In conclusion, the optical receiver achieves better sensitivity The improvement in sensitivity justifies the design of the proposed low-noise TIA compared to the TIA with an RGC input stage [5] [8]. And the frequency responses of the different stages can be implemented in Top spice tool and compares output of the corresponding blocks

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