Modified Cascaded Multilevel Inverter for PV System

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Abstract: In this paper, a Modified Five level cascaded multilevel Inverter topology is proposed which is useful for the minimization of leakage current. The number of switches is reduced as compared to the conventional five level CMLI. The proposed topology is connected to a PV system and its performance is studied. Topology consists of eight switches and complementary switching is employed for only four switches. Thus PV and Grid source can be isolated during Zero voltage state condition.

The PWM technique employed for proposed converter reduces High frequency voltage transitions and common mode voltages. This helps in reduction of leakage current to considerable level. MPPT technique is employed for proposed topology , which helps in reducing the common mode voltages and high frequency voltage transitions. The harmonics in Grid currents are also reduced and meet the IEEE 1547 Standard. The proposed Modified Five level CMLI is simulated using MATLAB/Simulink.

Keywords **– Cascaded Multilevel Inverter (CMLI), Photo voltaic (PV),Pulse Width Modulation (PWM), Common-Mode Voltage (CMV), Total Harmonic Distortion (THD),Leakage current, terminal voltage.**

I. INTRODUCTION

Multilevel inverter technology has been developed as a very significant alternative in the area of medium and high power applications. Jose Rodriguez discussed the most important topologies like diode clamped inverter, flying capacitor inverter, cascaded multi-cell with separate DC sources and emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters [3]. The most relevant control and modulation methods developed for this family of converters like multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination and space vector modulation were also discussed. Special attention was devoted to the latest and more relevant applications of these converters such as conveyor belts, laminators and unified power flow controllers. Finally, the peripherally developing areas such as high-voltage, high power devices, optical sensors and other opportunities for future development were addressed. The Sun is a very large of perennial source of energy, so this energy consumption can meet the present and future requirements on continues basis. This attracts attention in the world. The energy from sun i.e., Solar energy is converted to usable electricity. Solar power uses photovoltaic (PV) cells for the conversion of sunlight into electricity. The output from solar cell is in form of Direct current (DC).

1.1 Cascaded Multilevel Inverter

There is a growing interest in multilevel topologies since they can extend the application of power electronics systems to higher voltages and power ratios. Multilevel inverters are the most attractive technology for the medium to high voltage range, which includes motor drives, power distribution, power quality and power conditioning applications. A cascaded multilevel inverter by Corzine et al (1999) Liu et al (2006) consists of a series of H-bridge inverter units [2]. The general function of this multilevel inverter is to synthesize a desired voltage from several separate DC sources, which may be obtained from batteries, fuel cells, or solar cells. A particular advantage of this topology is that the modulation, control and protection requirements of each bridge are modular.

The cascaded inverter has been largely studied and used in the various fields such as drives, transmission system and power conditioning Corzine et al(2002) [2] .The cascaded H-Bridge multilevel inverter are the most advanced and important method of power electronic converters that analyses output voltage with number of dc sources as inputs .As compared to neutral point clamped multilevel inverter and flying capacitor multilevel inverter, the cascaded H-Bridge multilevel inverters requires less number of components and it reaches high quality output voltage which is close to sine wave. By increasing the number of output levels the total harmonic distortion in output voltage can be reduced.

In cascaded H-Bridge multilevel inverter required AC output voltage is obtain by synthesizing number of DC sources. The number of H-Bridge units with different DC sources is connected in series or cascade to produce cascaded H-Bridge multilevel inverter.

1.2 Features of Cascaded Multilevel Inverter

1. Synthesis of higher voltage levels using power devices of lower voltage ratings.
2. Increased number of voltage levels which leads to better voltage waveforms and reduced total harmonic distortion in output voltage.
3. Reduced switching stresses on the devices due to the reduction of step voltages between the levels.
4. It not only solves harmonics and EMI problems,[2] but also avoids possible high frequency switching stress dv/dt.

1.3 Solar Panel

A photovoltaic (PV) module is a packaged, connect assembly of typically 6x10 photovoltaic solar cells. Photovoltaic modules constitute the photovoltaic array of a photovoltaic system that generates and supplies solar electricity in commercial and residential applications.

Each module is rated by its DC output power under Standard Test Conditions (STC), and typically ranges from 100 to 365 Watts (W). The efficiency of a module determines the area of a module given the same rated output – an 8% efficient 230 W module will have twice the area of a 16% efficient 230 W module.[2] There are a few commercially available solar modules that exceed efficiency of 22% and reportedly also exceeding 24%.

A single solar module can produce only a limited amount of power; most installations contain multiple modules. A photovoltaic system typically includes an array of photovoltaic modules, an inverter, a battery pack for storage, interconnection wiring, and optionally a solar tracking mechanism.

II.PROPOSED SYSTEM

2.1 Introduction

An improved Cascaded Multilevel Inverter (CMLI) with five level topology based on a highly efficient and reliable configuration for the minimization of the leakage current is proposed. Apart from a reduced switch count, the proposed scheme has additional features of low switching and conduction losses. The proposed topology with the given Pulse Width Modulation (PWM) technique reduces the high frequency voltage transitions in the terminal and common mode voltages.

Avoiding high-frequency voltage transitions achieves the minimization of the leakage current and reduction in the size of electromagnetic interference filters [5].

The schematic circuit diagram of the proposed five-level CMLI for PV system is shown in Fig.1 The given configuration consists of two converters (Conv-1 and Conv-2). Conv-1 is a half-bridge inverter comprising two switches S_{11} and S_{12}. The Conv-2 comprises of a highly efficient and reliable inverter configuration with six switches (S_{21} to S_{26}). [5]Among the six switches, four switches (S_{21} to S_{24}) in Conv-2 constitute an H-bridge circuit. The remaining two switches S_{25} and S_{26} in Conv-2 are bi-directional switches. The switches in the Conv-1 are used to generate the voltage levels of V_{PV} and $V_{PV/2.}$ When switch S_{11} is turned ON, the voltage V_{PV} is applied at the terminal n with respect to the terminal z. Similarly, the terminal n attains the voltage $V_{PV/2}$ when switch S_{12} is turned ON. The switches S_{11} and S_{12} are complementary in nature. The generated voltage levels at the terminal n of Conv-1 are given as an input to the Conv-2.

The Conv-2 generates the positive, negative and zero levels of corresponding input voltage (voltage between the terminals n and z) across the load. The bi-directional switches S_{25} and S_{26} provide the free-wheeling path during zero voltage state. The output of the five-level CMLI is connected to the grid through an LCL filter as shown in fig.1 [6-8].

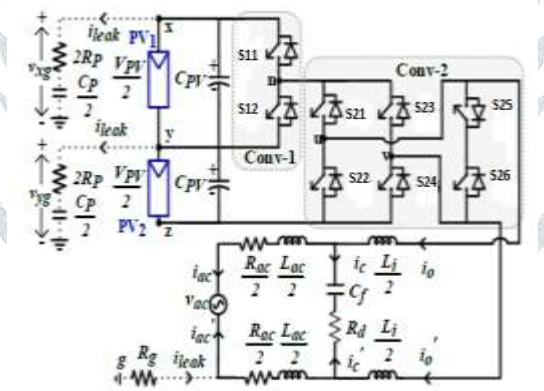


Fig: 1: Proposed five-level grid- connected CMLI with PV and parasitic elements.

It consists of inverter side inductance L_i, capacitance C_f and grid side inductance Lac. The resistance R_d in the shunt branch of the filter is used as a damping resistor. The resistance R_{ac} refers to the grid side resistance and the resistance R_g indicates resistance in the ground path. The variable v_{ac} refers to instantaneous grid voltage. The variables R_p and C_p refer to the parasitic resistance and capacitance in the PV system, respectively shown with dotted lines in Fig:1 the parasitic capacitance in PV system forms a resonant circuit with the filter inductances.[6] The variables i_o, i_c and i_{ac} denote the output current of five-level CMLI, current flowing through shunt branch of the filter and the current flowing into the grid respectively. The current i_{leak} indicates the leakage current flowing from the PV array into the ground through parasitic capacitance (see Fig.1).

The proposed MLI topology contains four pairs of complementary switches (S_{11}, S_{12}), (S_{21}, S_{22}), (S_{23}, S_{24}) and (S_{25}, S_{26}) in the proposed configuration. However, to minimize the leakage current, the complementary switching is employed only for the two pairs of switches (S_{11}, S_{12}) and (S_{25}, S_{26}).Avoiding complementary action for the other pairs of switches helps in isolating the PV and the grid source during zero voltage state. Fig. 2 shows the operation of the inverter in all its switching states. The inverter output voltage V_{uv} at different voltage levels [1] with the corresponding switching states of all the switches are shown in Table I. The inverter output voltage V_{uv} attains the voltage levels $+V_{PV}$ or $-V_{PV}$ when switch S_{11} is turned ON along with other inverter switches (S_{21}, S_{24}) or (S_{22}, S_{23}) respectively as shown in Figs.2(a) and 2(e). Similarly, the voltage levels $+V_{PV/2}$ or $-V_{PV/2}$ are obtained at V_{uv} when switch S_{12} is turned ON with the same switching combinations as shown in Figs. 2(b) and 2(d).The most important feature to be noticed during zero voltage state or free-wheeling stage is the isolation or disconnection between PV

source and the grid. The isolation between the PV source and the grid can be achieved by turning OFF all the switches of H-bridge inverter as shown in Fig. 2(c)

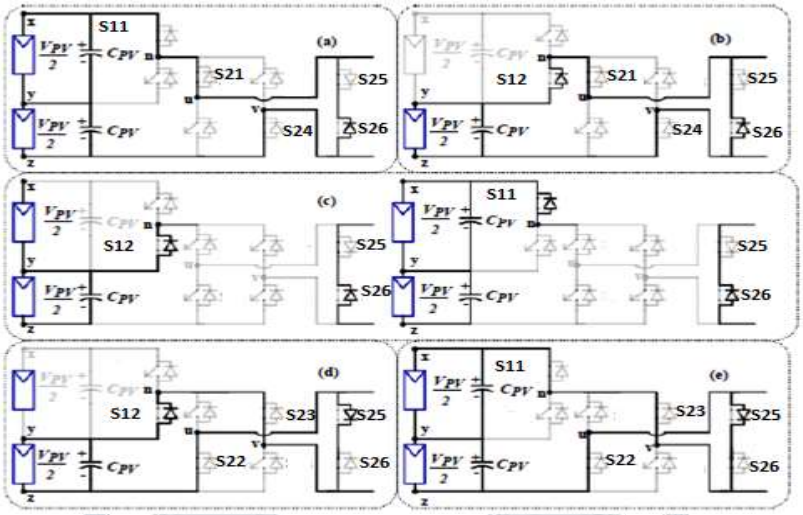


Fig: 2: Single Phase five-level cascaded MLI for output voltage levels (a) $+V_{pv}$ (b)$+V_{pv/2}$ (c) 0 (d)$-V_{pv/2}$ (e)$-V_{pv}$.

The turn-OFF state of four switches in H-bridge during zero voltage state results in the isolation of PV source from the grid. The bi-directional switches S_{25} and S_{26} provide a free-wheeling path for the inductor current during the turn-OFF period of a switching cycle. This action helps in minimizing the leakage current flowing through the parasitic capacitance. As there is no direct connection between the two sources, the PV terminal points (nodes x, y and z) float and have undefined voltages. The float or undefined value restricts the terminal voltages from becoming zero. Thus, high-frequency voltage transitions at the PV terminals are avoided.[1] In other words, the possibility of the flow of leakage current can be minimized. Also, in the other intermediate states like switching between $V_{PV/2}$ to V_{PV} or vice-versa, again the same principle can be used. The above action further helps in the minimization of the leakage current in the PV system. The PWM technique for the proposed five-level CMLI is broadly discussed. The expression for the pole voltages V_{uz} and V_{vz} are given in (1) and (2) respectively.

Table: 1: Switching states with their respective output voltage.

S_{11}	S_{12}	S_{21}	S_{22}	S_{23}	S_{24}	S_{25}	S_{26}	V_{uv}
1	0	1	0	0	1	1	0	$+V_{PV}$
0	1	1	0	0	1	1	0	$-V_{PV/2}$
0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	1	$-V_{PV/2}$
1	0	0	1	1	0	0	1	$-V_{PV}$

$$v_{uz} = \left(S_1 S_3 + 0.5 S_2 S_3 - \frac{1}{(S_3 + S_4)} + \frac{1}{(S_3 + S_4)(S_1 + S_2)} \right) V_{PV} \quad (1)$$

$$v_{vz} = \left(S_1 S_5 + 0.5 S_2 S_5 - \frac{1}{(S_5 + S_6)} + \frac{1}{(S_5 + S_6)(S_1 + S_2)} \right) V_{PV} \quad (2)$$

Where Sa, (a=1, 2, 3...) is the switching state of switch Sxa whose value can be either 1 (stands for turn-ON) or 0 (stands for turn-OFF) respectively.

Fig.3 shows the switching pattern of all the switches for the corresponding inverter output voltage *Vuv*. The switches S_{11} and S_{12} in the half-bridge are operated at low switching frequency[1]. In order to eliminate the high switching frequency operation, the switch S_{12} is kept turned ON in zero state during voltage transition between the levels *0* to $V_{PV/2}$. Similarly, the switch S_{11} is kept turned ON, during voltage transition between levels *0* to V_{PV}. The inverter switch pair (S_{21}, S_{24}) is operated with a high switching frequency during positive half-cycle, and it remains at the turn-OFF state during the negative half-cycle of the inverter output voltage V_{uv}.[1] A similar operation is applicable to the other inverter switch pair (S_{22}, S_{23}), which is operated with higher switching frequency during the negative half-cycle.

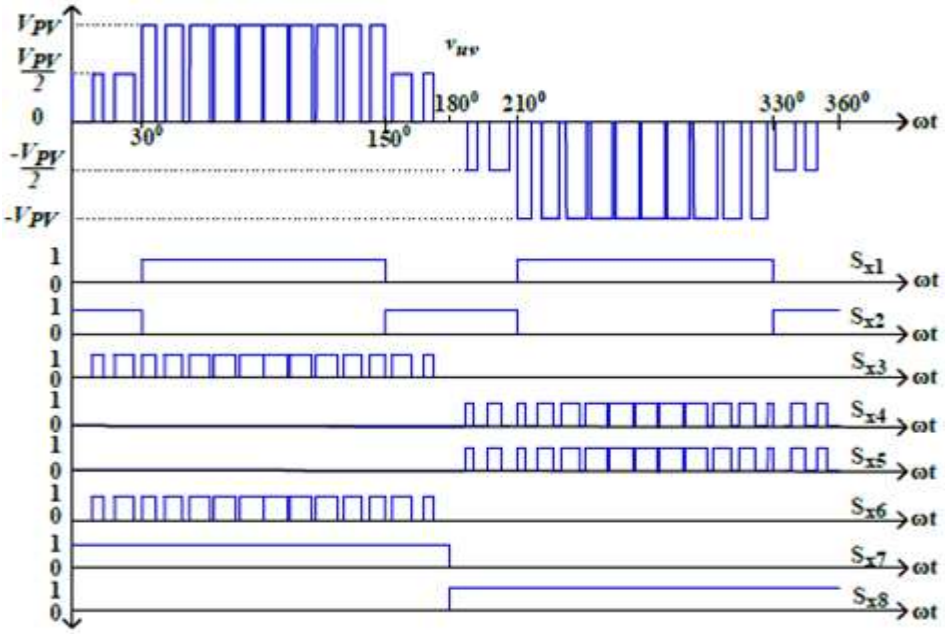


Fig: 3: Gate pulses for the switches corresponding to inverter output voltage.

The switches S_{25} and S_{26} are turned ON during positive and negative half cycles of the output voltage *Vuv* respectively. The removal of complementary action from the pair of switches (S_{21}, S_{22}) and (S_{23}, S_{24}) facilitates complete turn-OFF of the switches during each half-cycle of the output voltage V_{uv}.[1]Thus, the proposed system has the advantage of reduced switching losses, realizing to a highly efficient and reliable inverter configuration which may result in higher efficiency.

2.2 BLOCK DIAGRAM

The proposed system consists of solar panels connected to the 5 level Cascaded H – Bridge Multi level inverter. The output of 5-level CMLI is connected to the grid through an LCL filter.

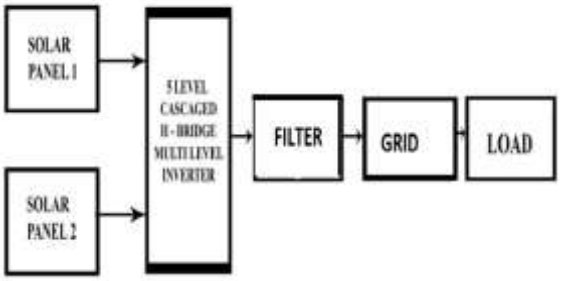


Fig 4 :Block Diagram of proposed system

III PULSE WIDTH MODULATION

3.1 Principle: Pulse width modulation (PWM) is a powerful technique for controlling analog circuits with a processor's digital outputs. PWM is employed in a wide variety of applications, ranging from measurement and communications to power control and conversion.

3.2 PWM Controllers

Many microcontrollers include on-chip PWM controllers. For example, Microchip's PIC16C67 includes two, each of which has a selectable on-time and period. The duty cycle is the ratio of the on-time to the period; the modulating frequency is the inverse of the period. To start PWM operation, the data sheet suggests the software should:

- Set the period in the on-chip timer/counter that provides the modulating square wave.
- Set the on-time in the PWM control register.
- Set the direction of the PWM output, which is one of the general-purpose I/O pins.
- Start the timer.Enable the PWM controller

3.3 Operation for PWM technique

The operation of the proposed PWM technique is explained by considering the given five-level CMLI. The high-frequency transitions in the terminal voltages V_{xg} and V_{yg} of five-level CMLI are minimized using the proposed PWM technique.

The suggested action can be achieved by switching from V_{PV} to *0* state or vice-versa instead of the switching from V_{PV} to $V_{PV/2}$ state or vice-versa. Additionally, during the zero voltage state or free-wheeling period of the switching cycle, the PV array is isolated from the grid. The isolation of the PV array and the grid during zero voltage state is similar to the inverter configuration reported in [5]. The magnitude of reference wave V_{mod} is lowered to 50% of its original value whenever the switching is toggled amongst the levels V_{PV} and *0*. The above action is mainly done to accommodate the value of PV voltage V_{PV}. The modification in the value of V_{mod} is done whenever the

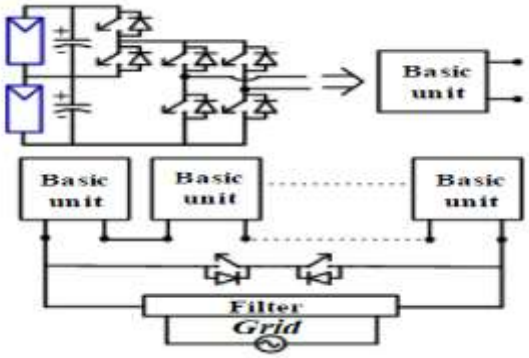


Fig: 5: Generalized 2m+1 level MLI topology derived from proposed five-level CMLI.

Instantaneous magnitude of modulating wave V_{mod} exceeds the value of *ma*/2, where *ma* refers to the modulation index. By incorporating the desired modification. The output voltage includes the zero voltage state (i.e., free-wheeling state) in all its switching periods.

IV. SIMULATION RESULTS

4.1 Simulation of proposed Modified 5-Level CMLI for PV system.

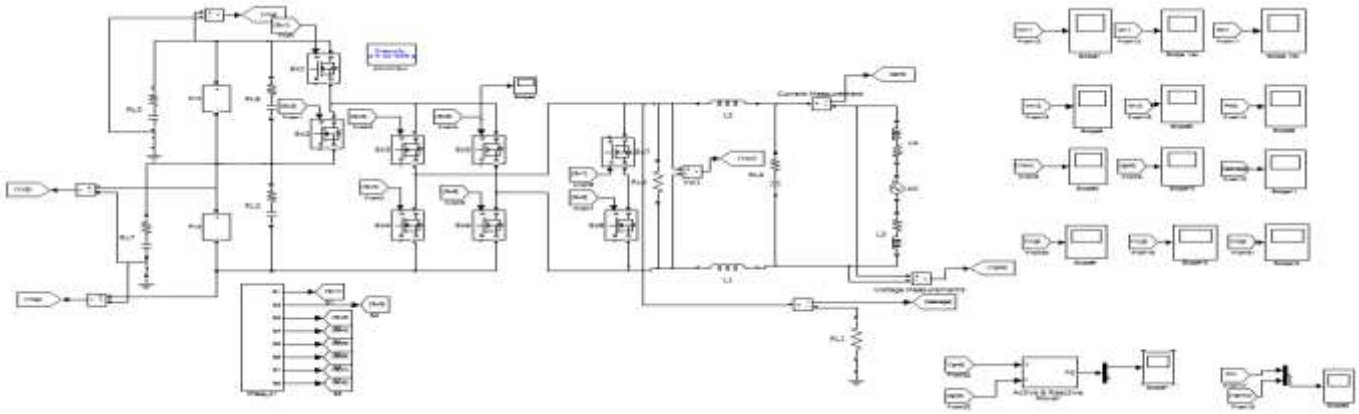


Fig 4.1. Simulation of proposed modified 5-level CMLI for PV system.

To support the switching function analysis given in the previous section, the proposed 5-level CMLI is simulated using MATLAB/Simulink software. Fig 4.1 shows the Simulink block diagram of modified 5-level CMLI for PV system. The proposed system consists of solar panels connected to the 5-level Cascaded Multilevel Inverter .The output of 5-level CMLI is connected to the grid through a LCL filter. It consists of 8 switches.

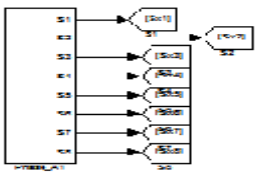


Fig:4.2 . Gate Pulses for the switches of proposed CMLI corresponding to inverter output voltage.

Fig 4.2 shows the gate pulses for the switches of proposed CMLI corresponding to inverter output voltage. The operation of an inverter, in all its switching states. The inverter output voltage V_{uv} at different voltage levels with the corresponding switching stage of all the switches.

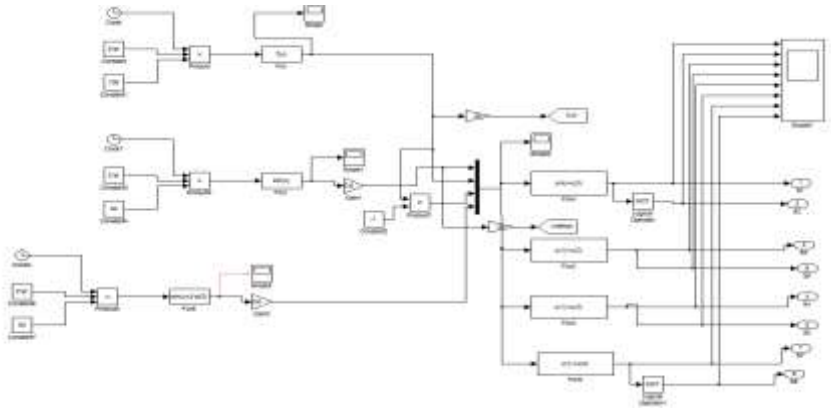


Fig:4.3 Gate Pulse simulink diagram.

Fig 4.4 Gate Pulse for the switches corresponding to inverter output voltages.

4.2 SIMULATION RESULTS

To support the switching function analysis, the proposed five-level CMLI is simulated using in MATLAB/SIMULINK software. The PWM technique explained in section 3 is used for the proposed five-level CMLI configuration. Table II gives the value of various parameters used for simulating the proposed five-level CMLI. The proposed five-level CMLI needs to generate a voltage *Vinv* having a phase *δinv* [6] to feed the required amount of active power *P* into the grid.

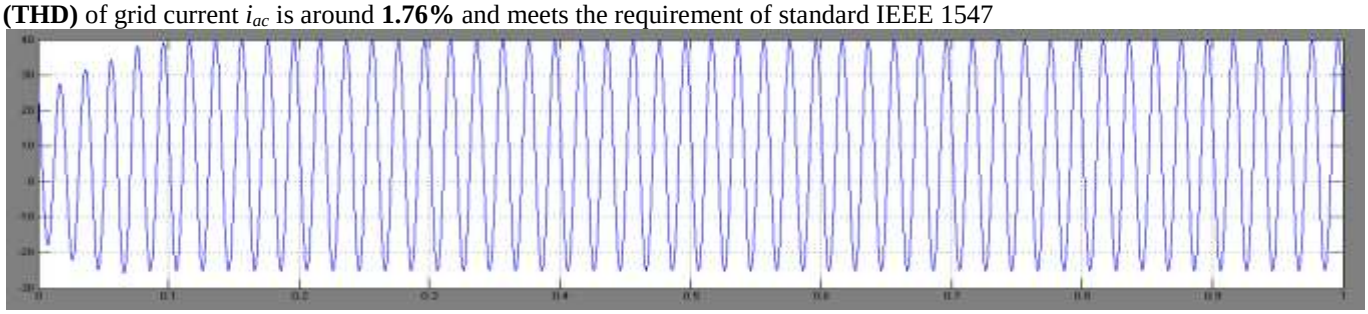
Table II

Parameter	P	V_{DC}	f_{sw}	v_{ac}	f_{ac}
Value	2.5kW	400V	25kHz	220V	50Hz
Parameter	L_{ac}	R_{ac}	R_g	L_i	C_f
Value	4mH	0.01Ω	0.1Ω	4mH	0.1 µF
Parameter	R_d	C_p	R_p		
Value	50mΩ	200nF	1Ω		

$$\delta_{inv} = \arctan\left(\frac{2\Pi f_{ac}(L_{ac}+L_f)P}{v_{ac}^2 + R_{ac}P}\right)$$

$$V_{inv} = \left(v_{ac} + \frac{R_{ac}P}{v_{ac}}\right)\frac{1}{\cos\delta_{inv}} \quad \textbf{(3)}$$

For a power of *P* =2.5kW, the value of *δinv* = 0.117 rad and *Vinv* = 323 V are calculated by substituting the parameters from Table II in (3) respectively. The simulation waveforms of proposed five-level CMLI using the proposed PWM technique are shown. The grid current i_{ac} is shown in Fig 4.5. Fig 4.5(a)The grid current is nearly sinusoidal. The Total Harmonic Distortion **(THD)** of grid current i_{ac} is around **1.76%** and meets the requirement of standard IEEE 1547



Time(sec)

Fig 4.5 : (a) Grid current i_{ac}.

The waveform of terminal voltages V_{xg},V_{yg} and V_{zg} are shown in subplots (b), (c) and (d) of Fig 4.5 respectively. The crucial observation made from these subplots is the absence of high-frequency voltage transitions.

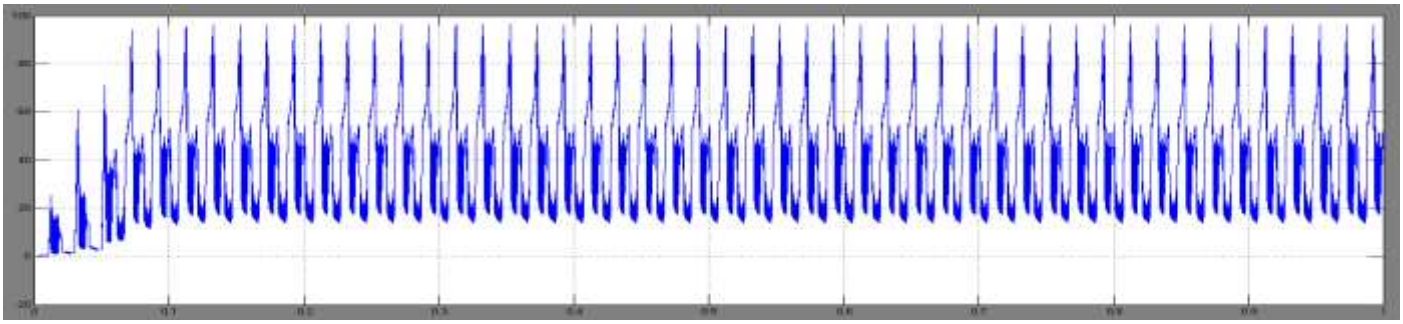


Fig 4.5 (b) Terminal voltage V_{xg}

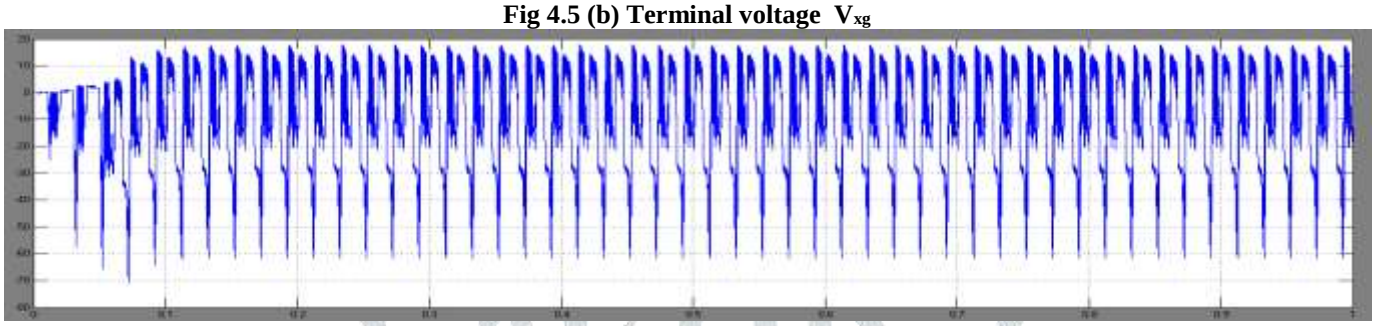


Fig 4.5(c) Terminal voltage V_{yg}

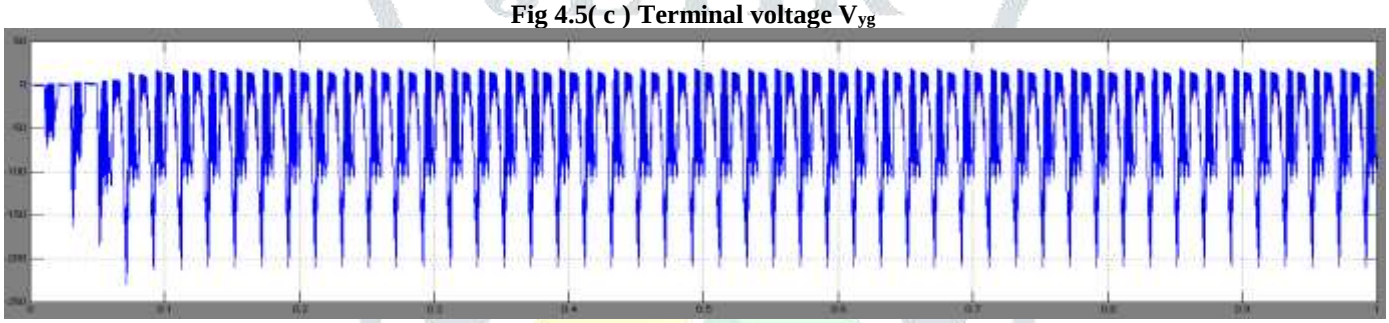


Fig 4.5(d) Terminal voltage V_{zg}

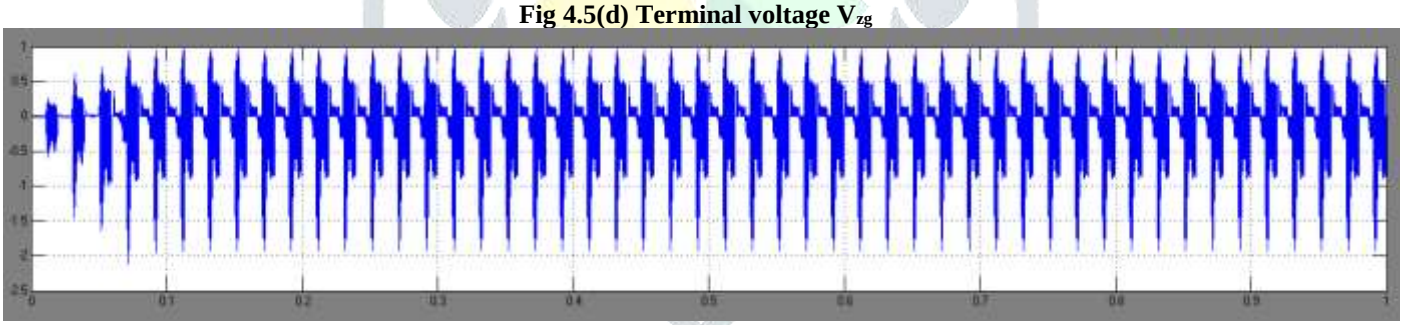


Fig 4.5(e) Leakage Current $i_{leak.}$

Fig 4.5 (e) shows the waveform for leakage current i_{leak} flowing through the parasitic capacitor. The proposed PWM technique reduces the value of leakage current as can be observed in fig 4.5 .(e). This is because of the low-frequency voltage transitions in the terminal voltages V_{xg}, V_{yg} and V_{zg}. The spikes in the leakage current are observed when there is a sudden voltage transition in the terminal voltage. The RMS value of i_{leak} is less than 20mA which is as per the standard VDE0126-1-1[9]

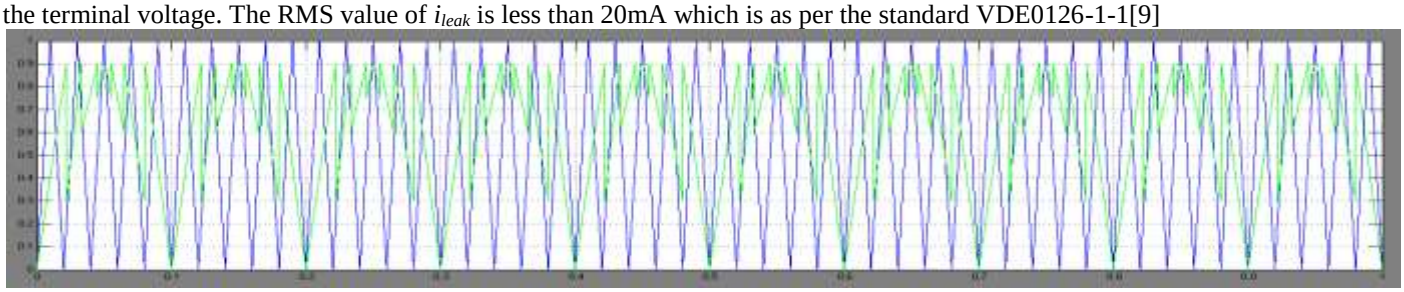
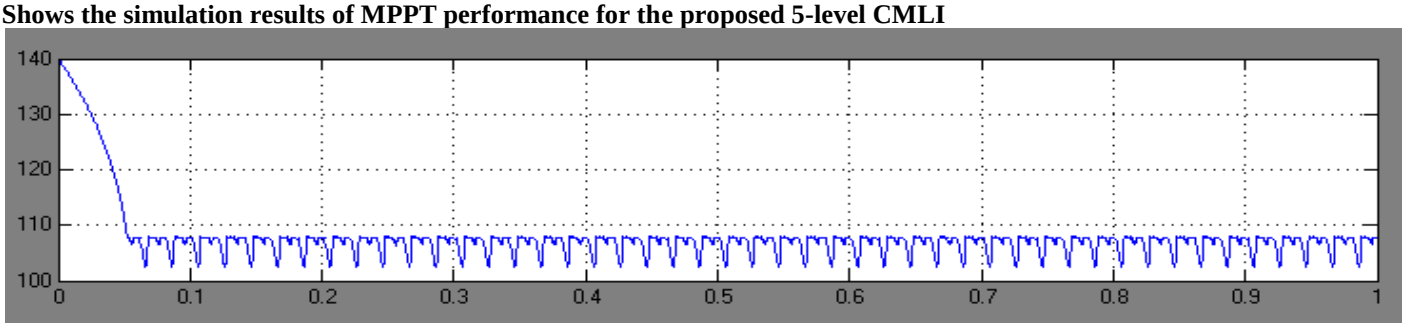


Fig 4.5 (f) common mode voltage V_{cm}

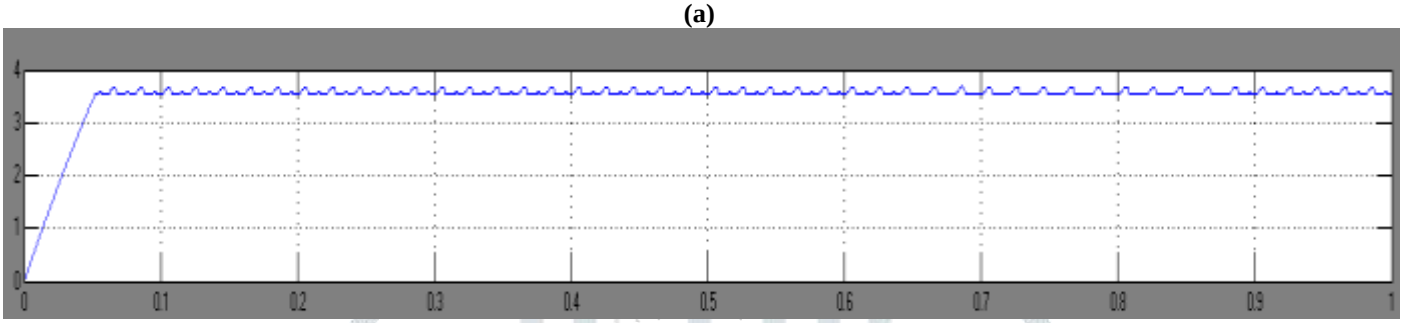
Fig 4.5. (f) shows the waveform of common-mode voltage V_{cm}. The high-frequency voltage transitions in the common-mode voltage are also avoided. This further brings down the size, weight and cost of the EMI filter to be used in the grid-connected system [10]

Shows the simulation results of MPPT performance for the proposed 5-level CMLI



Time(sec)

(a)

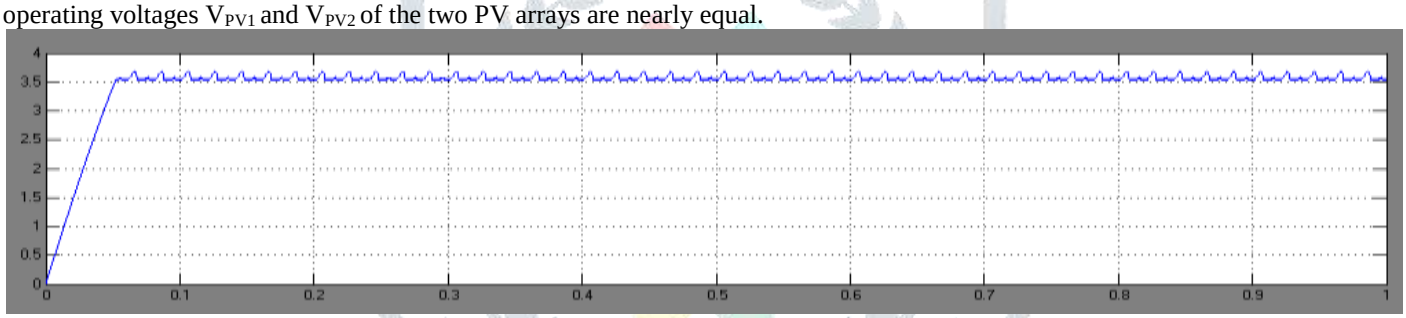


Time(sec)

(b)

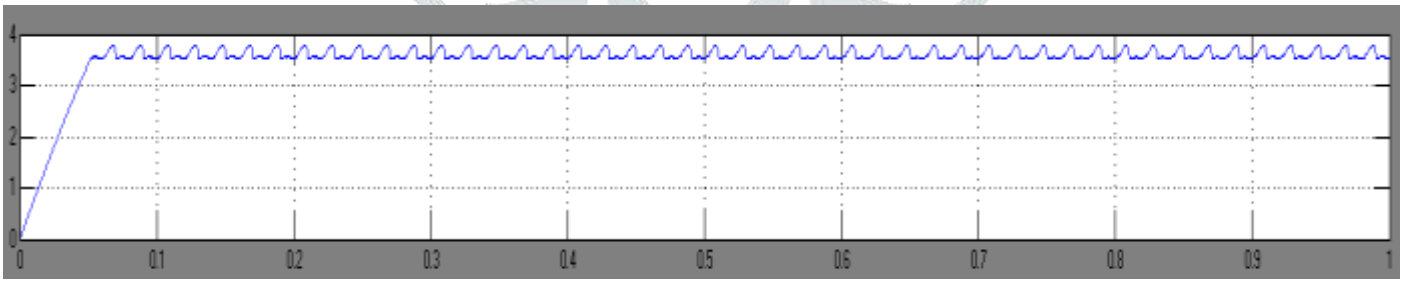
Fig 4.6(a)Voltage V_{PV1}, (b) Voltage V_{PV2}

Fig(4.6(a) and fig 4.6(b)) shows the simulation results of MPPT performance for the proposed five-level CMLI. The subplots (fig 4.6(a) and fig 4.6(b)) shows the waveforms of PV voltages V_{PV1} and V_{pv2} for P_{VI} and P_{V2} sources respectively. The values of the operating voltages V_{PV1} and V_{PV2} of the two PV arrays are nearly equal.



Time(sec)

(c)

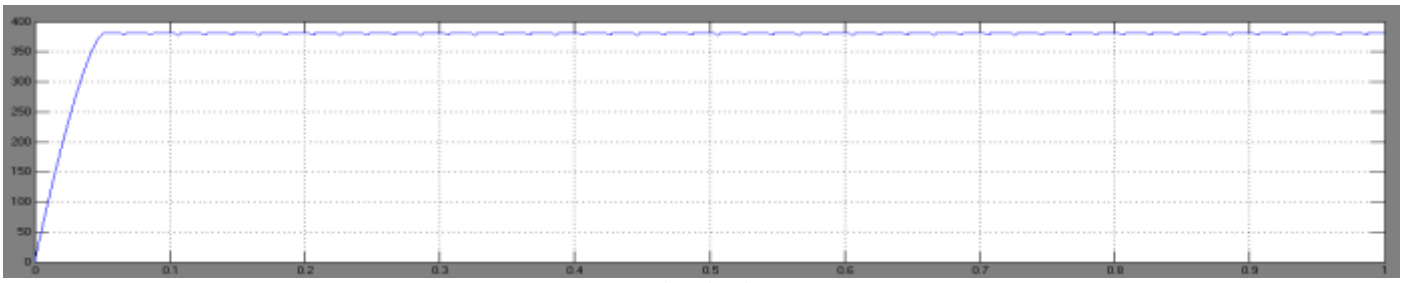


Time(sec)

(d)

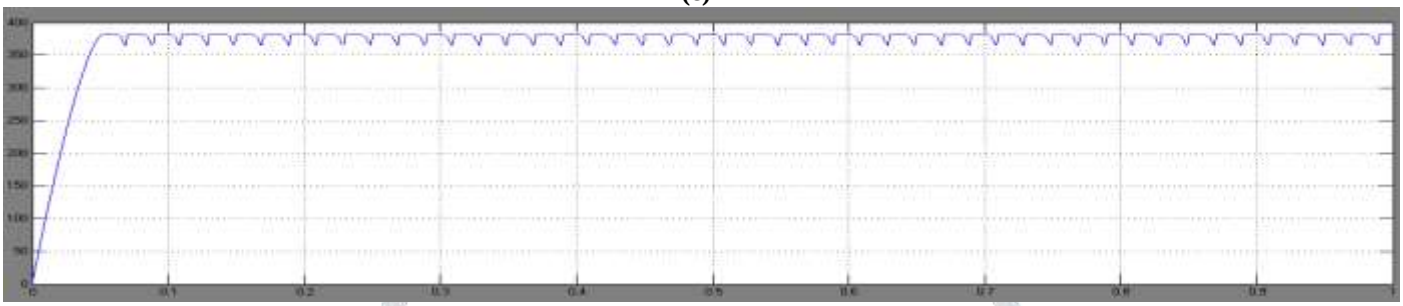
Fig 4.6(c) Current I_{PV1} (d) Current I_{PV2}

The subplot (fig 4.6(c) and fig 4.6(d)) shows the waveforms of PV current I_{pv1} and I_{pv2} respectively. The voltage current (v-i) characteristics of the PV array can be observed with the increasing value of current by decreasing voltage or vice-versa.



.Time(sec)

(e)



Time(sec)

(f)

Fig 4.6: (e) Power P_{PV1} (f) Power P_{PV2}.

The power P_{PV1} and P_{PV2} from the PV sources P_{V1} and P_{V2} are shown in subplots fig 4.6(e) and Fig. 4.6(f) respectively. The operation of two PV sources near MPP can be confirmed with the low value of ripple in the PV power and small oscillations in the modulation index *ma*, The waveform of output power across resistive load P_{load} is shown in subplot fig.4.6(g). It can be observed that the power across output load is nearly equal to the sum of the individual PV powers P_{PV1} and P_{PV2}. Integration of MPPT for the proposed five-level CMLI makes the inverter suitable for the PV systems.

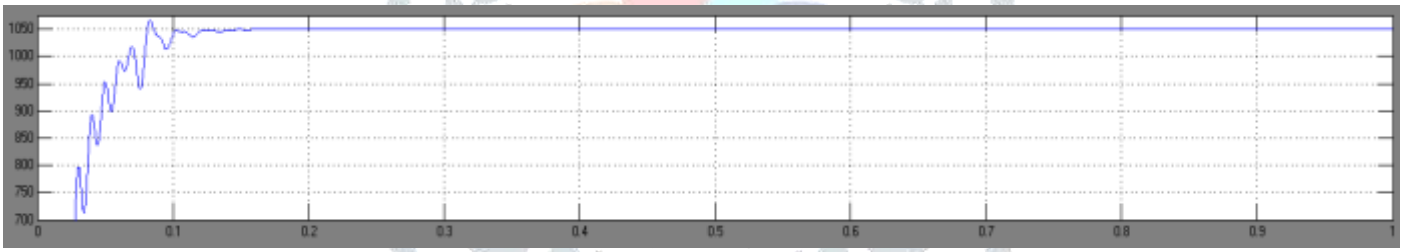
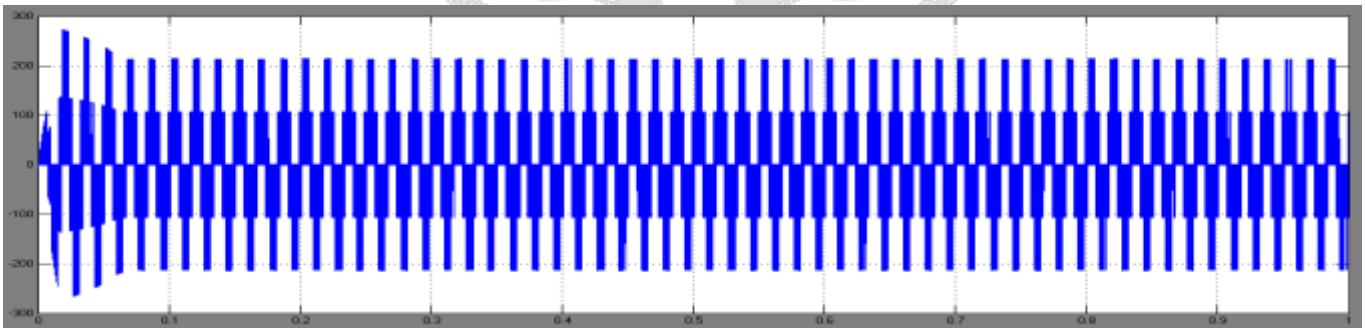


Fig 4.6 (g) output power P_{OUT}



Time(sec)

(h)

Fig 4.6: (h) output voltage V_{uv}

Fig 4.6(h) shows the output voltage of five-level CMLI. The presence of zero voltage state in all the voltage transitions of V_{uv} can be clearly noticed from the plot. The Integration of MPPT for the proposed five-level CMLI makes the inverter suitable for the PV system.

V.RESULTS AND DISCUSSION

The proposed five-level CMLI is operated using two MPPT algorithms to extract the maximum power from the individual PV arrays. The two individual MPPT algorithms are used for the two PV sources PV1 and PV2 which are identical (having same array configuration). Simulation is done considering a resistive load connected to the output of the inverter *via* an LC filter. The PV modules with an open circuit voltage of **21.05V** and short circuit current of **3.74A** at STC (Standard Test Conditions) are

chosen for the array simulation. The electrolytic capacitors of **5000μF** are used as a buffer between the PV sources and inverter as shown in Fig.1. The inverter is connected to a load of **20Ω** through an LC filter with the inductor and capacitor values of **4mH** and **2μF** respectively. The two PV arrays PV1 and PV2 have an open circuit voltage of **126.90V** and a short circuit current of **3.8A** at an insolation of 1.0 Sun and the temperature of **500C.** The improved Cascaded Multi-Level Inverter (CMLI) based on a highly efficient and reliable configuration for the minimization of the leakage current in a transformerless PV system. The proposed CMLI minimizes the leakage current by eliminating the high-frequency transitions in the terminal and common-mode voltages. The proposed topology also has reduced conduction and switching losses which makes it possible to operate the CMLI at high switching frequency. Furthermore, the solution for generalized *2m+1* levels CMLI is also presented in this paper. The given PWM technique requires only one carrier wave for the generation of *2m+1* levels. The operation, analysis of terminal and common-mode voltages for the CMLI is also presented. It can be observed that the power across output load is nearly equal to the sum of the individual PV powers P_{PV1} and $P_{PV2.}$

REFERENCES

[1]. Sachin Jain, Venu Jonti, "A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multi-Level Inverter for PV Systems", in IEEE transaction on Industrial Electronics.

[2] K. Corzine et al., "Control of Cascaded Multilevel Inverters," IEEE Transactions on Power Electronics, Institute of Electrical and Electronics Engineers (IEEE), May 2004

[3] Jose Rodriguez et al: "Multilevel Inverter: a survey of topologies controls and applications,'' IEEE Transaction on July 28, 2010.

[4] D.Grahame Holmes, Thomas A lipo " Pulse width modulation ," volume 18 of IEEE press series on power engineering.

[5] S. V. Araujo, P. Zacharias and R. Mallwitz, "Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems," *IEEE Trans. Ind. Elect*., vol. 57, no. 9, pp. 3118-3128, Sept. 2010

[6] O. Lopez, R. Teodorescu and J. D. Gandoy, "Multilevel transformerless topologies for single-phase grid-connected converters," APEC 2006, pp.5191-5196, Nov. 2006.

[7] O. Lopez, R. Teodorescu, F. Freijedo and J.D. Gandoy, "Leakage current evaluation of a single-phase Transformerless PV inverter connected to the grid," APEC 2007, pp.907-912, March 2007.

[8] O. Lopez, F.D. Freijedo, A.G. Yepes, P. F. Comesaa, J. Malvar, R. Teodorescu and J. D. Gandoy, "Eliminating Ground Current in a Transformerless Photovoltaic Application," *IEEE Trans. Energy Conv*., vol.25, no.1, pp.140-147, March 2010.

[9] G. Buticchi, D. Barater, E. Lorenzani, C. Concari and G. Franceschini, "A Nine-Level Grid-Connected Converter Topology for Single-Phase Transformerless PV Systems," *IEEE Trans. Ind. Elect*., vol.61, no.8, pp.3951-3960, Aug. 2014

[10] D. Barater, G. Buticchi, E. Lorenzani and C. Concari, "Active Common-Mode Filter for Ground Leakage Current Reduction in Grid-Connected PV Converters Operating With Arbitrary Power Factor," *IEEE Trans. Ind. Elect.*, vol.61, no.8, pp.3940-3950, Aug. 2014