DESIGN OF HIGH GAIN AND LARGE VOLTAGE SWING TWO STAGE MILLER COMPENSATED CMOS OPERATIONAL AMPLIFIER

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Abstract— A high Bandwidth Operational amplifier is required for many applications. So we need a study of operational Amplifier Bandwidth extension in such a way that other parameters are not affected. The two stage CMOS Op-Amp is exhibited in the paper that works at 1.8V supply voltage at 180nm technology and its input is relied on Bias current. Total power consumption of the circuit has been reduced by scaling down the supply voltage. The object of my research work is to decrease power dissipation, high gain and high swing. There is a back-and-forth amongst speed, power and gain at high supply voltages. Speed, power and gain determines the performance of any system. The op-amp has small stand-in power utilization, having large driving ability and works at small voltage in order that the circuit works at small power. This op-amp gives a gain of 70 dB, UGB of 53.01 MHz and phase margin of 27.83°. It has power consumption and CMRR of the operational amplifier are got as 523µW, and 73.33 dB respectively.

Keyword: Phase margin, CMOS Opamp, Low Power

1. Introduction:

An Op-Amp is one of the adaptable and essential constructing element in analog signal handling programs. An Op-Amp is excessive gain, DC coupled Voltage Amplifier having differential input and give either single or differential output for use and for accurately defining the close loop transfer characteristics it is used with negative feedback. A primary need of an Op-Amp is that it must have large open loop gain, large UGB, large input impedance, large speed and small output impedance. Such amplifiers are essential factors used in many analog subsystems, as like in switched Capacitor filters. It was seen that when analog circuits are designed using CMOS logic then it proved to be better than other logic designs of same generation because both analog and digital blocks can be implemented at same chip.

An Operational Amplifier are critical portions inside maximum analog circuits and structures. For getting high gain, just designing an amplification block is not sufficient but it also require right biasing circuitry together by efficient compensation method for getting stable operation. Fig 1 show an ordinary two level CMOS operational amplifier (op-amp). It comprises two purposeful elements. The first element suggests trans conductance stage which is the input of op-Amp accompanied by way of second stage. The second stage is formed by Common source supply Amplifier. Large Output swing and high DC gain is provided by second stage at given operating voltage and higher gain prompts bring down Bandwidth and therefore designer must determine among those tradeoffs primarily based at the specs and item prerequisites. Biasing circuit is there to build up the working point for the transistors in their quiescent level. There is a compensation circuit that gives balance to close loop performance. As Op-Amps are intended to function with terrible comments connection and therefore frequency compensation is important for stability. Right half plane (RHP) zero is introduced by feed forward path of miller capacitor which lower down the phase margin of circuit. But, we can eliminate the right half plane zero by usage of nulling resistor along with compensation capacitor.

An Op-Amps are used in lots of useful programs and in exceptionally large quantity of application and real performance of the amplifier is intently determined via the idealized amplifier version. Thus, in order to confirm acceptability of that approximation pretty frequency circuits are made. There are different situations in which idealization is certainly not the correct approximation yet it most likely as often as possible gives a begin line for an iterative way towards a last design. Think about the 741 amplifier, a more established anyway tried industry-in vogue device, that have a voltage gain surpassing 105 in customary activity. For making an output voltage to change among saturation voltage limit of

±15 volts, means we get output change of thirty-volt. Thus less than 0.3 millivolt change will be there in input voltage. Such a little voltage distinction might be dismissed i.e. considered as 0, as in comparison to different circuit voltages by which it is related in KVL loop equation [7-9].

The simple idea of op-amp is examined in the segment. We can say that an amplifier having overall attributes of high voltage gain, large input resistance, also extremely small output resistance is called as an Op-Amp. Op-Amp is used in many analog applications which has some quantity of negative feedback. Negative feedback is utilized to tell the Op-Amp how a mess to extend a signal. Furthermore, Op-Amp are significantly use to enforce the feedback system, specified accuracy of close loop system decides open loop gain of circuit[10].

An Op-Amp has 4 important elements

a. Current Mirror

b. Differential Amplifier
c. Level shift, differential to single ended gain stage
d. Output buffer

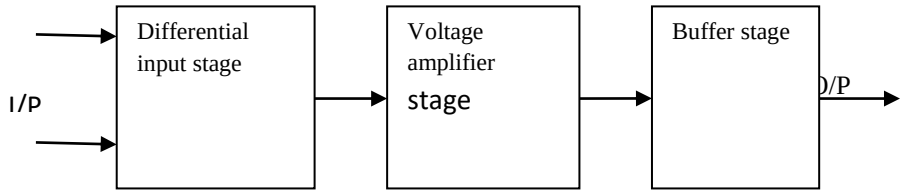

Fig 1. Typical two-stage design of op-amp

2. Related Work:

D. Nageshwarrao, 2013[8] The work affords design of two-stage operational amplifier that shows a Unity Gain Bandwidth(UGB) of 20 MHz and has gain of 42 dB with phase margin of 50 degree. New method are proposed to get high gain and phase margin. Result of simulation gives a gain of 48 db. Unity Gain frequency of 40MHz and phase margin of 89 degree. Cadence tool is used to accomplish the design. 180 nm technology is used to design the system. It used power supply of 3.5 volt. There is improvement in gain and phase margin in new design. In the new simulated result it gives a gain of 48db , unity gain frequency of 40 MHz , gain margin of 46db and 89.8 degree of phase margin is obtained.

Ketan J. Raut, 2014[9] provided the layout of 2-level operational amplifier (Op Amp).180nm virtual n-well CMOS strategy is used to design the circuit. The layout is much improved as the plan incorporates lesser number of transistors. Open loop gain of amplifier is accomplished as 74.89 db. It has unity gain bandwidth (UGB) as 7.3MHz and obtain phase margin of 43 degree. It uses 10 pf capacitor and resistive load of 1M ohm. It has power utilization of 0.402mW and has slew rate of 10V/us is obtained. We get slew rate as 10 V/us. Hence it can be taken into consideration as Op-Amp having moderate speed.

.**Shilpa Goyal, 2015[10]** In the work, Miller compensation approach has been used in design of two level CMOS operational amplifier that works at 2.5V. Here simulation is done by employing TSMC 180nm CMOS method and tanner EDA tool is used for making the design. By using SCMC technique two stage CMOS Op-Amp which is designed offers gain of 57.18db with phase margin of 56 degree. In second method, SCMC alongwith Nulling resistor is used in two stage CMOS Op-Amp design which causes increase in phase margin and in a roundabout way makes system more stable. By using nulling resistor in series with miller compensation capacitor it provide gain of 48.27 db and also gives phase margin of 86.48db.

Sayan bandyopadhyay, 2014[11] afforded a layout and he design the 2-stage of CMOS Op-Amp operating at 2.5V supply voltage and Tanner EDA Tool Cadence virtuoso is employed to do the simulation at 180 nm technology. We get the gain of 36.747db along with phase Margin of 48.1. It has power utilization of 0.804mW. The Simulation has been finished at 180 nm technology by use of cadence tool. By improving the parameter such as (W/L) gain has improved. Design equation were formed and by carefully choosing and sizing the shape of circuit. In the work we get gain of 36.747db along with phase margin of 48.1 and also the power utilization of circuit is 804uW.

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Goyal, 2015[12] This two-stage op-Amp which is presented in the paper provide open loop gain of 78db. It has GBW of 5.82MHz and phase margin of 63.9degree. The 180 nm technology is used for design. Supply voltage of 3.3 volt is used, having power dissipation of 144.3uW. Eldo (Mentor Graphics) is used for design and simulation of op-Amp and 180 nm technology is used. An operational Amplifier has dc gain of 78.21db, phase margin of 63.97 degree and unity gain bandwidth of 5.82 MHz. It has power utilization, PSRR and CMRR for the operational Amplifier is 143.3uW,117.73db, 89.05db respectively.

Klaas Bult,1990[7] presented a method in which he combines the excessive dc gain of the multistage design with a high frequency conduct of the uncoupled stage operational amplifier. It gives a gain of 90db and unity gain bandwidth of 116MHz by its measurement of Bode plot. The quick uncoupled –pole settling nature together with closed loop bandwidth of 18MHz and the settling accuracy better than 0.03% is shown by settling measurements having the feedback element. An output swing of about 4.2V can be obtained with supply voltage of 5V without any loss in dc gain. There was an increase of 30% in area of chip and increase of 15% in power intake.

Rajkumar S. Parihar,2006[15] The level fully differential, RC Miller compensated CMOS operational amplifier has been designed and implemented by him. It has high gain which permits the circuit to perform properly in the closed loop feedback device. It also has high bandwidth which permits its for large speed applications. The design is capable of handling the fluctuations in dc input or supply voltages and by the neglecting the effects due to perturbation it can provide stability. 180nm technology is used for implementation and equipments such as Mentor Graphics and cadence were used. The design of operational amplifier gives a dc gain of >95db, unity gain bandwidth of 135, phase margin of 53degree and slew rate of 132V/us for differential capacitive load of 1pf. A power dissipation below different nominal conditions is 2.29mW at supply voltage of

3.3V at temperature of 27degree Celsius. Some of extra characteristics of layout is best output differential swing of 5.9V and suitable linear variety of operation.

Hassan Sarbishaei,2005[16] offered a high gain, high speed, low power magnificence AB operational amplifier. To reinforce DC gain positive feedback gain enhancement method was used. For good Slew rate with low power Class AB approach was hired. For overcoming the swing problem, CDB technique was used to loading the transistor and thus decrease threshold voltage. Also a proposed operational amplifier may be used as the first level of the degree operational amplifier having rail to rail output swing like minded for excessive speed low power programs.

Neha Arora,2013[17] provided the designs of large gain and phase margin and low power CMOS operational amplifier in 200nm technology, by considering the fact that it's miles an essential constructing element in analog IC. In the work up to third order operational amplifier was supplied inclusive of designing the fully differential folded cascade arrangement having all of transistors are working in the saturation in all the configurations. These design are achieved in parallel primarily depending on better model of operational amplifier and simulation of the circuit in spice using Hspice model parameters. Optimization of most of the transistors parameter have been done to reap the good working of operational amplifier in 200nm technology. Results of simulation of spice agrees with the consequences of calculated parameters of the amplifier.

Ankit Sharma,2012[18] represented an advance layout of 2 level CMOS operational amplifier comparator which have ultra small power utilization that is useful in many small energy applications including many bio-medical packages. This proposed design is the changed layout of two level open loop comparator. A Cascade form of an op-amp have been designed. Simulation and analysis have acquired in 0.35 um CMOS TSMC technology on the tanner V7 EDA device having 3.3V of power supply having input voltage of 1V and ICMR of 0.4-3V. Comparator well-known shows a large resolution of 13-bit and ultra small power intake of 53uW at frequency of 100kHz with 0.4V of reference voltage. The propose comparator provides gain of 80db, UGB of 10MHz and PM of 49degree. A temperature of 27 degree was taken for making all the observations

3. Methodology:

We must discuss some relationships which are important for analyzing the performance of op-Amp before starting the design portion.

Slew rate,

$$S_R = \frac{I_5}{C_c} \quad (1)$$

First-stage gain,

$$A_{v1} = \frac{-g_{m1}}{g_{ds2}+g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2+\lambda_4)} \quad (2)$$

Second-stage gain,

$$A_{v2} = \frac{-g_{m6}}{g_{ds6}+g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6+\lambda_7)} \quad (3)$$

Gain bandwidth,

$$GB = \frac{g_{m1}}{C_c} \quad (4)$$

Output pole,

$$p_2 = \frac{-g_{m1}}{C_L} \quad (5)$$

RHP zero,

$$z_1 = \frac{g_{m6}}{C_c} \quad (6)$$

Positive CMR,

$$V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - [\, V_{T3(max)} + V_{T1(min)} \,] \quad (7)$$

Negative CMR,

$$V_{in(min)} = V_{SS} - \sqrt{\frac{I_5}{\beta_1}} + V_{T1(max)} + V_{DS5(sat)} \quad (8)$$

Saturation voltage,

$$V_{DS(sat)} = \sqrt{\frac{2I_{DS}}{\beta}} \quad (9)$$

It is considered that all the transistors that are shown in figure 2 are operating in saturation region for the above shown relations and also

$g_{m1} = g_{m2} = g_{mI}$,

$g_{m6} = g_{mII}$,

$g_{ds2} + g_{ds4} = G_I$ and $g_{ds6} + g_{ds7} = G_{II}$ (10)

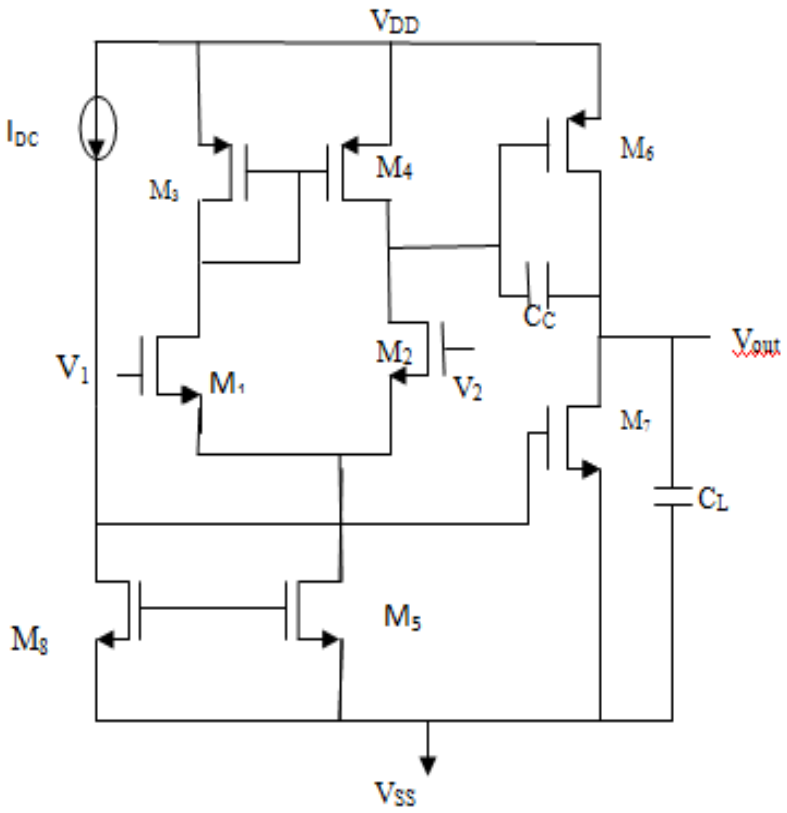

Fig2: Two stage Op-Amp

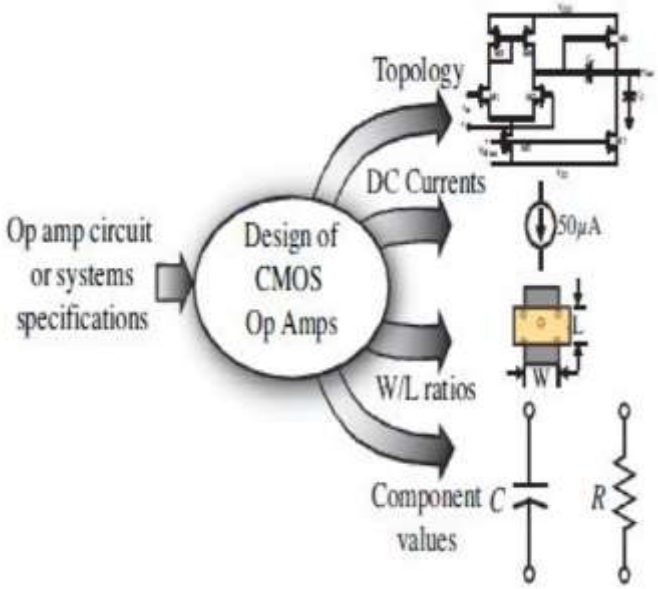

Figure 3: Design procedure of Op-Amp[8]

In the design [8], following sequence of steps are there. Firstly, the specific topology is selected. Secondly, values of DC currents are determined. Thirdly, We have to calculate the W/L ratios of transistors used. At the end, we have to find the values of passive elements present in circuit. Figure3 is drawn for classifying these things. A design process consider to the DC gain(A_v), unity-gain bandwidth (GB), Input common-mode range[$V_{in(min)}$ and $V_{in(max)}$], Load capacitance(C_L), slew rate(S_R), Settling Time(T_s), Output voltage swing [$V_{out(max)}$ and $V_{out(min)}$] and Power utillization(P_{diss}) are specified.

1. Length of device must be small enough to provide value of modulation parameter to be constant and must provide better current mirror matching .
2. From the desired phase margin, the minimum value for C_c is chosen ,that is for a 600 phase margin. We have used the following relationship. This assumes that z 10GB. $C_c > 0.22\ C_L$
3. The biggest of the two values is the least value for tail current $I_5 = S_R.C_C$

I_5 nearly equal to $\frac{10(V_{DD}+|V_{SS}|)}{2T_S}$

4. S3 is determined from the value of maximum input voltage

$$S_3 = \frac{2l_3}{K_3^1 V_{DD} - V_{in(max)} - [V_{T3(max)} + V_{T1(min)}]^2} > 1$$

5. We will not get dominant pole and zero by C_{gs3} and C_{gs4} (=0.67W_3L_3 C_{ox}) and let us assume pole p3 to be greater than 10GB.

$$\frac{g_{m3}}{2C_{gs3}} > 10GB$$

6. Design for S1(S2) to achieve desired GB.

$$g_{m1} = GB.C_c \geq S_1 = S_2 = \frac{g_{m2}}{K_2^1 I_5}$$

7. Design for M_5 from the minimum input voltage. First we have calculated $V_{DS5(sat)}$ and then we have find W/L of M_5.

$$V_{Ds5(sat)} = V_{in(min)} - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{1/2} - V_{TI(max)} \geq 100mV$$

$$(W/L)_5 = \frac{2I_5}{K_5^1 [V_{DD(sat)}]^2}$$

8. For W/L ratio of M_6 and value of I_6

.For 60 degree phase margin, $g_{m6} \geq 10g_{m1}$.

And $g_{m4} = [K_4^1(W/L)_4 2I_{d4})]^{1/2`}$

$\frac{(\frac{W}{L})6}{(\frac{W}{L})4} = \frac{I6}{I4} = \frac{gm6}{gm4}$

9. For W/L of M_7,

$\frac{I7}{I5} = \frac{(\frac{W}{L})7}{(\frac{W}{L})5}$

10. Check gain and power dissipation specifications.
11.By simulating the circuit we have seen that all the specifications are met.

4. Result and Discussion:

A power supply of 1.8 volt is used to operate the operational amplifier. Biasing circuit is used to provide proper biasing voltages to the op-Amp circuit. By using miller compensation technique in 180 nm technology design and simulation of op-Amp is done. And the power consumption of the circuit is 523 uW. Fig 4 shows the Op-Amp Schematic and Table 1 shows the Specification of Two Stage op-Amp Design.

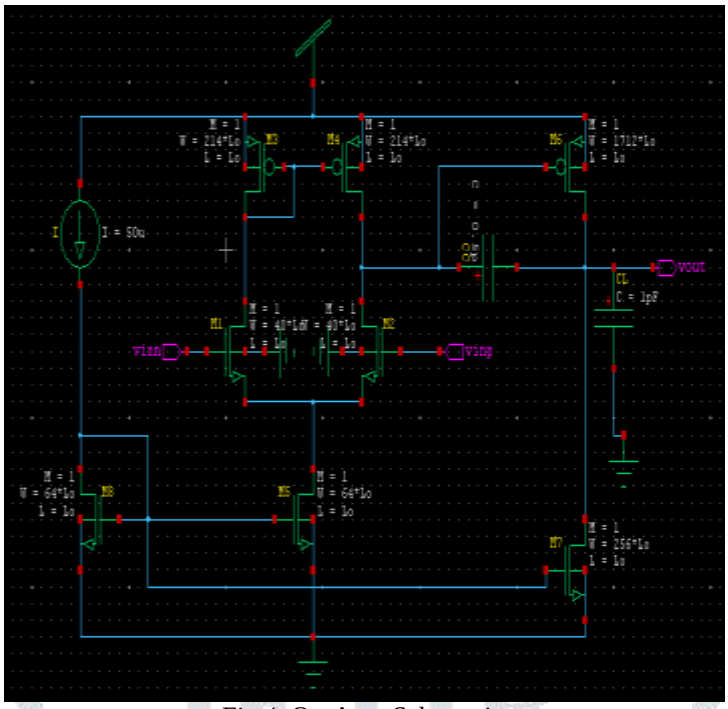

Fig.4 Op-Amp Schematic

Table 1: Specification of Two Stage op-Amp Design

Specification name	Value(Base Paper)[11]	Value
Supply Voltage	2.5V	1.8V
Bias Current	60uA	50uA
Compensation Capacitor	3pF	0.5pF
Load Capacitor	10pF	1pF

4.1 Simulation Results

This design provided a gain of 70.23dB with a common mode rejection ratio of 73.33 dB. Slew Rate is 46.97V/us. Unity gain bandwidth obtained was 53.01 MHz. The phase margin came out to be 27.83 degree making design relatively stable. The Common Mode Rejection Ratio is 73.33 dB.

4.1.1 AC Response

In Fig. 4.2, a process to measure the AC response is shown

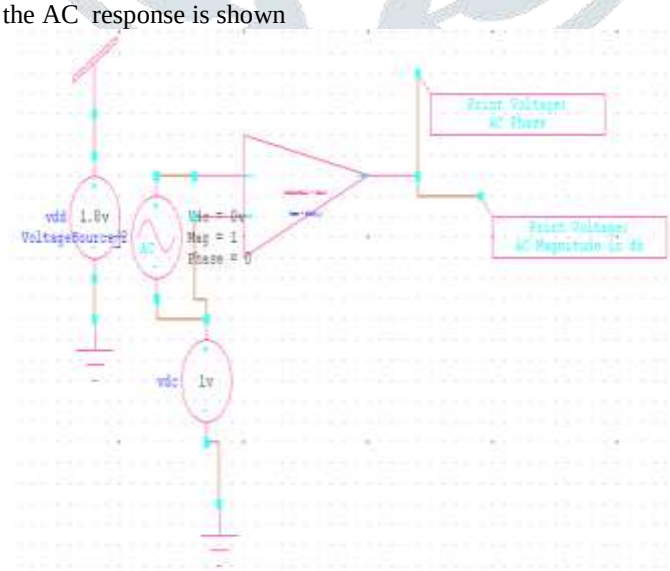

Fig 5: Arrangement used for simulating the open loop frequency response of an op amp

In the arrangement, an amplifier is in open loop condition, and at the input we have applied the AC signal. In Fig 6, a Bode and phase plot is shown.

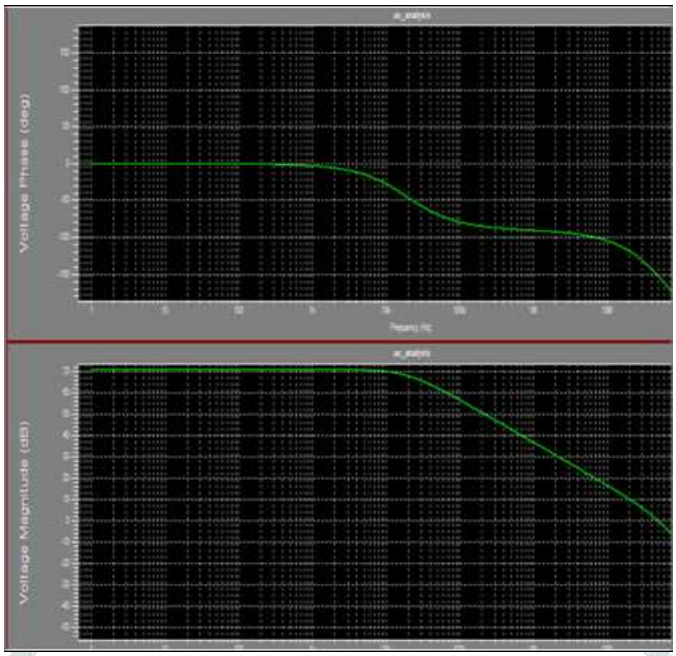

Fig 6. Frequency response of op amp.

By sinusoidal signal at the input, the transient simulation of amplifier in open loop gain configuration is there.

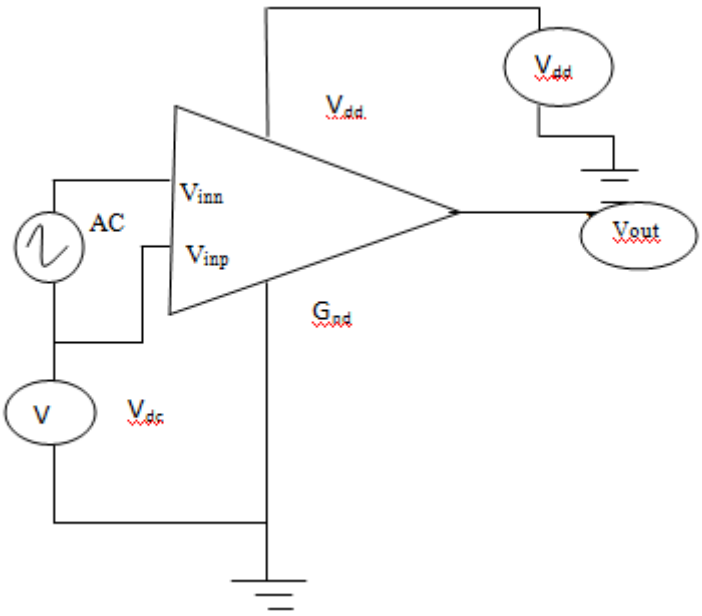

Fig 7. Arrangement for the transient response simulation

4.1.2 Slew Rate:

In Fig. 8, At the input , a step voltage is applid from ground to Vdd and in unity feedback configuration. And measure value of amplifier Slew rate is 46.97V/us. As shown in figure 9.

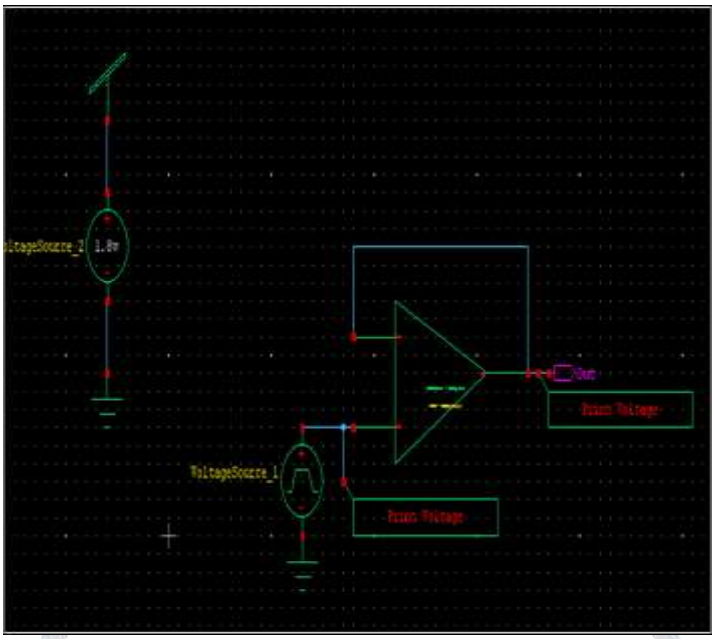

Fig 8: Arrangement for the measurement and analysis of slew rate.

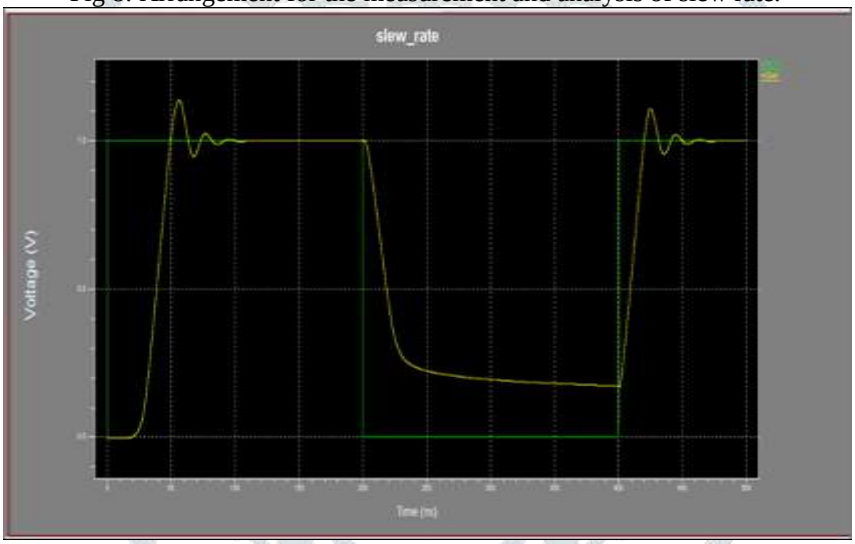

Fig. 9: Slew Rate for the rising and falling edge with unity gain configuration.

Table 2: Simulation Results of Op Amp

Parameter name	**Parameter Value (Base paper)[11]**	**Values at 0.6V**	**Values at 1.6V**
Power	804uW	**523uW**	583uW
GBW	16.54 MHz	47.58MHz	**53.01MHz**
Gain	36.747db	**70.37db**	70.23dB
Slew Rate	12.5V/us	46.97V/us	**46.97V/us**
Phase Margin	48.1 degree	**27.83 degree**	25.67 degree
CMRR	133.69dB	72.86dB	**73.33dB**

Table 2 provides op-Amp parameters values as like Power, GBW, Gain, slew rate, Phase Margin, and CMRR are in found to be better along with target specifications. Here best result is shown in bold.

5. Conclusion:

In the paper an operational Amplifier is designed with high gain and large swing. Compensation Capacitor has an prominent role in design of operational Amplifier for power utilization and also for noise parameter. Current buffer technique is less sensitive to parameters variations so this technique is used when there is decrease of power consumption with value of compensation capacitor. Tanner EDA tool in 180nm process technology is used for design and simulation of operational amplifier. The proposed operational Amplifier has dc gain of 70.37db, unity gain Bandwidth of 53.01MHz, phase margin of 27.83degree. It has the power utilization and CMRR are gotten as 523µW, and 73.33 dB respectively.

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