Highly Linear Active Feedback Noise Cancelling Wideband Low Noise Amplifier for Next Generation RF Frontend using 0.18µm CMOS

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Abstract — Next generation wireless terminal should support multiple standards (UMTS, WiMAX, LTE, IEEE 802.11a/b/g, Zig-Bee, Bluetooth etc.), receive multiple frequency bands, and allow any modulation scheme. So, Next generation RF (Radio Frequency) Frontend requires wideband with multiple standards support. RF Frontend relaxes tough requirements (dynamic range, speed, noise performance and linearity) of Baseband A/D converter. An LNA (Low Noise Amplifier) of RF Frontend relaxes the noise performance and dynamic range requirements by amplifying weak received signal with adding minimum noise to improve signal to noise ratio.
This paper we have design and simulate 2-7Ghz wideband Low Noise amplifier for next generation RF frontend receiver using 0.18µm CMOS technology. The proposed technique exploits the complementary characteristics of NMOS and PMOS to improve the linearity performance. A two-stage Wideband LNA is optimized to achieve high linearity with high gain and low NF over the 2-7 GHz range. The first stage espouse inverter topology with resistive and common drain active feedback to provide high linearity, wideband input matching and noise cancelling, whereas the second stage is a cascode amplifier with series and shunt inductive peaking techniques to extend the bandwidth and achieve high gain simultaneously. The proposed Wideband LNA demonstrate a gain of 12.7-15.6 dB within the entire band, a noise figure of 2-4 dB, and an IIP3 is greater than 8dBm in entire band and 17dBm maximum at 5GHz while consuming 20 mw from a 1.8 V power supply. The simulated input return loss is below −8 dB, and the output return loss is −8 dB, from 2-7 GHz. Its shows that the design achieve comparable good performance compare to published work in wideband LNA.

Keywords-CMOS; Low Noise Amplifier; RF frontend; Wideband

I. INTRODUCTION

Today's wireless mobile terminal should support multiple communication standards like: GSM, UMTS, WiMAX, LTE, ZigBee, Bluetooth, IEEE 802.11a/b/g etc; operated on difference frequency band and different modulation scheme [1]. This mobile terminal is termed as commercial Software Defined Radio(SDR), as proposed by Mitiola [2].

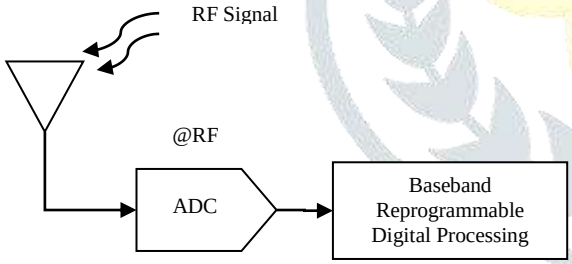

Figure 1. Ideal SDR Receiver.

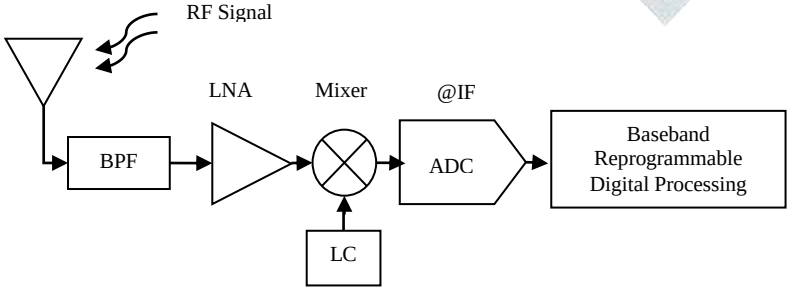

Figure 2. Practical SDR receiver.

The ideal SDR architecture proposed by Mitiola (Figure 1) puts very tough requirements on the dynamic range, speed, noise performance and linearity of A/D converter. A practical SDR architecture as shown in figure 2. An LNA relaxes the noise performance and dynamic range requirements while the mixer block reduces the speed requirements of the A/D converter by converting RF signal to IF signal. That is why Low Noise amplifier is essential part in wideband RF Frontend design.

The linearity parameters of the LNA will become more stringent if these filter specifications are relaxed. This clearly shows that the implementation of a receiver chain without an LNA is practically impossible. In a receiver, the first amplifying block is LNA. Its noise performance defines the NF of complete receiver. A classical narrowband LNA to achieve high gain, low NF, good linearity, low power, 50 Ω matching and stability at the frequency of interest is easy but to achieve same specification wideband is challenging task. To accommodate different standards with different modulation scheme require specification of wideband LNA are:

- Minimum signal reflection by achieving good (50 Ω) input matching (S11≤−15dB) for all frequencies [6].
- NF≤3.5 dB over the entire bandwidth [7].
- Higher linearity (IIP3≥0 dBm) [8].
- Flat gain across the entire bandwidth.
- Unconditional stability over entire frequency range.

Numerous wireless communication standards have been developed with close frequency spacing. High linearity plays the most important role in receiver design because of gain compression and interference from the existing standards. The main source of nonlinearity in a LNA is the nonlinear transconductance gm due to the nonlinear Ids −Vgs relation. In particular, the most important component for linearity is the third-order derivative of the DC transfer characteristic, which changes from positive to negative in the moderate inversion region [50]. Many techniques have been adopted to achieve a high-linearity amplifier. Optimum gate biasing is used to bias the transistor at the zero-crossing point [51]. The major drawback of this technique is that biasing in the moderate inversion region degrades NF and reduces the gain. The feed-forward technique is also applied to achieve high linearity [52–54]. This technique requires highly accurate scaling between the input signals of the main and auxiliary gain stages. Derivative superposition (DS) is the most popular method for achieving high linearity [55]. It uses two transistors connected in parallel; the main transistor is biased in the strong inversion region, whereas the auxiliary transistor is in the weak inversion region. The nonlinearity of the auxiliary transistor cancels the nonlinearity of the main transistor, but this technique is sensitive to process, voltage and temperature (PVT) variations, and it is difficult to align the positive and negative peaks. Also, the feedback of the second-order component through Cgd degrades the third-order intercept point. The modified derivative superposition issues the feedback of the second-order nonlinearity to the IM3 components [56].

The complementary CMOS push–pull technique and multiple gate configurations are used in this paper to improve the IIP2 and the IIP3 intermodulation. The complementary characteristic of NMOS and PMOS transistors is used to enhance the linearity of the proposed UWB LNA circuit [57]. Also, the shunt and series peaking inductance are used to extend the performance for an ultra-wideband system. The proposed UWB LNA technique preserves low noise, high gain, and wideband input matching.

Most linearization techniques are used to improve third-order nonlinearity (g3), but they hurt the second-order nonlinearity (g2) at the same time, which limits improvement in the IIP3, especially at high frequencies. However, in the proposed technique, high linearity is achieved by cancellation of g3 and a slight cancellation of g2, which relaxes and reduces the IIP2 problem.

This paper is organized as follows. Section 2 analyzes CMOS inverter technique. Section 3 describes the proposed Wideband LNA circuit design. The implementation and simulation results are provided in Section 4. Finally, the conclusion and references are presented in Section 5 and section 6 respectively.

II. CMOS INVERTER LINEARITY TECHNIQUE

Fig. 3 shows the CMOS Inverter configuration amplifier. It consists of two transistors NMOS and PMOS. The signal is input from the tied gate of NMOS and PMOS and the output is taken from drain of both transistor. The drain current of both transistors can be expressed as follows:

$$i_{dsn} = g_{1A}V_{gs} + g_{2A}V_{gs}^2 + g_{3A}V_{gs}^3 + \cdots$$
$$i_{dsp} = -g_{1B}V_{gs} + g_{2B}V_{gs}^2 - g_{3B}V_{gs}^3 + \cdots$$
$$i_{out} = i_{dsn} - i_{dsp} = (g_{1A} + g_{1B})V_{gs} + (g_{2A} - g_{2B})V_{gs}^2 + (g_{3A} + g_{3B})V_{gs}^3$$

where g_1, g_2 and g_3 are the main transconductance, second-order and third-order nonlinearity coefficients respectively. The second order nonlinearity is cancel in output due out off phase signal by NMOS and PMOS. The optimum biasing is used to obtain a high IIP3 by reducing the total g3, the IIP3 can be calculate as follows:

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|}$$

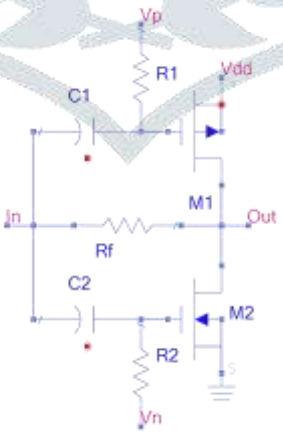

Figure 3. Complementary DS with common source configuration.

With a simple analysis, this configuration employs two PMOS and NMOS gain devices to boost the overall transconductance, leading to high g. With the proposed technique, reducing g3 and increasing g1 leads to highly linear and high gain performance over a wide range of frequencies.

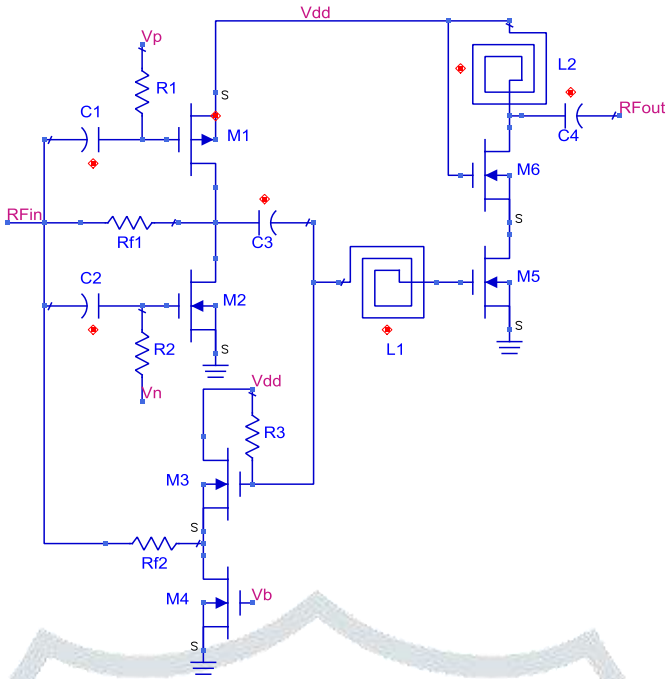

Figure 4. Proposed Wideband LNA without bias circuit

Figure 5.

III. PROPOSED WIDEBAND LNA CIRCUIT ANALYSIS

3.1. Wide-band input matching technique

Numerous topologies are proposed to adopt wideband performance. The distributed amplifier (DA) uses multiple amplifying stages and transmission lines to absorb the parasitic capacitances of transistors and provides good wideband gain but its suffer from larger chip area and large power consumption [58,59]. Another topology is common source amplifier with LC filter. However larger value of inductor not possible in RFIC need put inductors as an off chip components [60,61]. The common gate amplifier is a well known topology for constant wideband input matching with cost of low gain and high noise margin [62].

The first stage of proposed Wideband LNA consist shunt restive and common drain active feedback provide wideband matching and partial cancel noise to improve NF. In common source amplifier has a trade off between noise performance and tranconductance of amplifier. By using common drain active feedback we can set independent transconductance and noise performance. Fig. 4 shows the proposed Wideband LNA design. It consists of two stages. The first stage is an inverter configuration with resistive feedback in order to adopt wideband input matching and a low noise level. The second stage is a cascode amplifier for high gain in series and shunt inductive peaking to achieve a wider bandwidth.

3.2. Enhancement of gain

The series and shunt inductive gain peaking technique is used in second stage to boost the high-frequency gain of cascode amplifiers and to improve gain. The coupling circuit between two stage consists of inductor L2 and capacitor C2, which acts as a series resonance and resonates at the middle of the entire band. The drain low quality factor inductor L3 is used in output to improve the gain flatness at high frequencies. The two inductors value choose such that split the poles to extend bandwidth [57].

3.3. Noise analysis

In CMOS inverter the value of the feedback resistance plays an important role in deciding the amount of noise added to the input. There is tread off between noise figure and wideband input matching higher value of feedback resistor decrease NF but it not provide wider band input matching and vice versa. [42]. This tread off can be avoid by using common drain (CD) active feedback. Trough CD feedback we can add one more degree of freedom to set NF and input matching for wideband. Using CD feedback cancel some amount of noise by adding out off phase noise signals.

IV. SIMULATION RESULTS AND DISCUSSION

The proposed Wideband LNA was designed and simulate using the TSMC 0.18 µm RFCMOS process. Fig. 5 shows the simulation of S parameters. The input return loss (S11) was kept less than −8 dB within the entire band of interest. The output return loss (S22) was less than −8 dB in interested band. The simulated results of the gain (S21) is 12.7-15.6 dB in interested band. Figure 6 shows noise figure simulation result it is 2-4 dB in selected band.

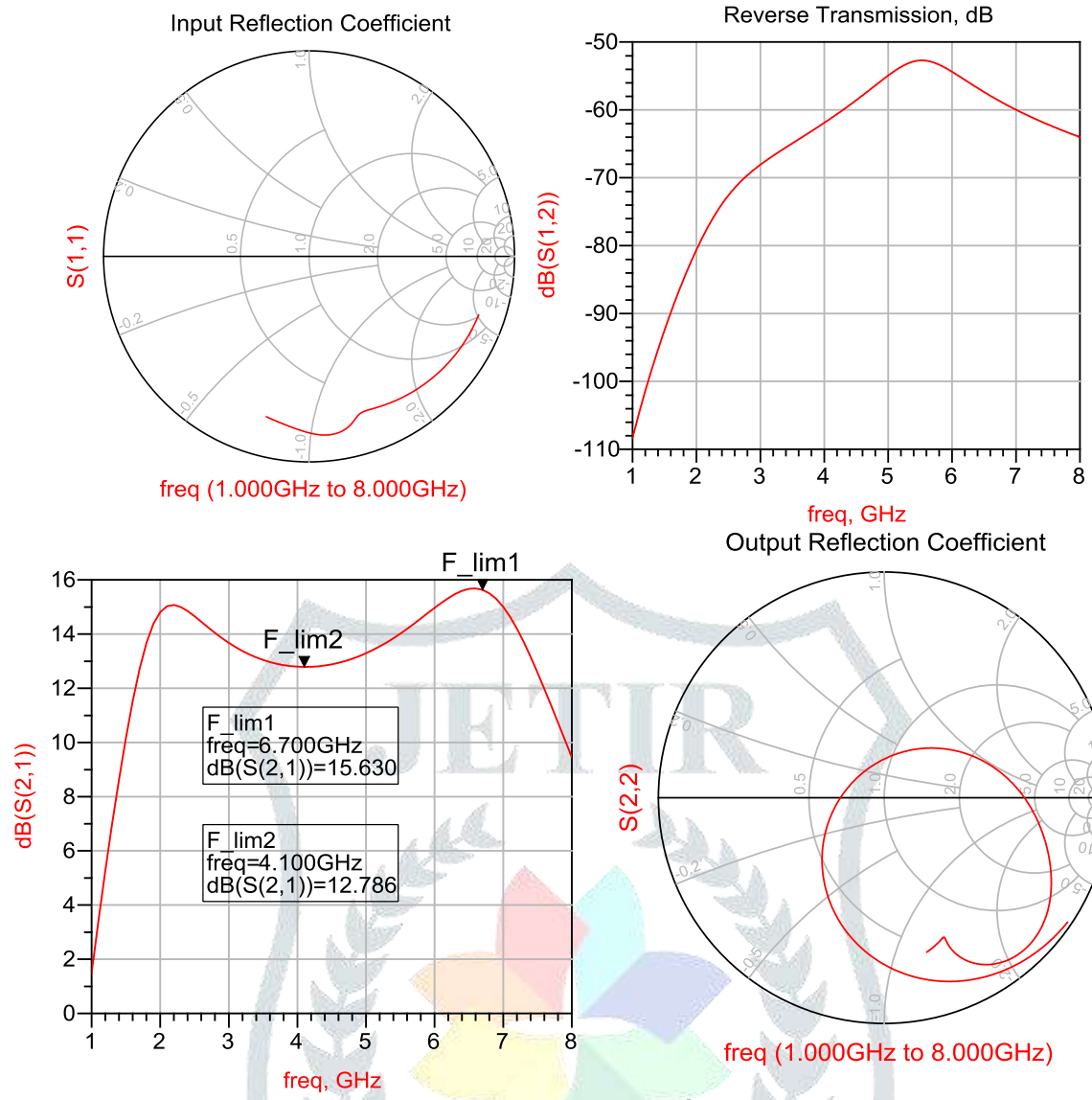

Figure 6. S Parameter results

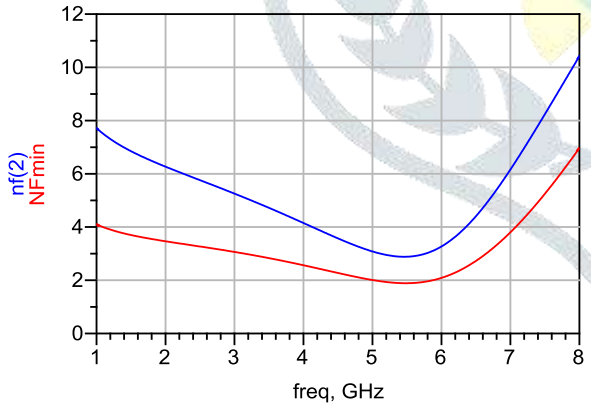

Figure 7. Noise Figure Simulation result

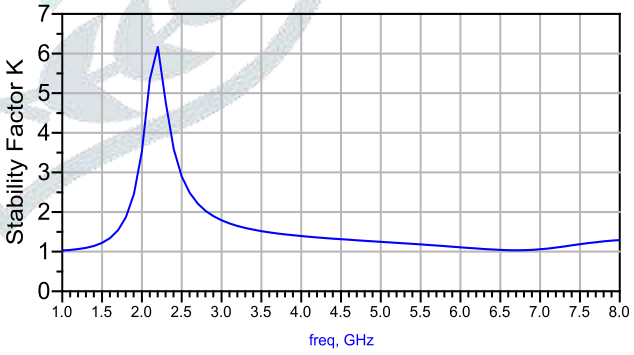

Figure 7. Stabilty Factor K v/s Frequency plot

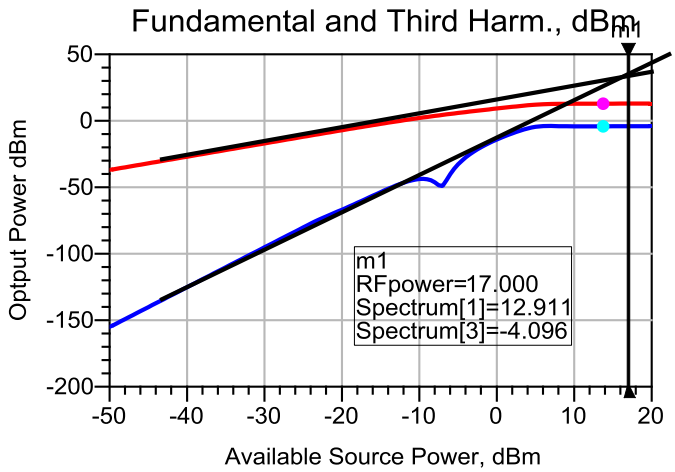

Figure 8 IIP3 at 5GHz

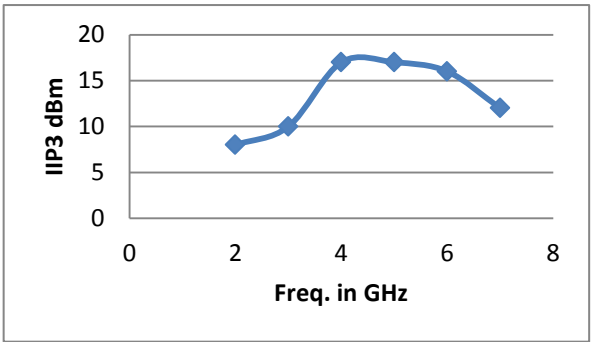

Figure 9 IIP3 value at different frequecy

The two tone test was performed for intermodulation distortion measurements, with 1 MHz spacing for IIP3 measurements. The two tone test was simulated at different frequencies within the band of interest (@ 3, 4, 5, and 6 GHz). Figure 7 shows the IIP3. At 5 GHz, the IIP3 is 17 dBm. As shown in Figure 8 presents the input third order intercept point at different frequencies its is greater than 8dBm in entire band. Table 1 presents the performance summary of the proposed Wideband LNA compared with recently published wideband LNAs. The total power consumption was 20 mw from 1.8 V voltage power supply.

The Figure 9 shows stability factor K graph which is more than 1 in interested band which shows circuit is unconditionally stable. The wideband LNA prove that the proposed linearization technique is effective in a wide range of frequencies, while maintaining high gain and excellent noise performance over the entire band of interest. As seen in Table 1, our proposed technique for linearity improvement achieves good result comparable to an IIP3 with the published wideband LNA. In Next generation receiver highly linear wideband LNA design is stringent requirement. Our design is stratified requirement of next generation receiver architecture to accommodate all standards.

V. CONCLUSION

A highly linear Wideband LNA is designed and simulated using standard 0.18 µm RFCMOS process. Based on the CMOS inverter topology, the proposed Wideband LNA greatly improves the IIP3 performance with a high gain and acceptable noise figure. The wideband extension technique was used in this paper by using in second stage series and shunt inductor to increase gain cover the entire band. The results of proposed Wideband LNA shows proposed design achieve a wide bandwidth performance with high linearity and gain and low NF. As per our knowledge this is first topology which provide excellent linearity with high gain, low noise figure and low power consumption.

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TABLE I. COMPARE RESULTS WITH PUBLISHED WIDEBAND LOW NOISE AMPLIFIER

Source	CMOS Technology (um)	BW (GHz)	S21 (dB)	NF (dB)	IIP3 (dBm)	Power Consumption (mW)	Topology
JSSC-2004 [20]	0.25	0.002-1.6	13.7	2.4	0	35	R FB +NMOS/PMOS
JSSC-2004 [21]	0.18	2.3-9.2	9.3	4	-6.7	9	CS + degeneration and input BPF
JSSC-2005 [22]	0.18	2-4.6	9.8	2.3	-7	12.6	CS + series RC FB
ICAT-2005 [23]	0.18	2.7-9.3	10	3.3	-0.3	14	Cascode + input HPF
JSSE-2006 [24]	0.18	3.1-10.6	9.5	5-5.6	-13	9.4	Cascode + input filter
JSSCC-2006 [25]	0.18	3-5	<16	2.2	-9	7.68	CS + miller effect input matching filter
JSSC-2006 [26]	0.18	0.04-7	8.6	4.2	+3	9	Distributed cascode
JSSC-2007 [27]	0.13	3.1-10.6	15.1	2.5	-8.5	9	CS + reactive FB
JSSC-2007 [28]	0.18	1.2-11.9	9.7	4.7	-6.2	20	CG + noise cancellation
JSSC-2007 [29]	0.18 SiGe	0.1-11	8	2.9	-3.55	21.6	Distributed cascode + BW enhancement
ISSCC-2007 [30]	0.13	1-7	17	2.4	-4.1	25	Cascode + CD FB
JSSC-2008 [31]	0.13	0.8-2	14.5	2.6	16	17.4	CG + noise and distortion cancellation
MJ-2008 [32]	0.18	5-6	20.5	1.8-2.6	-6.2	2	Cascode + inter stage LC network
ISSCC-2009	0.18	0.3-	21	2	-3.2	3.6	Differential CG + C Cross coupling

[33]		0.92					
ISSCC-2009 [34]	0.13	3.1-10.6	15	<4.5	-12.5	26	Weighted distributed cascode
TCAS-II -2010 [35]	0.18	3.1-10.6	13.9	4.7	-8.5	14.4	Parallel RC FB
MTT-s 2010 [36]	0.09	3.1-10.6	10.5	3.2	4	21.6	Cs + Π input filter
MTT-S 2010 [37]	0.18	31.-10.6	13	4.68	-12	10.34	CS + RLC input filter
RFIC 2010 [38]	0.09	21	15.4	6	-6.6	12.5	Distributed CS + tapered transmission line
MTT-2011 [39]	0.09	0.01-1.77	23	2	-2.85	2.8	Differential CG + multiple feedback
IET MAP 2012 [40]	0.18	2.4-11.2	14.8	3.9	-11.5	3.4	CG + current reuse
MTT-2012 [41]	0.13	0.6-3	42	3	-14	30	Pseudo differential + resistive FB
IJEC-2012 [42]	0.18	3.1-10.6	15	3.5-3.9	6.4	16.2	Inverter with FB
MWCL-2012 [43]	0.065	0.01-2.8	32	1	-13.6	40	Cascode + active –C element
TCAS-II-2013 [44]	0.18	0-1.3	10	3	+7.5	18	Cascode + active feedback
IJMST-2013 [45]	0.18	2.5-16	11	3.3	-	20	RC FB CS + current reuse
IJEC-2015 [46]	0.13	2.35-9.37	10.3	3.68	-4	9.97	CG current resue + noise cancelling
MJ-2015[47]	0.13	3.5-5	14	3.5-3.9	4	21	Fully differential + active FB + Noise cancelling
This Work	**0.18**	**2-7**	**12.7-15.6**	**3.5-4**	**17 @ 5GHz**	**20**	**CMOS inverter+active feedback**

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