Design of Level Shifter with Wide Voltage Conversion Range for System on Chip Applications

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Abstract : ***An energy efficient level shifter is an interfacing circuit which can interface low core voltage to high input-output voltage. It address the challenges posed by simultaneous use of different supply-voltage levels on the same circuit. It allows communication between different modules without adding any extra pin. so it can easily avoid voltage mismatch problem. The main objective of the work is to minimize power dissipation in shifter, which is due to multiple supply voltages in the circuit. The model presents a new energy efficient level shifter for logic voltage shifting from subthreshold to above- threshold domain. The proposed method uses Multi-threshold Complementary metal oxide semiconductor technique, which is one of the energy efficient design technique to achieve power minimization and also to provide a wide voltage conversion. The proposed design is implemented in CADENCE Virtuoso 180-nm technology process.***

Keywords : Level shifter, multi-supply voltage design, subthreshold operation,MTCMOS.

I. INTRODUCTION

ENERGY efficiency is one of the most important issues to address in today's System-on-a-Chip designs. Among thetechniques known in the literature to reduce power consumption, those based on power supply voltage reduction are considered very effective even though they can severely penalize speed performances [1], [2]. An alternative approach, known as the multi-supply voltage domain technique [3], consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements. Time-critical domains run at higher power supply voltage (VDDH) to maximize the performance, whereas noncritical sections work at lower power supply voltage (VDDL) to improve power efficiency. For extremely low-power applications, the presence of sections of the system operating in a sub-threshold regime is a valuable option [4]. A key challenge in the design of efficient multiple-supply circuits is minimizing the cost of the level conversion between different voltage domains while maintaining the overall robustness of the design. To such a purpose, level shifter (LS) circuitshave to be used. To down-convert from a higher voltage (within the oxide breakdown limits) to a lower voltage domain, CMOS inverters are usually adequate [4]. On the contrary, more complex LS topologies are required to up-convert signals from the lower to the higher power supply domain [5]. The issue is particularly compounded when the VDDL is lowered below the transistor's threshold voltage. In fact, in such a case, balancing the input section driving capability of the LS with sections of the circuit working at the VDDH voltage level requires proper design techniques [4], [6]–[10].

II RELATED WORKS

The traditional LS topology is the differential cascade voltage switch (DCVS) circuit. The DCVS-LS behaves as a ratioed circuit As a consequence, pull-up and pull-down strengths has to be properly balanced to ensure correct functionality of the circuit. This is difficult to achieve in practice when input signals have sub-threshold voltage levels[2]. Lütkemeier estimated that a NMOS-to-PMOS ratio of ~2400 is needed to design a fully functional DCVS-LS circuit which converts 0.2 V input signal into 1-V output signals, with 90-nm CMOS process technology [8].

III. CONVENTIONAL LEVEL SHIFER

The traditional LS topology is the differential cascade voltage switch (DCVS) circuit, as shown in Fig. 1. It includes a half-latch formed by two PMOS transistors (MP2 and MP3) and a pair of NMOS devices Controlled by the differential low-voltage input signals A and AN. When the input voltage A (AN) goes from low (high) to high (low), MN2 (MN3) is turned on (off). As a consequence, the voltage at node NH (NL) is pulled down, leading MP3 (MP2) to be turned on. This occurs when NH (NL) voltage reaches VDDH-Vth,MP3 (VDDH-Vth,MP2). Once MP3 (MP2) is turned on, the node NL (NH) starts to be charged, weakening MP2 (MP3). Thus, the positive feedback accelerates the voltage level conversion. It should be noted that the DCVS-LS behaves as a ratioed circuit and there is a contention between MP2 (MP3) and MN2 (MN3) transistors. As a consequence, pull-up and pull-down strengths need to be properly balanced to assure correct functionality. This requirement is difficult to achieve in practice when input signals have sub-threshold voltage levels [4].

A.VOLTAGE CONVERSION:

In [6], an architecture using four DCVS cascaded circuits is employed to convert voltages from 200 mV to 1.2V. Unfortunately, each conversion stage uses its own VDDH (i.e., 0.3, 0.4, 0.6, and 1.2 V).

B. STRATEGIES OF LEVEL SHIFTER:

The first one exploits a DCVS circuit with an always-on diode connected NMOS transistor at the top, whereas the second stage is a traditional DCVS circuit for achieving rail to rail swing.

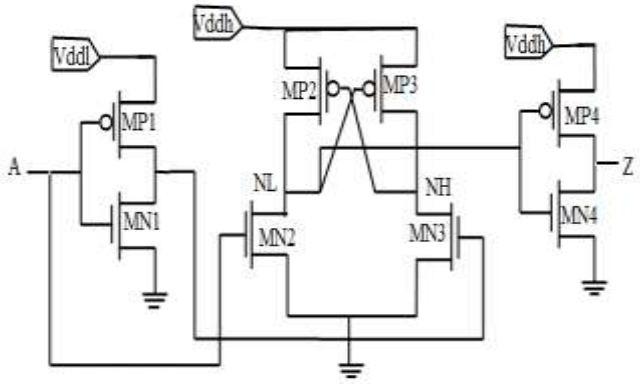

Figure.1. Conventional DCVS Level Converter.

C. DRAWBACKS

1. The above DCVS circuit introduce large power penalties. Because it is requiring multiple power switching to generate intermediate VDDHs.
2. It does not allow high-speed performance to be achieved where the above level shifter crcuit does not contain intermediate power lines

IV PROPOSED LEVEL SHIFTER

The proposed LS was designed using the commercial 90-nm CMOS ST Microelectronics process technology. The latter provides the designer with low-voltage threshold (lvt), standard voltage threshold (svt), and high-voltage threshold (hvt) transistors.

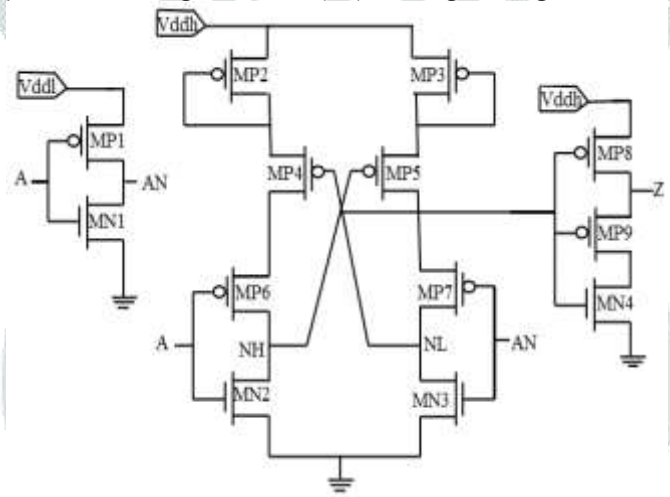

Figure.2. Schematic of proposed level shifter circuit.

A. Input Inverter

The input inverter consists of PMOS and NMOS transistors. They are driven by a lower supply voltage VDDL. The source of the PMOS transistor is connected to low supply voltage and the drain of NMOS is connected to ground. Low input signal of 375mV will be given to the input of the inverter.

B. Voltage Conversion Stage

It is based on DCVS (Differential Cascade Voltage Switch) logic. Figure 2 shows the explanation of the voltage conversion circuit. The circuit is designed with low-voltage threshold (lvt), standard voltage threshold (svt), and high-voltage threshold (hvt) transistors. To provide fast differential low-voltage input signals and to increase the strength of the pull-down network of the main voltage conversion stage, the input inverter was created using lvtdevices. To reduce the effect of cross bar current flowing in the nodes NH and NL, two lvt PMOS devices (MP2 and MP3) are adopted. MP4 and MP5 were chosen as hvt transistors. This helps in weakening the pull-up networks of the main voltage conversion stage. Finally, to ensure reliable voltage conversion, two diode connected hvt PMOS devices (MP6 and MP7) were placed between the pull-up logics and the supply rail VDDH. These devices limit the pull-up strength, but also lead to considerable reduced static power. We now briefly describe the running of the proposed circuit with particular attention to the differences between the new architecture and the conventional DCVS one. A high to low transition of the main input causes MP4 being turned on. Its drain current brings the diode-connected MP6 device into the saturation region. This creates a voltage drop(i.e., Vth,MP6) across MP6 terminals that produces a correspondent bulk source voltage drop on MP4. Due to the bulk effect, this increases the MP4 threshold voltage. The reduced voltage level (VDDH-Vth, MP6) on the source terminal of MP4 limits its VGS, thus further weakening the MP4 action. All the above effects reduce the contention on the node NH, thus allowing faster discharging to be achieved.

C. Factors affecting leakage:

Sub-threshold current increases exponentially due to reduction in threshold voltage and to Increase in thermal voltage.

D. Reducing the subthresthold leakage.

When MP4 is turned on, MP5 is consequently turned off. In this case, the small leakage current flowing through MP5 is not enough to turn MP7 on. For this reason, MP5 results power gated from the VDDH power rail, leading to a significant reduction in its sub-threshold current. The diode connected MP7 device participates in minimizing the leakage current, also by increasing the threshold voltage of MP5. In

fact,MP7 causes the source of transistor M5 to be at lower voltage than the bulk node and thereby reduces the subthreshold leakage current due to the bulk effect.

E. Output Inverter

Since MP6 limits the output range of the main conversion stage to [0 V, VDDH − VTp], an output inverter is connected to node NH, to assure a rail-to-rail conversion. The pull-down of such an inverter uses ansvtdevice, whereas its pull-up is designed by exploiting an hvtPMOS transistors stack, thus limiting the leakage current flowing through the pull-up network of the output inverter, when NH is high.

V. RESULTS AND DISCUSSIONS

The proposed circuit is implemented in CADENCE – Virtuoso tool and implemented in 180 nm CMOS technology. Figure 4 shows the schematic drawn in Cadence tool. The circuit dissipates 514.03µW of static power with the supply voltage of less than 375mV.

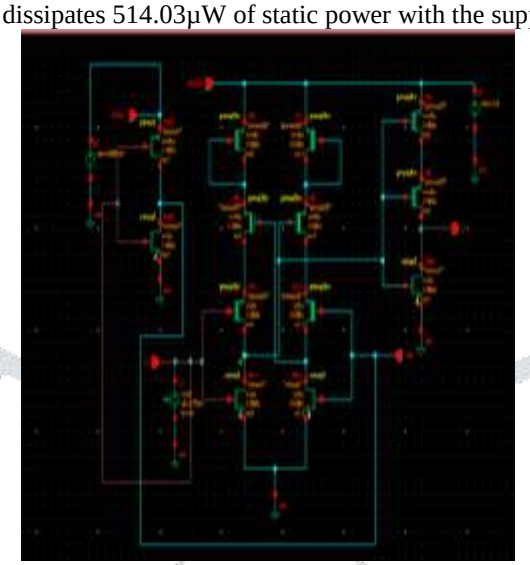

Figure.3 Schematic Circuit drawn in Cadence

The Figure.4 shows the simulated waveform in Cadence. Table 1 shows the performance comparison of DCVS and DCVS with MTCMOS level shifter circuits.It shows 375mV input signal will be converted into 1.8V output signal without affecting any conversion range of output signal by using Level shifter circuit with MTCMOS Technique.The table also shows a considerable reduction in static power.

Power calculations determine power-supply sizing, current requirements, Two components determine the power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

The power dissipation of the proposed LS circuit can be expressed as

Static power= I_{AVG} VDDH …. (1)

Dynamic power= CL V^2DDH f_{IN} … (2)

Where IAVG is the average current flowing through the circuit. Equation (1) shows that P is independent of VDDL and depends on fIN and the square of VDDH. Therefore average power calculation is expressed as

$$P_{AVG} = \alpha_{0\to1} . C_L . V_{DD}2 . f_{clk} \quad .. \quad (3)$$

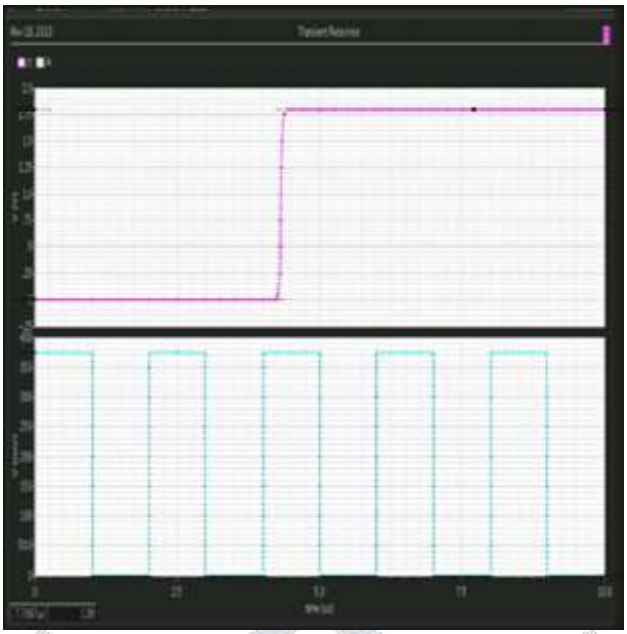

Figure.4 Simulated Output in Cadence

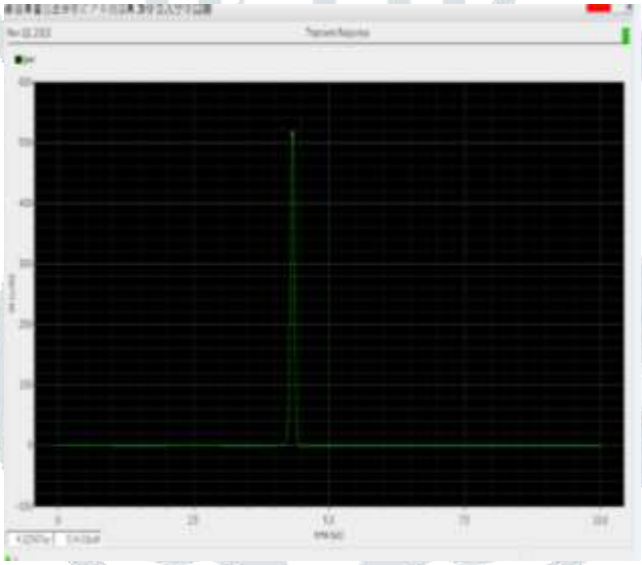

Figure.5 Power Spectral Graph of Proposed Circuit

Quan-tity	Compa-rator	Conventional DCVS	DCVS with MTCMOS
V_{DDL} (V)	200mV	375mV	375mV
Static power	6.4nW	784.2µW	514.0µW

Table.1 Performance Comparison Table

VI. CONCLUSION

The proposed level shifter with MTCMOS is presented and simulated in Cadence Virtuoso tool. The proposed circuit is implemented in 180-nm CMOS technology. The static power dissipation achieved was 514.03µW with a supply voltage of 0.2V.

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