HIGH PERFORMANCE AND LOW POWER VLSI CMOS 8-BIT MAGNITUDE COMPARATOR CIRCUIT DESIGN USING ONOFIC APPROACH

Dr. S. Aruna[1],K. Mounika [2], K. Srinivasa Naik[3]
Assistant Professor[1], M.Tech Scholar [2], Associate Professor[3]
[1,2,3]Department of Electronics and Communication Engineering
[1,2]Andhra University College of Engineering, India
[3]VIIT, India

Abstract: In low power VLSI circuit designs, the leakage power reduction plays an important role. The scaling down of threshold voltage has contributed vastly towards increase in sub threshold leakage current thereby making the static (leakage) power dissipation very high. Due to the leakage power the battery operated devices with long duration in standby mode may be drained out very quickly. In this work, high performance and low power ONOFIC approach have been implemented for VLSI CMOS (Complementary Metal Oxide Semiconductor) circuits. Many techniques have been proposed for reducing leakage current in deep submicron but with some limitations they are not suitable for actual requirements. Here discuss three techniques named CMOS, LECTOR (LEakage Control TransistOR) and ONOFIC (On/Off logic). In this work, 8-bit magnitude comparator is designed by three techniques and compare the power dissipation and performance among CMOS, LECTOR and ONOFIC. The tool which is used for implementing the design is Tanner EDA V15.0.

Keywords: Leakage current, ONOFIC, LECTOR, deep submicron.

I. INTRODUCTION

In the last some years due to the ever growing demand for portable and small sized devices, integrated circuits need electronic circuit design methods to implement integrated circuits with low power consumption. The design of a low power circuits mainly focus on a problem occurred due to the performance, power dissipation and chip area.The constraint in deep submicron is to reduce the device dimensions in the design of logic circuit leads to decreased chip area [4]. To improve the reliability of a logic circuit in deep submicron regime, the supply voltage is reduced. In electronic devices, to control the power consumption a supply voltage plays an important role. Supply voltage scaling without scaling of threshold voltage degrades the performance of the device. By reduction of threshold voltage and supply voltages proportionally retains the performance. The threshold voltage reduction leads to the five times higher leakage current [5]. In the modern design of several electronic components High speed operation with low power dissipation is becoming a critical factor. In this paper we are discussing Leakage control transistor (LCT) technique is LECTOR and ONOFIC to reduce the power consumption and power dissipation.

II.LITERATUREREVIEW

Many techniques have been come into existence to overcome the leakage power problem in the nanoscale technology, but those techniques have tradeoff between area, delay and also active power. Sleep transistor technique is one of the techniques proposed for leakage reduction, Bulky NMOS and/or PMOS device called sleep transistor is used in a path between supply voltage and ground rails in the circuit ground, and creating virtual power [6]. When the circuit is operating in active mode this creates a negative effect on the switching speed of the circuit. Forced stack technique introduces an additional transistor for every input of the gate in both N-network and P-network. This ensures that two transistors are OFF instead of one for every OFF-input of the gate and hence makes a significant savings on the leakage current [7]. Both techniques creates a negative effect on the switching speed of the circuit. Sleepy stack technique each transistor is replaced with two half sized transistors and one extra sleep transistor [8]. In sleepy stack structure the leakage reduction occurs in two ways. One is the leakage power is suppressed by high-Vth transistors and the other is two stacked and turned off transistors induce the stack effect. By mix these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. MTCMOS technique uses low, normal and high threshold voltage transistors in designing a CMOS circuit. The low-threshold voltage transistors which have high performance are used to reduce the propagation delay time in the

critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path [9], [10]. This technique needs two distinct threshold voltage transistors which lead to extra mask layers. This makes the fabrication process complex. In LECTOR technique, two leakage control transistors (PMOS andNMOS) are introduced [11] between the pull-up network and pull-down network within the logic circuit shown in Figure 1. These transistors are connected as such that one of the transistors is always near the cut-off voltage for any input combination. This increases the path resistance from supply to ground, leading to significant reduction of leakage currents. In both active modes as well as in the standby modes the LECTOR technique works effectively.

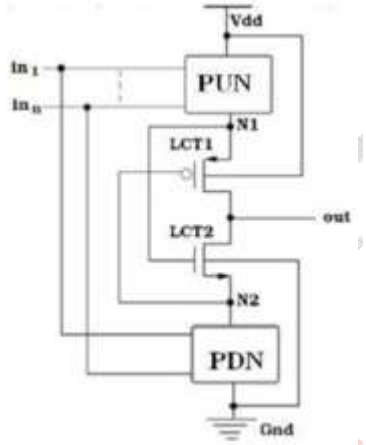

Figure 1: Generalized structure for leakage control gates

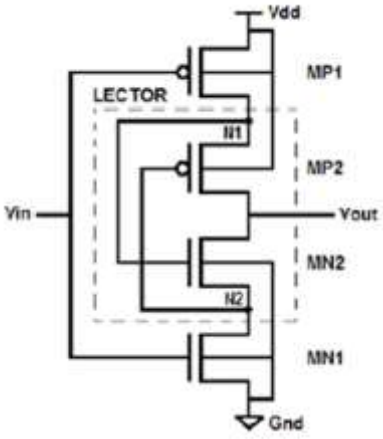

Figure 2: Inverter Gate design using LECTOR

Table 1: Truth table for LECTOR Inverter

Input	MP1(PMOS)	MP2(PMOS)	MN1(NMOS)	MN2(NMOS)	Output
0	ON	Near Cut-off	OFF	ON	1
1	OFF	ON	ON	Near Cut-off	0

III. PROPOSEDONOFIC

The proposed On/Off logic (ONOFIC) approach [1], [2] reduces the leakage current and power with single threshold voltage level approach. ONOFIC Technique able to reduces the leakage current in both active and standby mode of logic circuit. Same as LECTOR technique the ONOFIC approach also introduces an additional logic between pull-up and pull down networks for leakage reduction. This extra introduced circuit is called On/Off logic (ONOFIC) circuit. This proposed approach contains one PMOS and one NMOS transistor. Due to maintaining either on or off condition for any output logic level this technique is known as ONOFIC. The connection of ONOFIC is shown in Figure 2 .When ONOFIC block is off this technique provides maximum resistance and it provides minimum resistance when it is in on state. This logic gives less power dissipation and propagation delay of the logiccircuit.

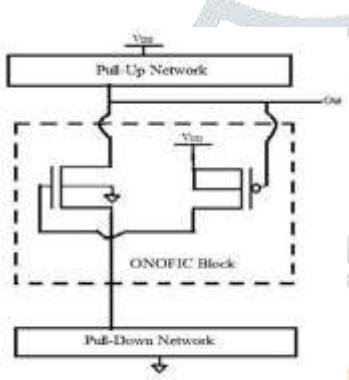

Figure 3: Schematic of ONOFIC logic

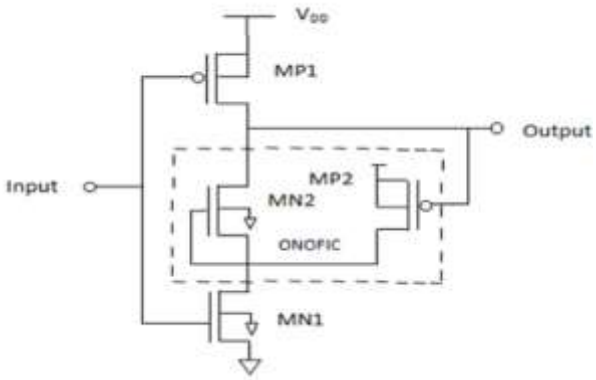

Figure 4: Inverter circuit using ONOFIC logic

Table 2: Truth table for ONOFIC

Input	MP1(PMOS)	MN1(NMOS)	ONOFFIC (PMOS)	ONOFFIC (NMOS)	Output
0	ON	OFF	OFF	OFF	1
1	OFF	ON	ON	ON	0

IV. INTRODUCTION ABOUTCOMPARATORS

In digital systems Data comparison is needed while performing arithmetic or logical operations. Common and very useful combinational logic circuit is digital comparator circuit. Digital or Binary comparators are made up are from standard AND,OR and NOT gates that compare the digital signals present in their input terminals and produce an output depending on the input condition of those inputs.

Types of digital comparators

Identity Comparator: It is a digital comparator and that has only one output terminal for when A=B either "HIGH " A=B=1 or "LOW"A=B=0.

Magnitude Comparator: Magnitude comparator is a digital comparator which has three output terminals. One each for equality, A=B greater than, A>B less than A<B.

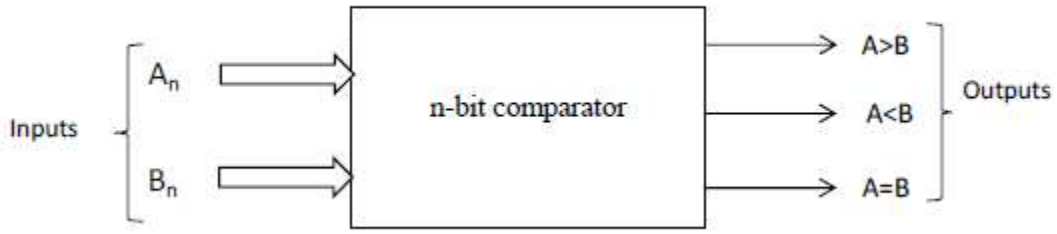

Figure 5: n-bit comparator

Depending up on the application requirement these comparators can compare 2-bit, 4-bit and 8-bit numbers. These are available in TTL as well as CMOS logic family ICs and some of these ICs include IC 7485 & 74LS85 (4-bit comparators), IC 4585 (4-bit comparator in CMOS family) and IC 74AS885 (8-bitcomparator).

4-bit magnitude comparator:

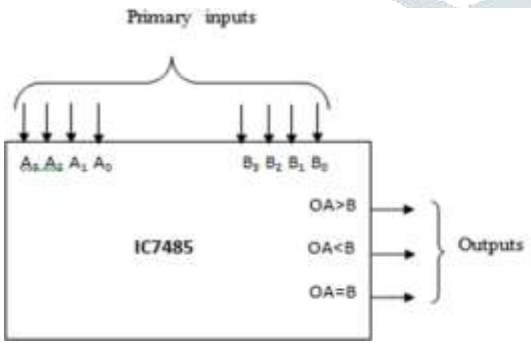

Figure 6: 4-bitmagnitude comparator

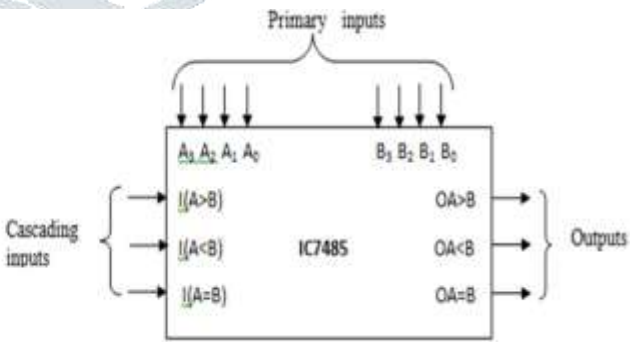

Figure 7: 4-bit magnitude comparator with cascading inputs

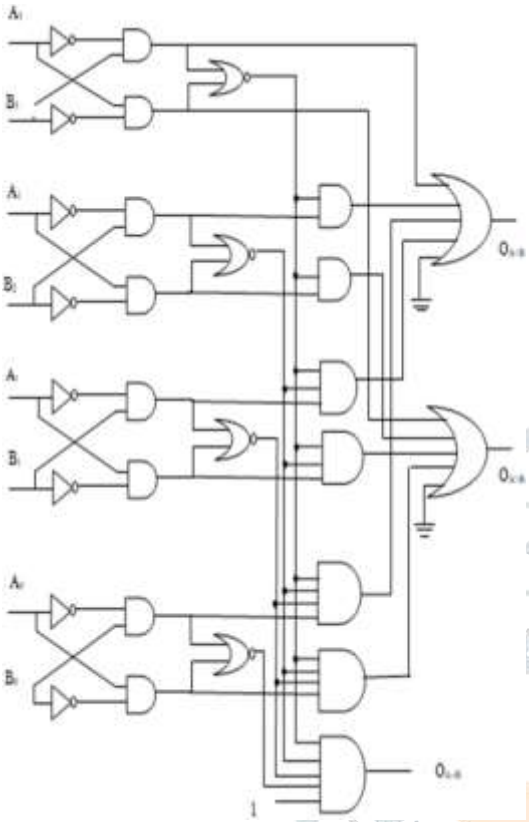

Figure 8: Schematic diagram for 4-bit magnitude comparator

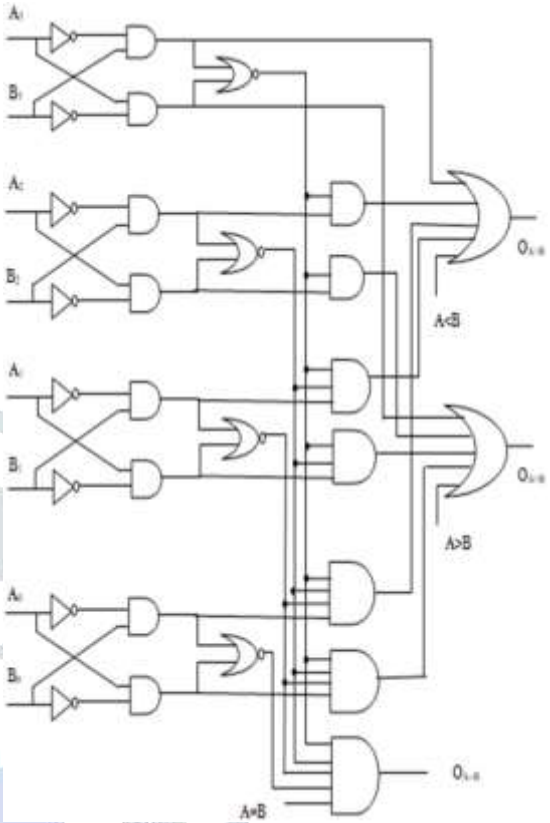

Figure 9: Schematic diagram for 4-bit magnitude comparator with cascading inputs

Table 3: Truth table for 4-bit magnitude comparator

Comparing inputs				outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B
A3>B3	X	X	X	H	L	L
A3<B3	X	X	X	L	H	L
A3=B3	A2>B2	X	X	H	L	L
A3=B3	A2<B2	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	H	L	L
A3=B3	A2=B2	A1<B1	X	L	H	L
A3=B3	A2=B2	A1=B1	A1>B1	H	L	L
A3=B3	A2=B2	A1=B1	A1<B1	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H

Table 4: Truth table for 4-bit magnitude comparator with cascading inputs

Comparing inputs				Cascading inputs			outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A>B	A<B	A=B	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A1>B1	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A1<B1	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

8-Bit Magnitude Comparator:

An 8-bit comparator compares the two 8-bit numbers by cascading of two 4-bit comparators. The circuit connection of this comparator is shown below in which the lower order comparator A<B, A=B and A>B outputs are connected to the respective cascade inputs of the higher order comparator.

For the lower order comparator, the A=B cascade input must be connected High, while the other two cascading inputs A ,B must be connected to LOW. The outputs of the higher order comparator become the outputs of this eight-bit comparator.

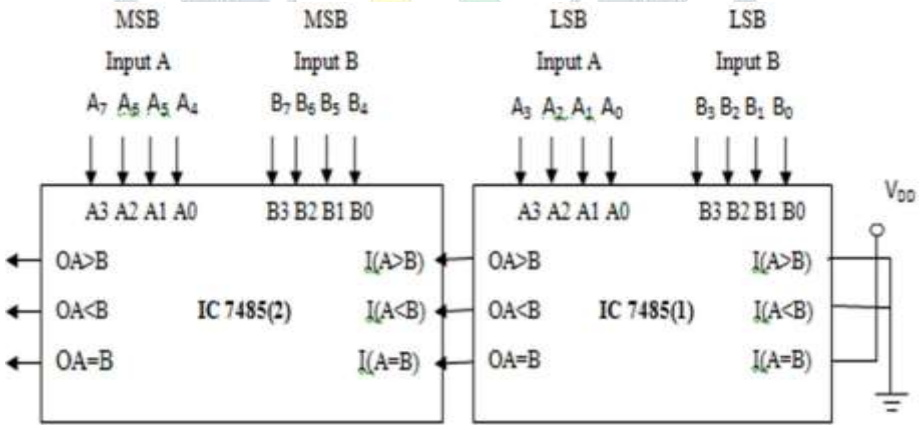

Figure 10: 8-bit magnitude comparator

Table 5: Function table for 8-bit magnitude comparator

Inputs		Outputs		
A7-A4,B7-B4 (**H**igher nibble)	A3-A0,B3-B0 (**L**ower nibble)	A>B	A<B	A=B
$A_H>B_H$	X	H	L	L
$A_H<B_H$	X	L	H	L
$A_H=B_H$	$A_L>B_L$	H	L	L
$A_H=B_H$	$A_L<B_L$	L	H	L
$A_H=B_H$	$A_L=B_L$	L	L	H

V. RESULTS &DISSCUSSIONS

Schematic diagrams for inverter using different logics:

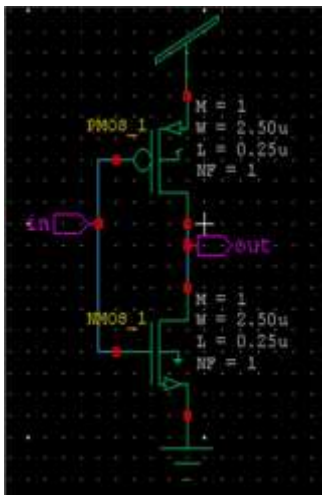

Figure 11: CMOS Inverter

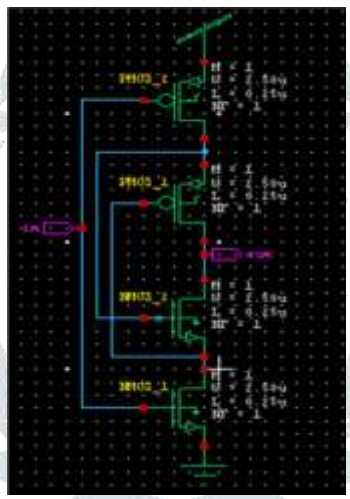

Figure 12:LECTOR Inverter

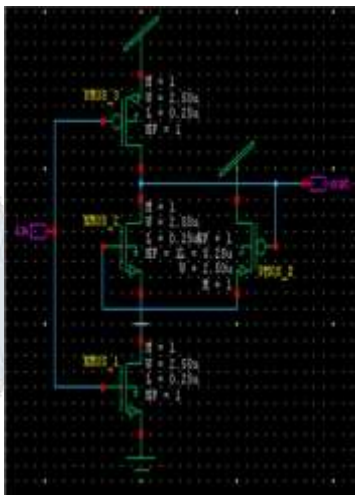

Figure 13: ONOFIC Inverter

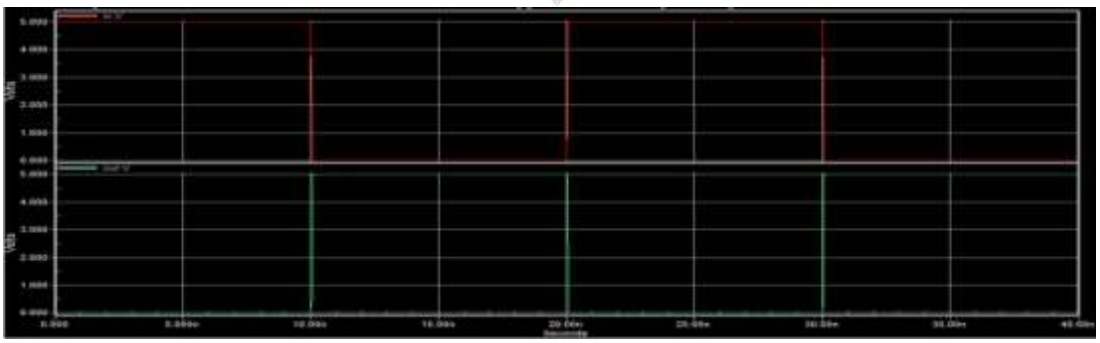

Figure 14: Output waveforms for Inverter

Schematic diagrams for inverter using different logics:

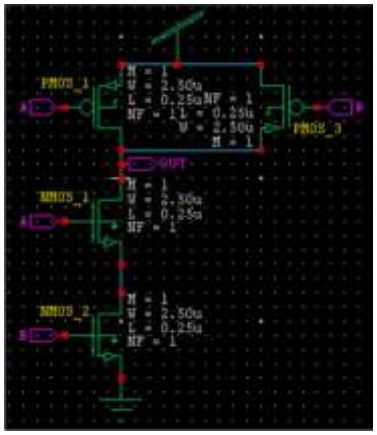

Figure 15: CMOS NAND

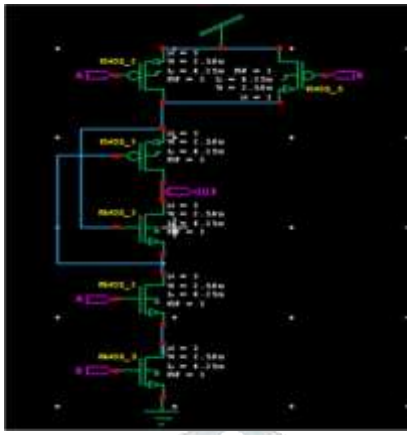

Figure 16: LECTOR NAND

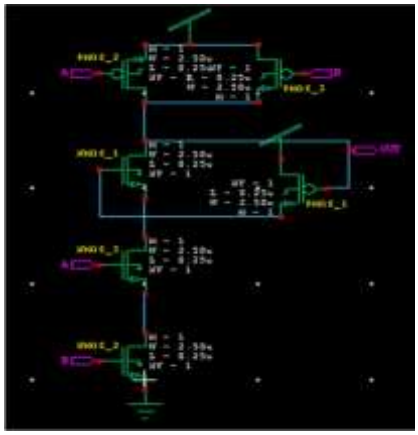

Figure 17: ONOFIC NAND

Figure 18: Output waveform for NAND

Schematic diagrams for NAND gate using different logics:

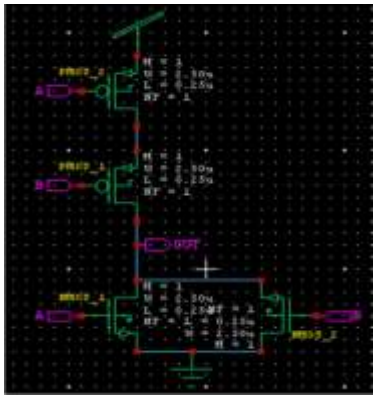

Figure 19: CMOS NOR

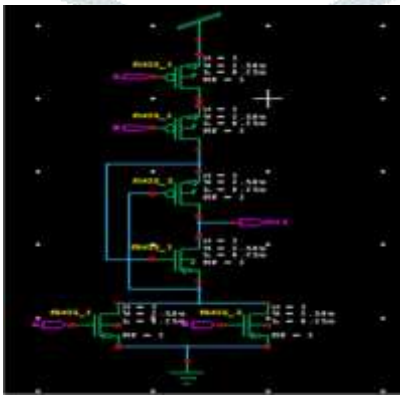

Figure 20:LECTOR NOR

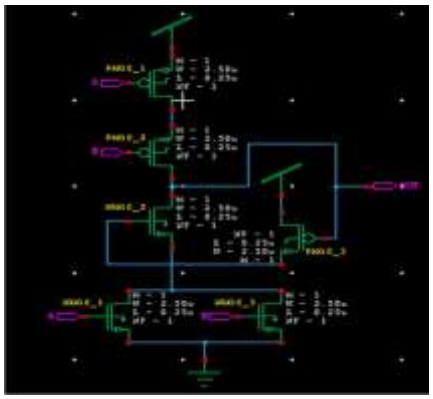

Figure 21: ONOFIC NOR

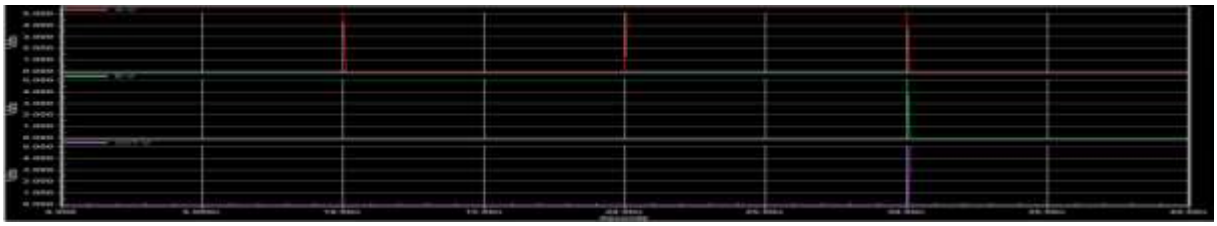

Figure 22: Output waveforms for NOR

4-bit Magnitude Comparator:

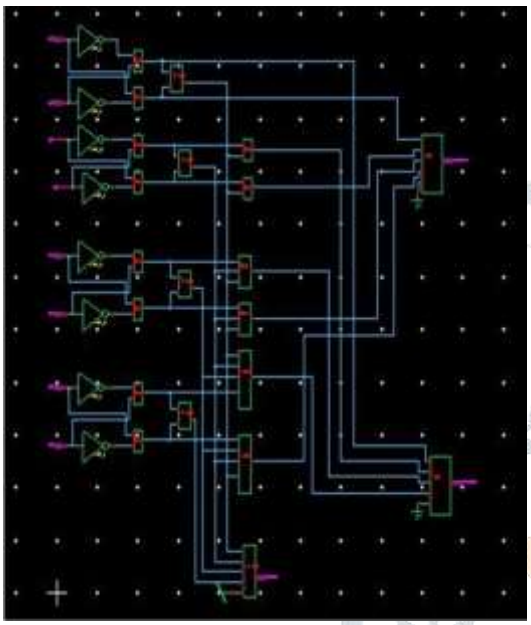

Figure 23: Schematic diagram for 4-bit Magnitude Comparator

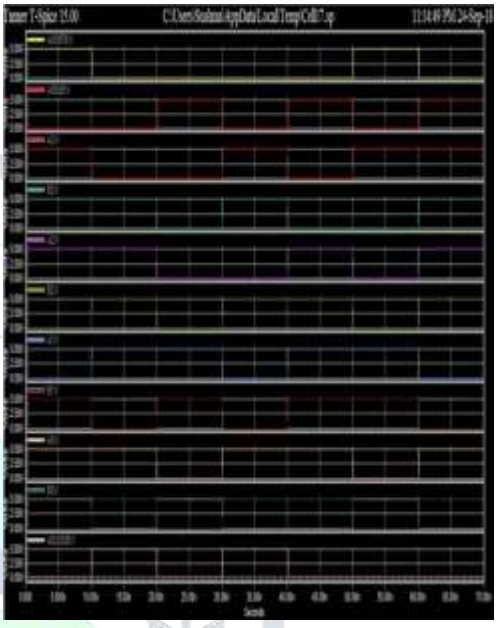

Figure 24: Output waveforms for 4-bit Magnitude Comparator

4-bit Magnitude Comparator with cascading inputs :

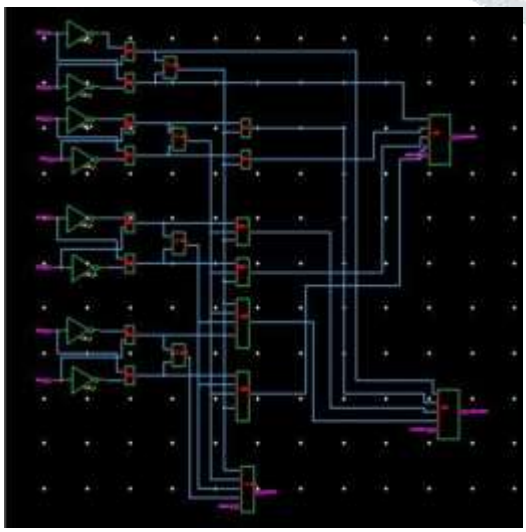

Figure 25: Schematic diagram for 4-bit Magnitude Comparator with cascading inputs

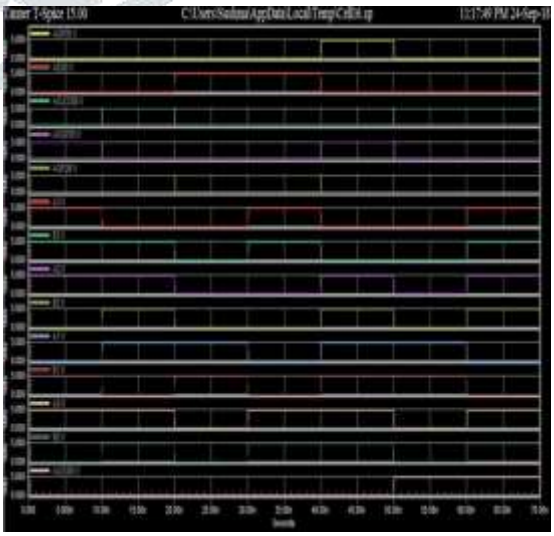

Figure 26: Output waveforms for 4-bit Magnitude Comparator with cascading

inputs

8-bit magnitude comparator:

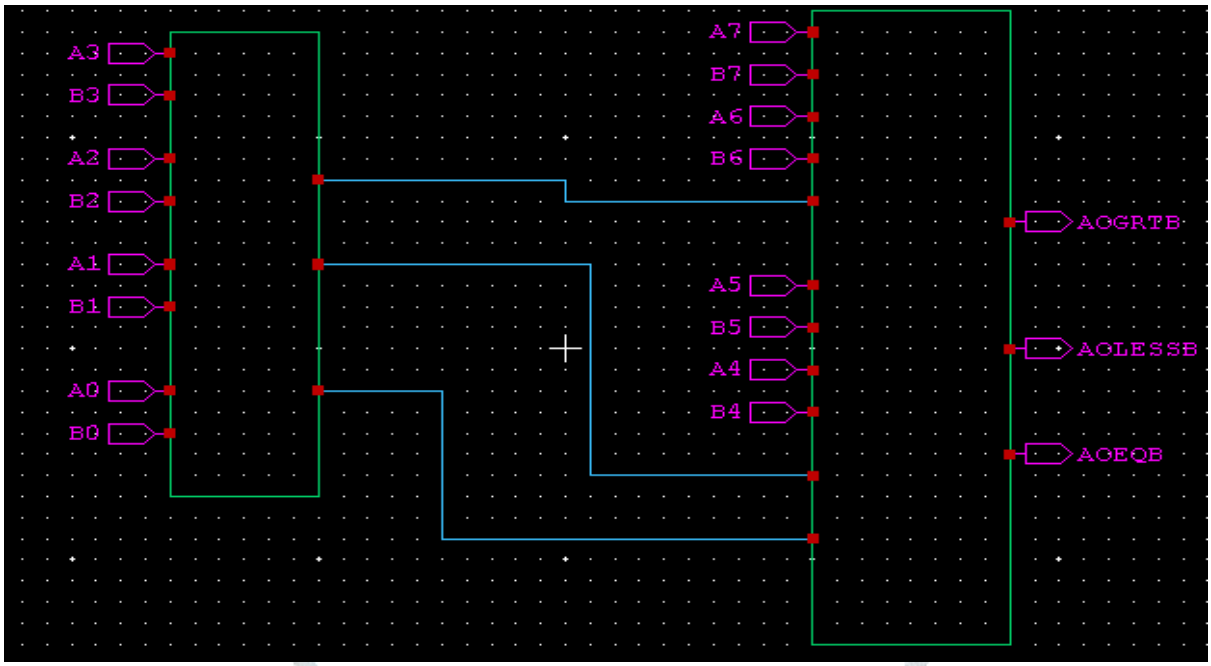

Figure 27: Schematic diagram for 8-bit Magnitude Comparator by cascading with two 4-bit Comparators

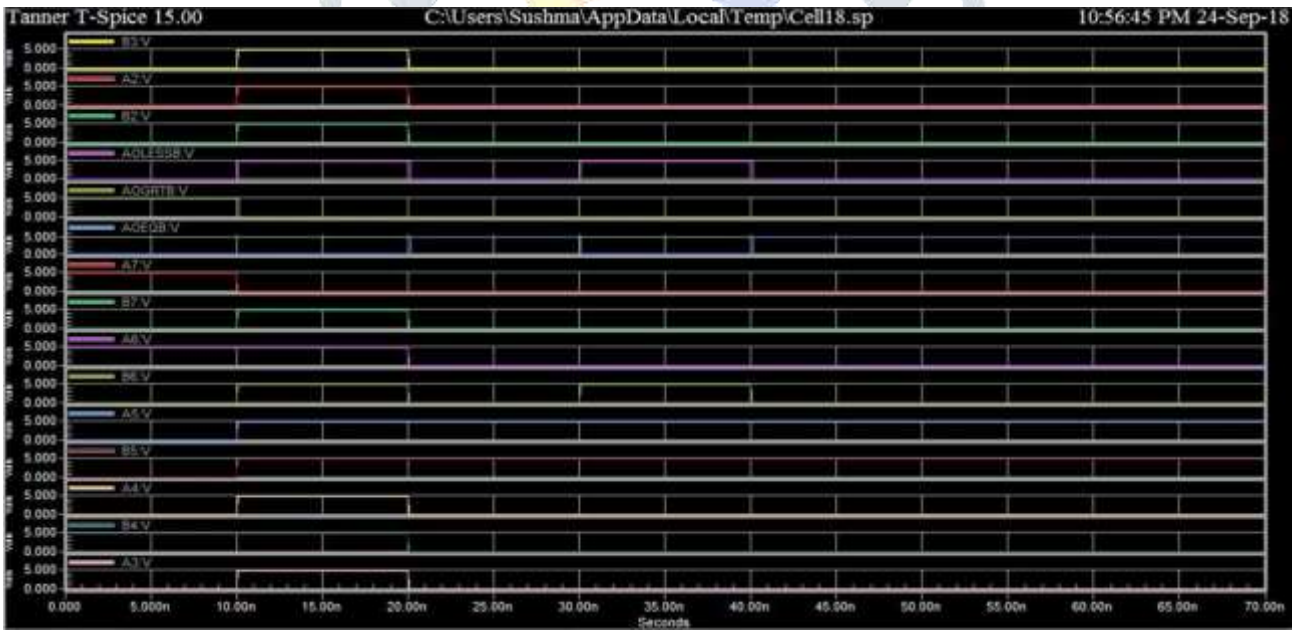

Figure 28: Output waveforms for 8-bit Magnitude Comparator by cascading with two 4-bit Comparators

Table 6: Average power dissipation and delay for different logics

Type of design	Delay (ns)	Power dissipation(µw)
CMOS Inverter	10.01	0.638
LECTOR Inverter	9.98	0.534
ONOFIC Inverter	9.01	0.398
CMOS NAND	19.97	0.12
LECTOR NAND	10.46	0.08
ONOFIC NAND	10.41	0.03
CMOS NOR	9.59	0.67
LECTOR NOR	9.61	0.66
ONOFIC NOR	9.53	0.14

Table 7: Delay results for CMOS, LECTOR and ONOFIC logics

Type of circuit	Delay (Ps)		
	CMOS	LECTOR	ONOFIC
4-bit magnitude comparator	20.97	19.72	17.54
4-bit magnitude comparator with cascading inputs	11.65	10.62	9.98
8-bit magnitude comparator	16.17	10.78	10.15

The above Table 7 gives comparison is among conventional CMOS circuits, LECTOR & ONOFI. It is found that delay of ONOFIC decreases with compare to conventional CMOS results, LECTOR results.so our proposed ONOFIC technique gives high performance compare to other techniques.

Table 8: Average power consumption in CMOS, LECTOR and ONOFIC logics

Type of circuit	Average power consumption in (µw)			% of power saving in ONOFIC compare with CMOS
	CMOS	LECTOR	ONOFIC	
4-bit magnitude comparator	0.12	0.11	0.10	16
4-bit magnitude comparator with cascading inputs	1.15	1.12	1.10	4.3
8-bit magnitude comparator	0.14	0.12	0.11	21.4

The above Table 8 gives comparison of average power consumption is among conventional CMOS circuits, LECTOR &ONOFIC.

From above observation the ONOFIC logic consume less power compare with LECTOR & ONOFIC .21.4% of power saving in 8-bit magnitude ONOFIC comparator compared with CMOS & 8.3% of power saving in 8-bit magnitude ONOFIC comparator compared with LECTOR. So finally in ONOFIC logic power consumption is less compare with conventional CMOS and LECTOR.

VI .CONCLUSION

In this work the new low power technology is used to designed ONOFIC technique for reducing the leakage power and improve the performance. The Inverter, NAND, NOR gates and 8-bit magnitude comparator has been designed by three (CMOS, LECTOR, ONOFIC) logic techniques. These techniques are implemented in the TANNER EDA V15.0 tool to find the leakage power dissipation and propagation delay. This proposed ONOFIC technique is proved which gives better results due to provides the maximum resistance to the ONOFIC block when it is in off state and minimum resistance when it is in on state. So, it is helpful in saving power i.e., 21.4% & 8.3% of power saving in 8-bit magnitude ONOFIC comparator compared with CMOS & LECTOR respectively. Due to less power & delay the proposed ONOFIC approach for 8-bit magnitude comparator is suitable for faster circuit operation, if propagation delay is the main criteria.

REFERENCES:

[1] Preeti Varma,''Estimation of leakage power and delay in CMOS circuits using parametricvariation''ELSEVIER-2016.

[2] Umesh jeevalu chavan, Siddarama R Patil''High Performance and Low Power ONOFIC Approach for VLSI CMOS CircuitsDesign''IEEE-2016.

[3] Siddesh Gaonkar" Design of CMOS inverter using LECTOR technique to reduce the leakage power. Issue 31(September, 2015).

[4] Partha Bhatatacharyya," Performance Analysis Of A Low Power High Speed Hybrid 1-Bit Full Adder Circuit".10.11.09\TVLSI' 2014'2357057 IEEE ,23 pp. 1036–8210.

[5] Vijay Kumar, Manisha Pattanaik" VSLSI Scaling And Low Power CMOS Buffer Circuit"Vol 34 No .9 2013 10.1088/16744926/34//9095001.

[6] M. D. Powell, S. H. Yang, B. Falsafi, K. Roy, and T. N. Vijay kumar, "Gated-Vdd: A ciruit technique to reduce leakage in deep submicron cache memories," in Proc. IEEE ISLPED, 2000, pp.90-95.

[7] S. Narendra, S. Borkar, V. De, D. Antoniadis, and A. P. Chandrakasan, "Scaling of stack effect and its application for leakage reduction," Proc. IEEE ISLPLED, pp. 195– 200, Aug.2001.

[8] J. C. Park, "Sleepy Stack: A new approach to Low Power VLSI logic and memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology,2005.

[9] Phanikumar M and N. Shanmukha Rao, "A Low Power and High Speed Design for VLSI Logic Circuits Using Multi-Threshold Voltage CMOS Technology", International Journal of Computer Science and Information Technologies (IJCSIT), Vol. 3(3), 2012,4131-4133.

[10] Dong Whee Kim, JeongBeomKee, "Low Power Carry Look-Ahead Adder With Multi Threshold Voltage CMOS Technology", in Proceeding of ICSICT International Conference on Solid-State and Integrated Circuit Technology, pp. 2160-2163,2008.

[11] NarenderHanchateand and Nagarajan Ranganathan, "LECTOR: A Technique for Leakage Reduction in CMOS Circuits," IEEE Transactions on VLSI Systems, vol. 12, no. 2, Feb 2004, pp.196-205.

[12] Angshumn Chakraboty And Sambhu Nath Pradhan"Two New Techniques To Reduce Gate Leakage At 65 nm Technology".*IEEE*-978-1-4673-2620-9/12/2012.CODEC.

[13] RohitLorenzo,AndSaurabhChaudhury"ANewLowLeakageAndHighSpeedTechniqueForCMOSCircuits".*IEEE* 2014 978-1-4799-4939-7/14.

[14] Anjana R And Ajay Kumar Somkwar "Analysis Of Sub Threshold Leakage Techniques In Deep Sub Micron Regime For CMOS VLSI Circuits" *IEEE*-2013978-1-4673-5301-4/13.

[15] Frank Anthony Hurt ado And Eugene John"A Combination Analysis Of Leakage Reduction Techniques In Nano scale CMOS Arithmetic Circuits" *IEEE*2014.

[16] C.J.XiayingZhao AndJiangfang"LeakagePowerReductionForCMOSCombinationCircuits"2006*IEEE*1-4244-0161.

[17] HeungJunJeon,YongBinKim"StandbyLeakagePowerReductionTechniqueForNanoscaleCMOSVLSISystems"*IEEE* 2010].