DESIGN OF 4-2 COMPRESSOR STRATEGY THROUGH INNOVATIVE XOR-XNOR MODULE

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ABSTRACT:

A low-strength excessive pace 4:2 compressor circuits is proposed for immediate virtual arithmetic incorporated circuits. The 4:2 compressors have been extensively hired for multiplier realizations. Based on a brand new different OR (XOR) and extraordinary NOR (XNOR) module, a four: 2 compressor circuits have been designed. Proposed circuit suggests strength intake could be very less. Power consumption and put off of proposed 4-2 compressor circuit were in comparison with in advance suggested circuits and proposed circuit is demonstrated to have the minimal strength consumption and the lowest delay. Simulations have been completed by means of the usage of Verilog HDL

INTRODUCTION:

Multipliers are one of the most large blocks in computer mathematics and are generally utilized in distinct digital sign processors. There is developing needs for excessive pace multipliers in unique packages of computing systems, collectively with pc snap shots, medical calculation, image processing and so forth. Speed of multiplier determines how rapid the processors will run and architects are truely more focused on immoderate speed with low electricity intake. The multiplier shape consists of a partial product generation level, partial product discount level and the final addition level. The partial product reduction diploma is accountable for a huge a part of the total multiplication postpone, energy and place. Therefore in order to build up partial products, compressors usually put in force this degree because of the fact they contribute to the discount of the partial products and moreover contribute to lessen the vital path this is critical to keep the circuit's standard overall performance.First all the eight inputs are fed as enter to the AND gates which shape sixteen products as established within the fig and shape a tree like shape. Then the ones inputs are further fed to ½ adders, whole adders and compressors to reduce the partial merchandise.

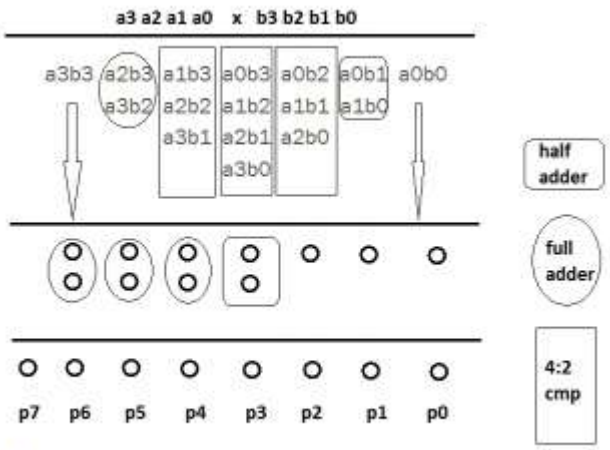


Fig.1.

This is accomplished with the aid of the use of 3-2, 4-2 compressor systems. A three-2 compressor circuit is likewise called complete adder cell. Since those compressors are used again and again in big systems, so improved design will make a contribution masses closer to standard tool performance. The inner structure of compressors is essentially composed of XOR-XNOR gates and multiplexers. The XOR-XNOR circuits are also constructing blocks in numerous circuits like mathematics circuits, multipliers, compressors, parity checkers, and many others. Optimized format of those XOR-XNOR gates can improve the overall performance of multiplier circuit. In gift work, a XOR-XNOR module has been proposed and 4-2 compressor has been applied the usage of this module. By the usage of partial product accumulation in proposed circuit reduces electricity consumption. Following circuit shows compressor circuit is fashioned by using manner of xor-xnor gates

COMPRESSOR CIRCUIT BUILDING BLOCKS

There are different architectures and designs of 4-2 compressor circuits reported in literature. These are mainly composed of two types of circuits: XOR-XNOR circuits and multiplexers (MUX). Complementary CMOS uses the dual networks to implement a given function. One part consists of complementary pull-up PMOS network while other part consists of pull-down NMOS networks. This technique requires more numbers of transistors and large layout area. Static CMOS XOR and XNOR [3] gate is shown in figure 1(a). Another implementation of XOR-XNOR circuit with 12 transistors is shown in figure 1(b) [4]. Further in figure 1(c) two pull-up PMOS-transistors and two pull-down NMOS–transistors are added to restore full swing operation. The circuit performs successfully at low supply voltages but this comes at the expense of increased area and number of transistors. Another disadvantage of the circuit is that each of the inputs drives four gates instead of two gates doubling the input load. This will cause slow response when this circuit is cascaded added together in this manner. It is only the final recombination of the final carry and sum that requires a carry propagating addition. 3:2 compressor is also known as full adder. It adds three one bit binary numbers, a sum and a carry. The full adder is usually a component in a cascade of adders. The carry input for the full adder circuit is from the carry output from the cascade circuit. Carry output from full adder is fed to another full adder

III. 4:2COMPRESSOR

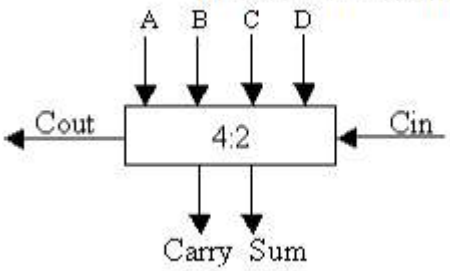
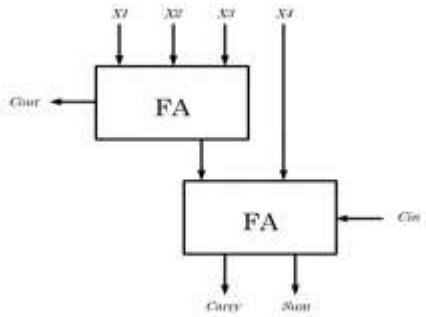


Fig.2. High level view of the 4:2 compressor.

The characteristics of the 4:2 compressor are:

- The outputs represent the sum of the five inputs, so it is really a 5 bit adder as shown in Fig.2.
- Both carries are of equal weighting (i.e. add "1" to the next column)
- To avoid carry propagation, the value of Cout depends only on A, B, C and D. It is independent of Cin.
- The Cout signal forms the input to the Cin of a 4:2 of the next column.

The common implementation of a 4-2 compressor is accomplished by utilizing two full-adder (FA) To add binary numbers cells.4:2 compressor is composed of two serially connected full adders. With minimal carry propagation we use compressor adder instead of other adder. Compressor is a digital modern circuit which is used for high speed with minimum gates requires designing technique. This compressor becomes the essential tool for fast multiplication adding technique on fast processor and lesser area



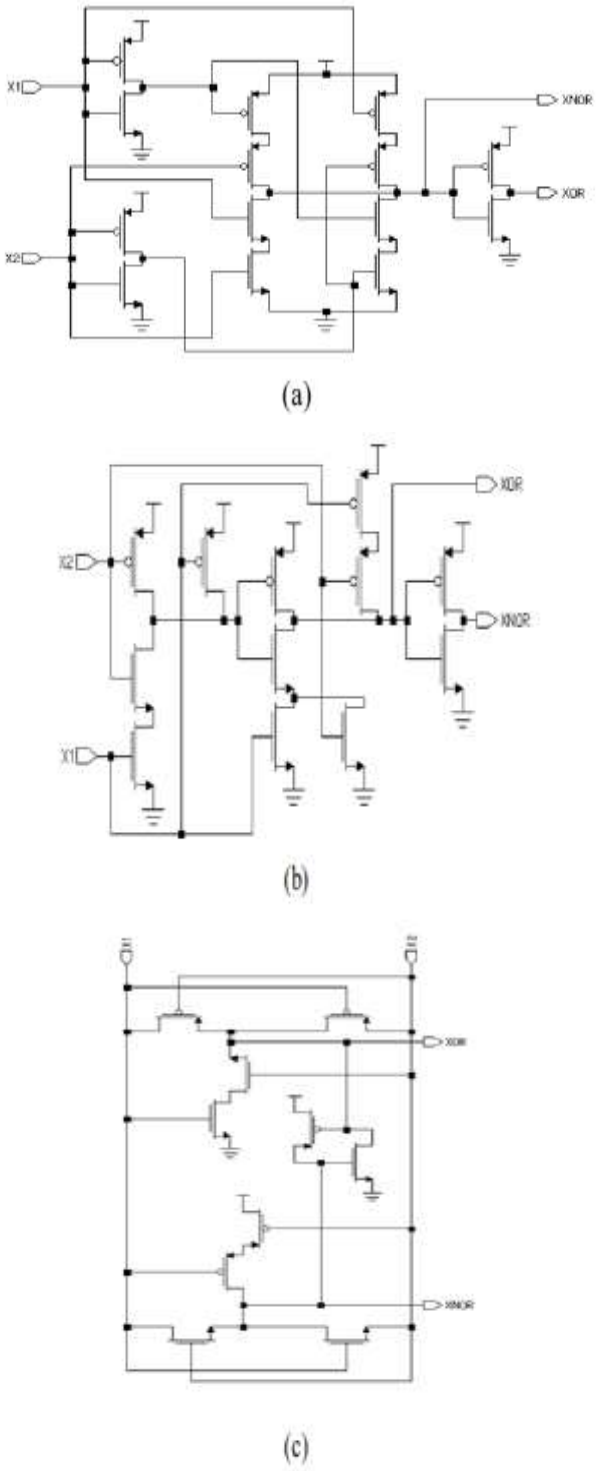
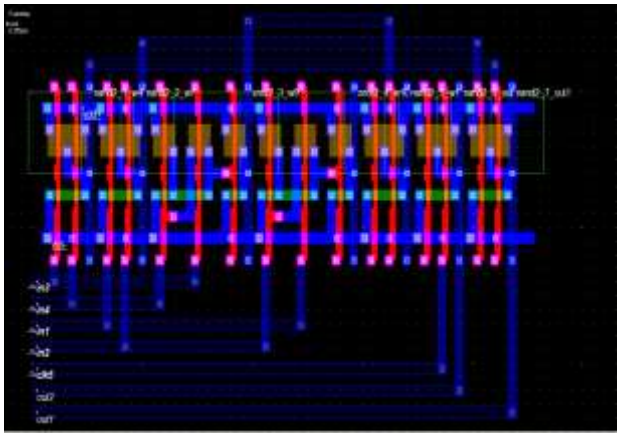
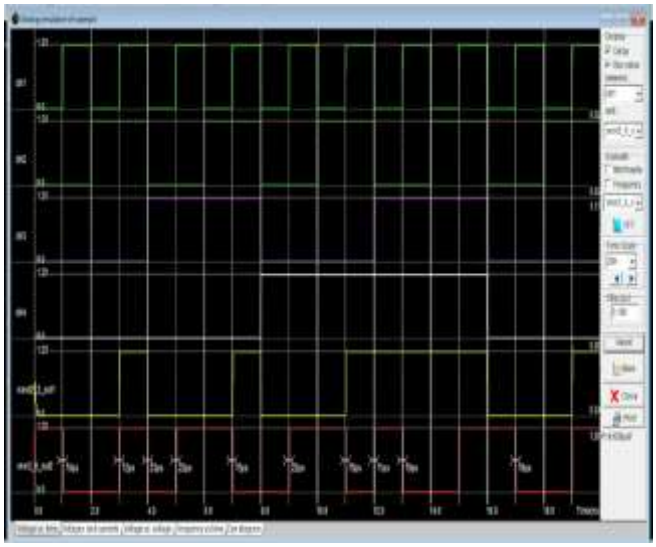
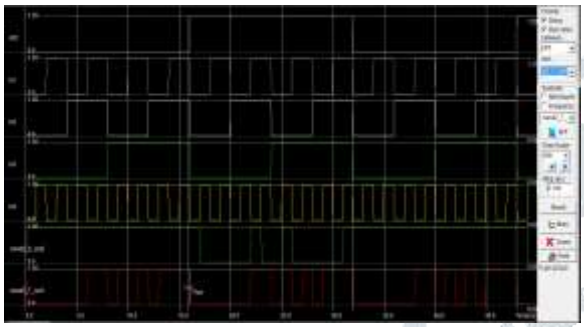


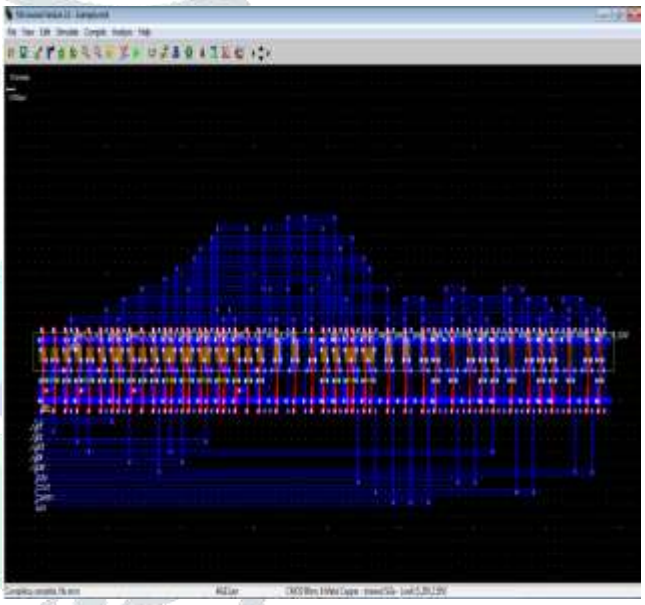
Fig: Different implementation of XOR-XNOR

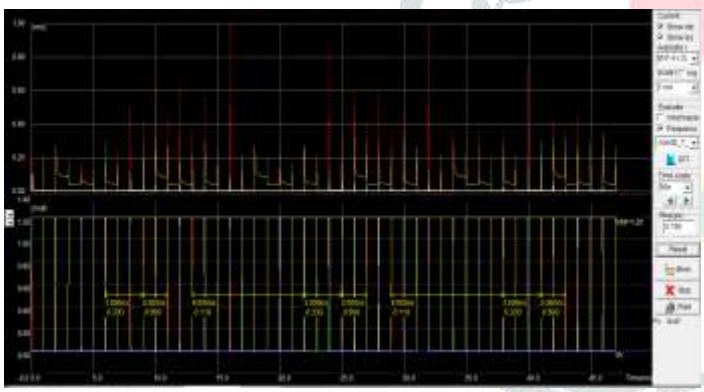
SIMULATION RESULTS:

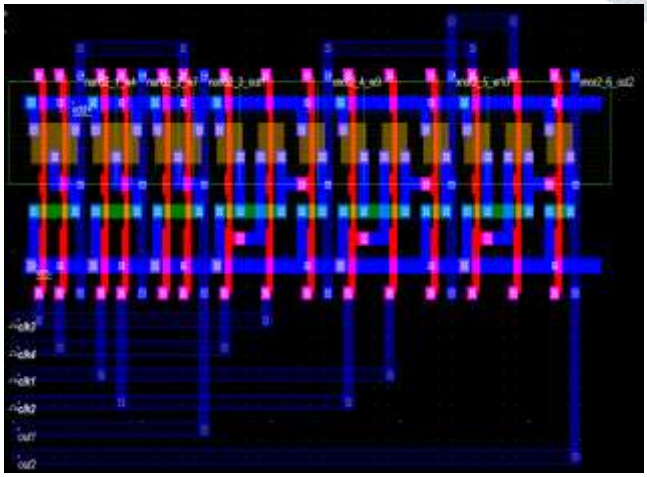


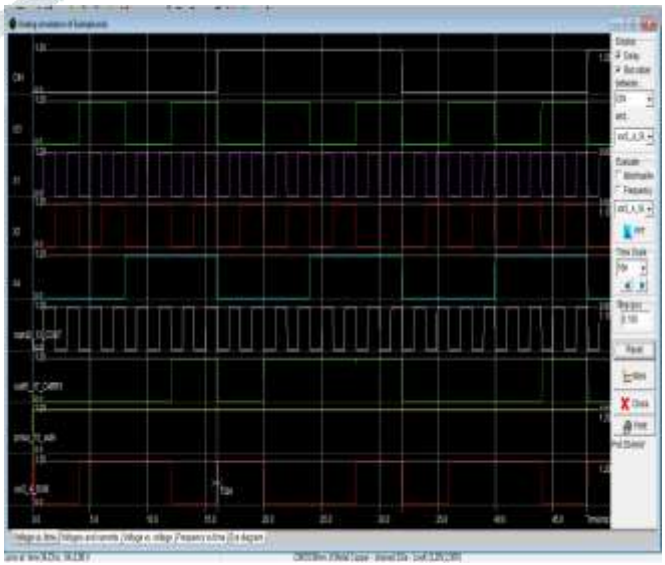


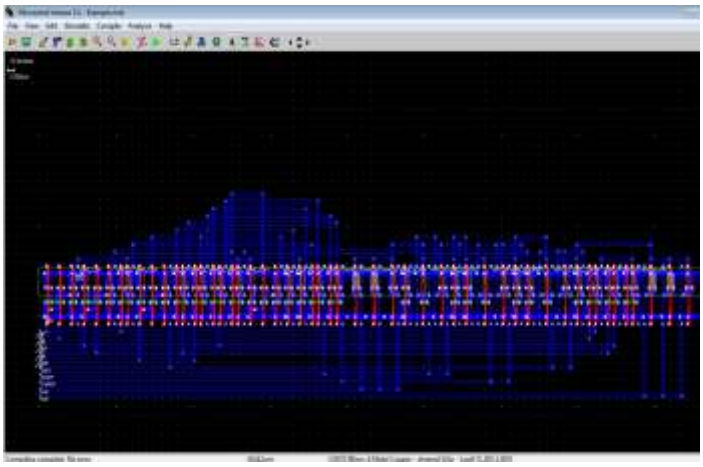












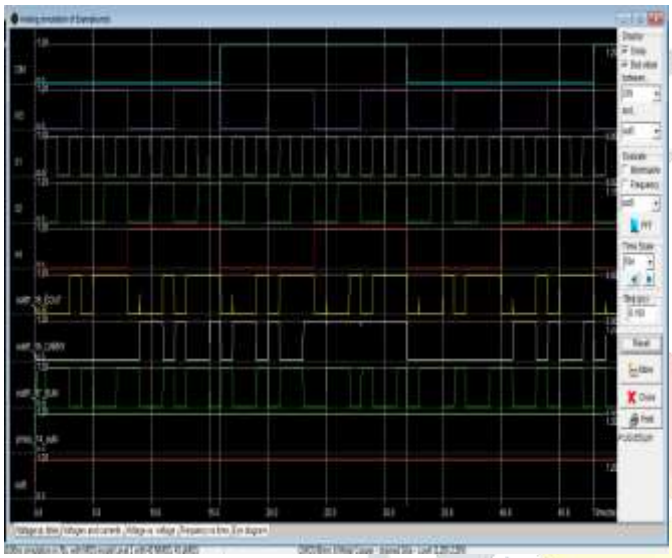


Fig. Input and output waveform for proposed 4-2 compressor circuit

CONCLUSION:

A 4-2 compressor circuit based on a new XOR-XNOR designed provide better performance. The proposed XORXNOR design shows power consumption. The XOR provide maximum output delay of and XNOR shows delay. The performance of this circuit have been compared to earlier reported circuits in terms of power consumption, maximum output delay. The proposed circuit result shows better performance than existing circuits in all aspect.

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