DESIGN AND ANALYSIS OF DOUBLE TAIL COMPARATOR FOR LOW VOLTAGE AND LOW POWER RELEVANCES

[1]Y.UMA DEVI, [2]NAVEEN RATHEE
[1]PG Scholar, Dept. of VLSI System Design, Bharat Institute of Engineering and Technology, Hyderabad, Telangana, India.
[2]Professor and Project Incharge in ECE Dept., Bharat Institute of Engineering and Technology, Hyderabad, Telangana, India.

Abstract: There is a need for high speed Analog to digital Convertors, ultra low power and area efficient circuits. Hence designing high speed comparators is more challenging, when supply is smaller i.e. in a given technology to achieve high speed larger transistors are required to compensate the reduction of supply voltage, which also mean that more due area and power is required. To improve the speed and delay the Dynamic regenerative comparators is used. In this paper, a double tail comparator is proposed and executed in tanner tool version 13.0 using S-EDIT. Its schematic and waveform is analysed and after analysis it is observed that from single tail to double tail comparator delay has been reduced by 26 ns i.e. 5 times although its power is increased to two fold. By changing the aspect ratio of transistors we can achieve less delay. Based on requirement one can opt for either high speed or low voltage circuits.

***Index Terms* – comparator, Speed, Power, Aspect ratio.**

I. INTRODUCTION

Comparators are the most important building blocks of analog and digital convertors, signal processing elements etc. A comparator circuit compares two voltages and outputs either 1 or 0 depending on the input. It is also used to check whether input has reached to predetermined level. It is necessary first to sample the input and then applied to a combination of comparators to determine the digital equivalent of analog signal.

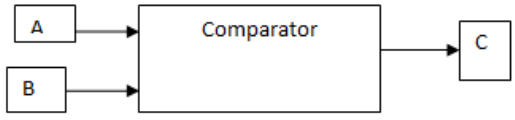

Fig: Comparator

High speed comparators in ultra-deep sub micrometre(UDSM) CMOS technology suffers from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at same phase as the supply voltage of the modern CMOS processes[1].Besides, many techniques such as supply boosting methods, techniques employing body driven transistors, current mode design and those using dual oxide processes, which can handle higher supply voltage, have been devolved to meet the low voltage design challenges[2][3].

Many versions of the comparator are proposed to achieve desirable output in submicron and deep sub-micron design technologies. The selection of particular technology depends upon requirement and application of design. In this project discusses about the low voltage and high speed design Comparator a double tail comparator is developed which has less delay.

High speed comparators use transistors with larger aspect ratio and hence consume more power. Depending on the application select comparator of either high speed or low power consumption. For example Nano- powered comparators in space saving chip scale packages(UCSP) are ideal for ultra-low-power, portable applications. Likewise if a comparator is needed to implement relaxation oscillator circuit to create a high speed signal then comparators having few Nano seconds of propagation delay may be suitable [4]

Differential amplifier cancels the common mode voltage i.e. offset voltage and also cancels noise generated by other elements in the circuit. Two types of noise are eliminated by differential amplifiers

1) Power supply noise 2) electromagnetic interference noise (EMI) Noise. If each stage has the same DC biasing then the output DC voltages of both stages are equal. If the AC input voltages are not equal, then the AC output voltages are not equal.

CMOS comparators are classified into 3 categories static, class AB and dynamic. The dynamic comparators are most power efficient which leads to selection of this comparator [4].

2. LITERATURE SURVEY

2.1 SINGLE TAIL COMPARATOR:

This are mainly used in A/D convertors, which has high input impedance, rail-to -rail output swing,aand no static power consumption the schematic diagram is shown in fig.

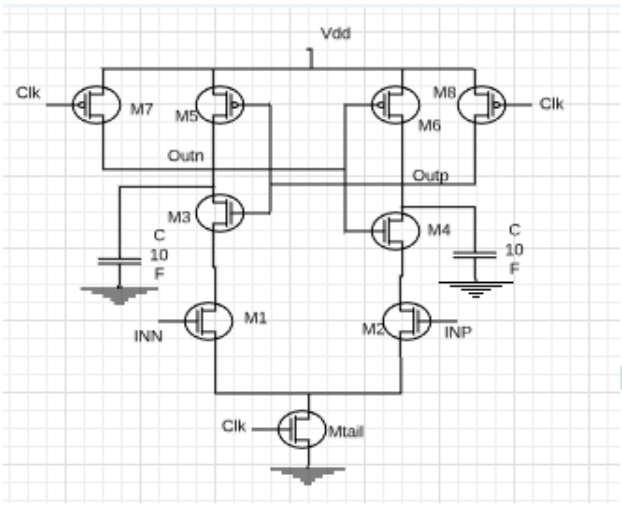

Fig: Single Tail Comparator

The operation of comparator is as follows. During reset phase Clk= 0 and M_{tail} is Off which in turn the reset transistors(M_7 ,M_8) pull both output nodes to V_{DD} which gives a valid logic during reset phase[5] .During decision making phase i.e. when Clk=V_{DD}, transistors M_7 and M_8 are off and Mtail is on. Output voltages(OUT_N, OUT_P) which are pre-charged to V_{DD} starts discharging depends on the input voltages(I_{NN},I_{NP}).If $V_{INP} > V_{INN}$, OUT_p discharges faster than OUT_N , hence when OUT_p falls down to V_{DD}-$|V_{thp}|$ before OUT_N, the corresponding PMOS transistor(M_5) will turn on makes latch regeneration caused by back -to- back inverters(M_3,M_5 and M_4,M_6) which makes OUT_N pulls to V_{DD} and OUT_p discharges to ground. If $V_{INP} < V_{INN}$,the circuit works vice versa[6-8].

For working of circuit all the transistors must work in saturation region .The two stages must take equal amount of current. The aspect ratio is calculated by taking L value 0.13 nm and V_{th}=0.43v by choosing I value as 20µA and μ_n, μ_p, C_{ox} values taken from 65nm technology file and supply voltage(V_{DD}) is taken as 1.2V and L value is taken as 130 nm for all the cases and calculate the W value by equation of

$$I_d=1/2\ \mu_n\ Cox\ (W/L)(V_{gs}-V_t)^2$$

Table: single tail comparator

Transistors	M_{TAIL}	M_1,M_2	M_3,M_4	M_5,M_6,M_7,M_8
VALUES (W)	1.46 µm	0.7 µm	0.7 µm	0.91 µm

2.2 DOUBLE TAIL COMPARATOR:

This topology has less stacking and therefore can operate at lower supply voltages compared to conventional dynamic comparator

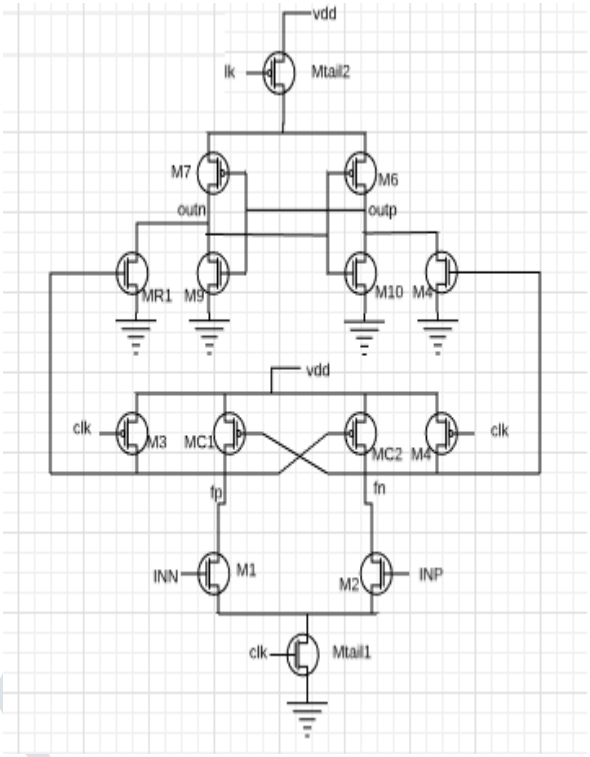

Fig: Double tail Comparator

OPERATION:

Reset Phase: when CLK is low, Mtail1 and Mtail2 are off,M3 and M4 pulls both fn and fp nodes to V_{DD} hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors M_{R1} and M_{R2} reset both latch outputs to ground [9-10].

Decision Making Phase: when clk is high, M_{Tail1} and M_{Tail2} are On, transistors M_3 and M_4 turn off. At the beginning of this phase the control transistors are still off since fn and fp are V_{DD}. Thus fn and fp starts with different discharging rates depending on input voltages .If $V_{INP}>V_{INN,}$ fn drops faster than fp. As fn continues falling, the corresponding PMOS control transistor Mc1 starts to turn On pulling fp node back to V_{DD}. The control transistor (Mc2) remains off allowing fn to be discharged completely [11] [12].

The values of transistors are calculated and tabulated. For the transistor to be on all must be in saturation region. The values are calculated W/L ratios are optimized by using 65 nm technology file [13].

Table: Double tail comparator

Transistors	M_{TAIL1}	M_{TAIL2}	M_1,M_2	M_3,M_{C1},M_{C2},M_4	M_6,M_7
VALUES(W)	2.67µm	6.7µm	1.3µm	1.7µm	3.3µm

3. PROPOSED COMPARATOR

The double tail comparator consists of two tail transistors which are used for fast switching purpose .The main idea of this proposed is to increase the speed by adding four nmos transistors in series to input transistors whose input voltage is differential voltage provided at the input and control transistors .The diagram of proposed is shown in the fig:

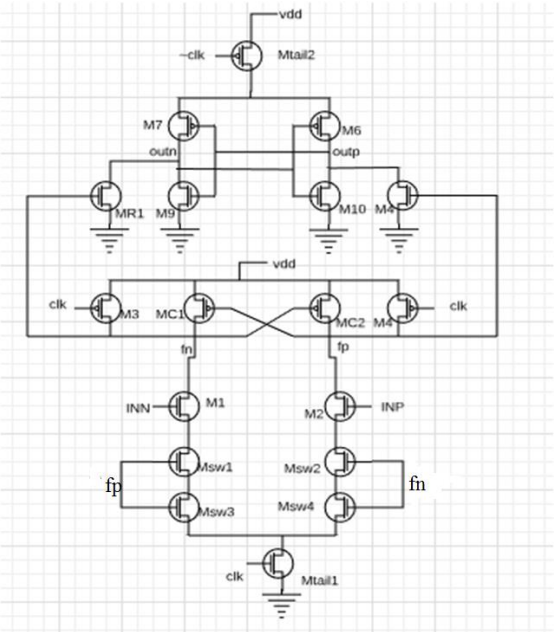

Fig: Proposed Double Tail Comparator

WORKING:

Reset Phase: when clk is low mtail1 and mtail2 are off to avoid static power m3 and m4 transistors pulls both fn and fp nodes to vdd. So mc1 and mc2 transistors are in cut-off therefore the transistors mR1 and mR2 reset both latch outputs to ground [1]

Decision –Making Phase: when clk is high, mtail1 and mtail2 are working, m3 and m4 are turn off. At the beginning the mc1 and mc2 transistors are turn off thus fn and fp starts to drop at different discharging rates according to input voltages .suppose Vinp>Vinn fn drops faster than fp. As long as fn continues falling, the corresponding pmos mc1 starts to turn on. Pulling fp node back to vdd. So mc2 remains off. In double tail comparator difference voltage of fn and fp is just a function of input transistor trans-conductance and input difference voltage

In proposed as soon as the comparator detects that one of the value of fn (or fp) is discharging faster, a pmos transistor mc1 (or mc2) turns on making other node back to vdd .there as time passing ,the difference voltage between fn and fp increases in an exponential manner ,lead to reduce of latch regeneration time[1].

When one of the control transistors (mc1 or mc2) turns on a current from supply is drawn to ground via input tail transistor. Two overcome this issue four nmos transistors are used below the input transistors. (msw1, msw2, msw3, msw4).At the beginning of decision making phase, the fact that the fn and fp nodes are charged before the same of supply voltage. During reset phase switches are closed and fn and fp start to drop with different discharging rates. As soon as comparator detects that one of the fn or fp is discharging faster, the control transistor will make to increase voltage difference. suppose fn is pulling up to vdd and fp should be discharged completely the switches in the charging path of fn opened and other switches connected to fn will be closed to allow the complete discharge of fp node.

For proper working of transistors equal current has to be flown for the two side of the circuit. To operate correctly all transistors must be in saturation region. The a aspect ratio i.e. W/L ratio is calculated by taking the I_d as 20ua and V_{th} as 0.43 v and u_n and u_p values taken from 65nm technology file. In case of analog circuit designing we have taken the double value of length we have to choose

The equation transistors to be saturation is

$$Id = \frac{1}{2} * \mu_n * C_{ox} * (Vgs - vt)^2$$

Table: Proposed Double Tail Comparator

Transistors	M_{TAIL1}	M_{TAIL2}	M_1,M_2,M_{sw1}, M_{sw2},M_{sw3}, M_{sw4}	M_3,M_{C1},M_{C2},M_4	M_{R1},M_9,M_{10},M_{R2}	M_6,M_7
VALUES(W)	2.67µm	6.7µm	1.3µm	1.7µm	0.6µm	3.3µm

RESULTS

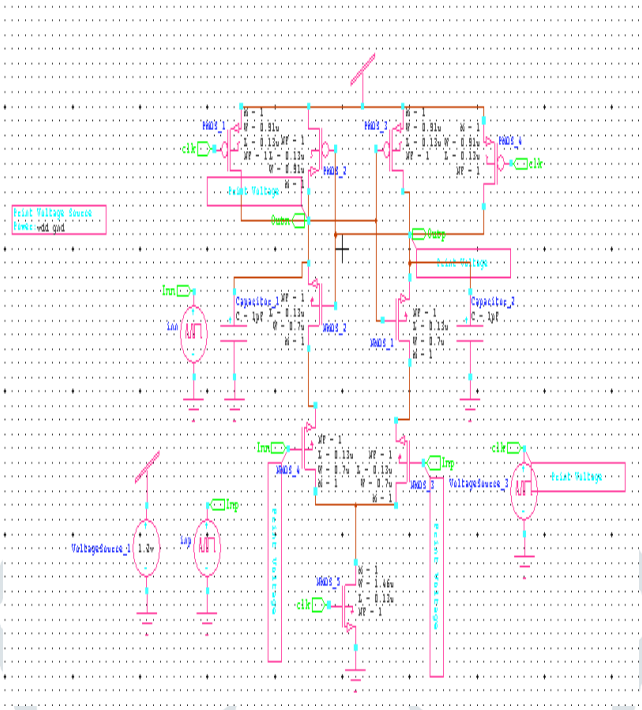

Fig Schematic of Single Tail Comparator

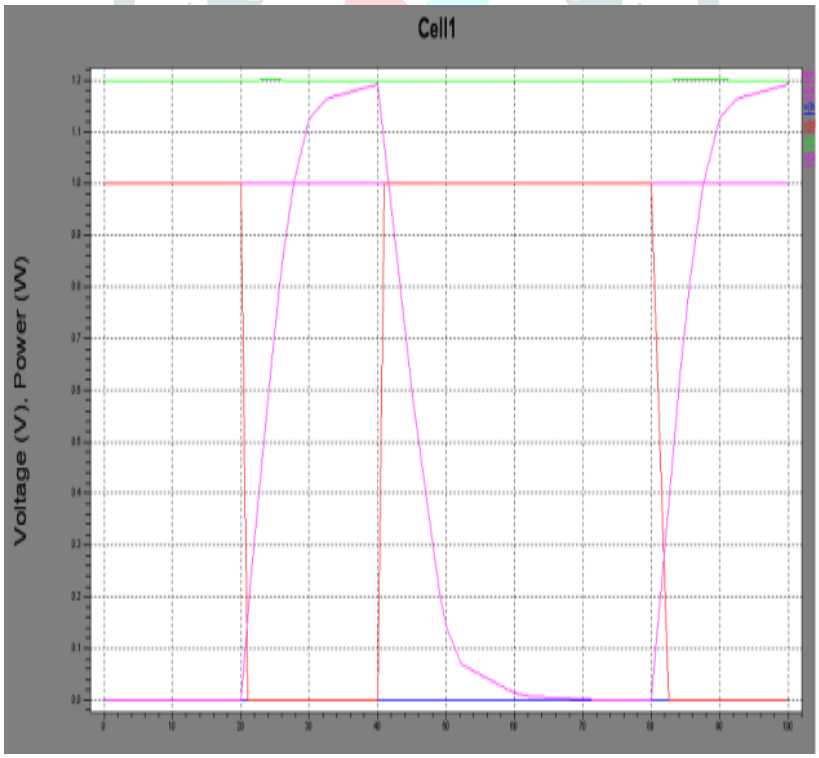

Fig Output of Single Tail Comparator

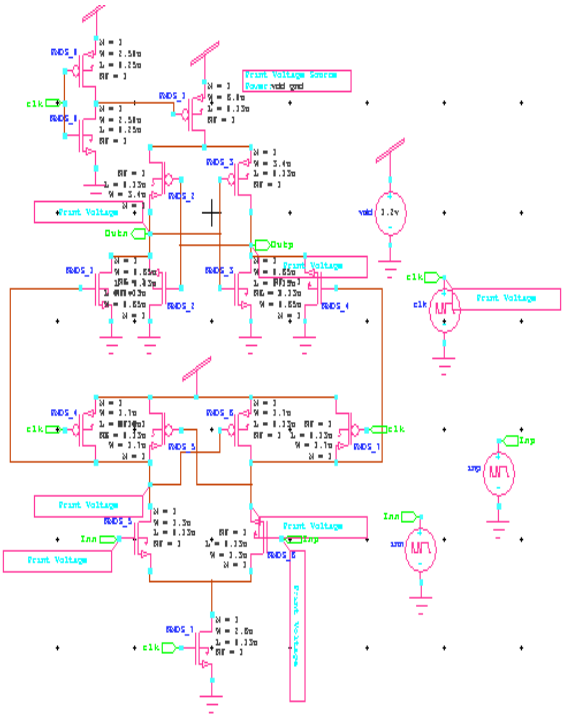

Fig Schematic of Double tail comparator Tail Comparator

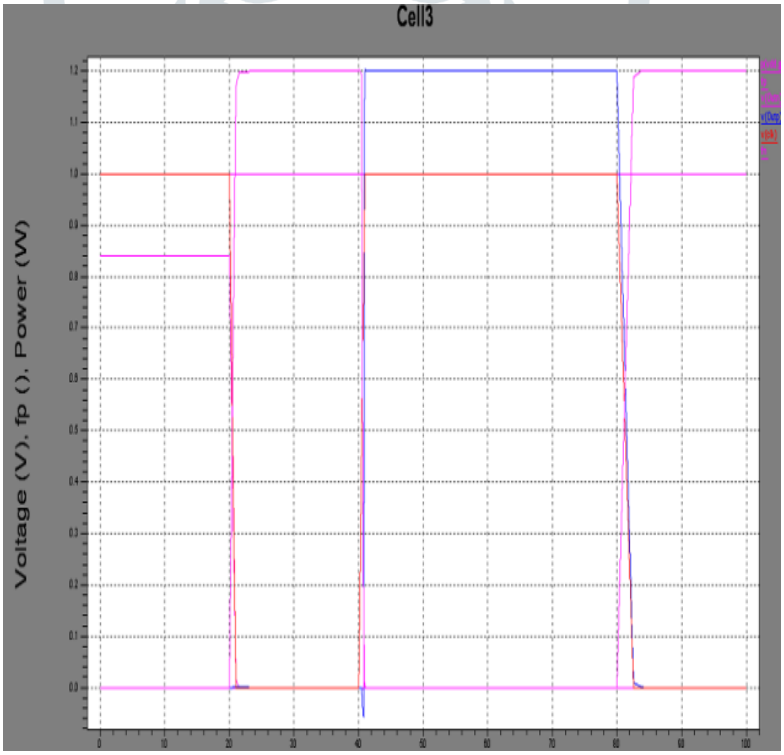

Fig Double Tail Comparator

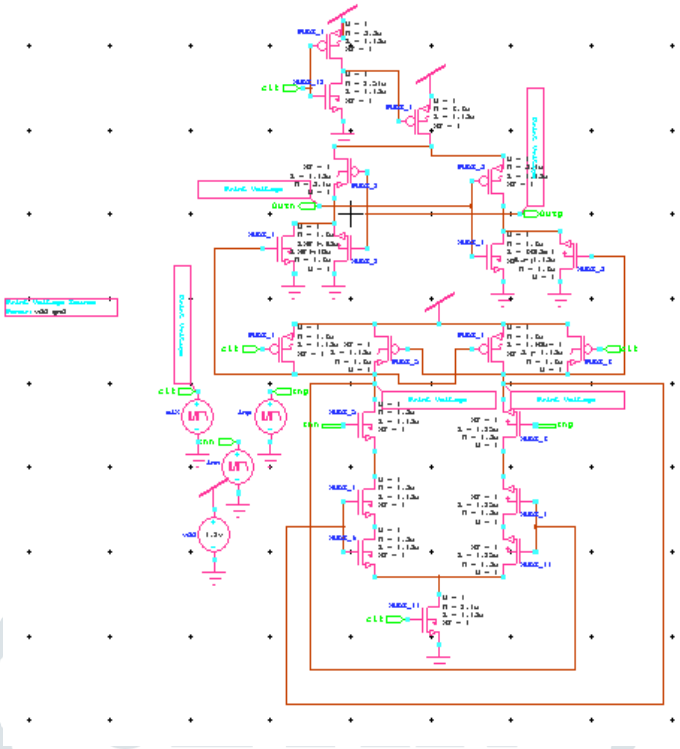

Fig Schematic of Proposed Double Tail Comparator

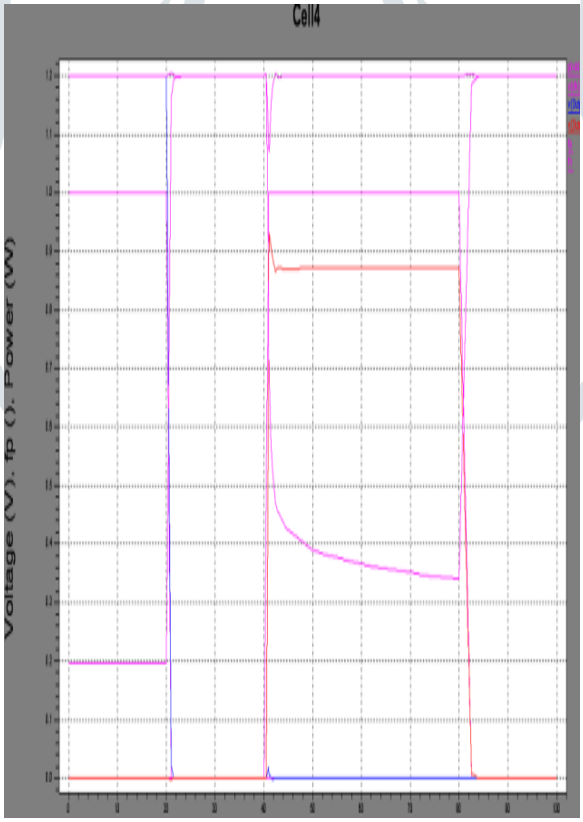

Fig Output of Proposed Double Tail Comparator

4. CONCLUSION:

Hence a double tail comparator is proposed and its schematic is seen, waveforms are observed, power and delay values are calculated by using tanner EDA tool version 13.0. It is observed that delay and power is reduced compared to previous circuits that are Single tail Comparator and Double Tail Comparator. Based up on requirement we have to choose for either high speed or less power consumption circuits

Table: Result

	Single tail comparator	Double tail comparator	Proposed double tail comparator
Power	33µm	68µw	66µm
Delay	30ns	26ns	4.9ns

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Author's Profiles:

Y.Uma Devi, student in Department of VLSI System Design, Bharat Institute of Engineering and Technology, India.

GUIDE DETAILS:

Prof. Naveen Rathee

With B.E (E&T), M.Tech (ECE), PhD (ECE) and hardcore Industrial experience of 08 years working as Project Manager in Bottling plant and Power Cable Industries and rich Academic experience of 15 years to his credit, presently spearheading the post of Professor and Project Incharge in the Department of Electronics and Communication Engineering at Bharat Institute of Engineering and Technology from 2017 onwards. His area of Interest includes Digital System Design, Embedded Systems Design, Reconfigurable FPGAs, and OFDM-MIMO Systems.

dean.sbit@gmail.com