ULTRA LOW POWER INVERTER USING SET

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Abstract: The current flowing through a set is due to tunneling of electrons through the junctions. As tunneling is random so magnitude of current flowing through a SET is also very small. So, drain and source voltage requirements are also very small. Due to these factors the power consumption of SET is ultra low. In this work, The SET inverter structure is reached which switches output from high to low when electron is added to input. Two complimentary biased SET are combined in a single circuit to create an inverter. Simulation script is used to short electrode of n-type and p-type SET using interconnects method.

KEYWORD: SINGLE ELECTRON TRANSISTOR (SET).

I. INTRODUCTION

The already-high and ever-improving performance of data processing devices has brought about an unfortunate side effect of rapidly expanding electric power consumption. In this age of concern for the earth's environment, one of the major problems to overcome in realizing a full-fledged multimedia society is that of achieving both lower power consumption and higher performance in such devices.

Single-electron devices with their ultra-low power consumption are one means of addressing this issue. Since control in these devices is obtained literally by utilizing the behavior of a single electron, device size and power consumption are but a fraction of those in conventional devices. As a result, they are attracting considerable attention as devices for use in the ultra-large-scale, ultra-low-power-consumption integrated circuits of the future.

Application is the basic aim behind the fabrication of a device .In this work an inverter is designed and simulated. The inverter is a basic building block in digital electronics. Multiplexers, decoders, state machines, and other sophisticated digital devices may use inverters. The inverter designed with SET will dissipate very small power so can be used at different levels. The design flexibility is provided by low power dissipation for circuit level design.

II. INVERTER STRUCTURE

Structure has been designed using Visual TCAD. An n-type SET is combined with a p-type SET. The oxide is used to isolate the device with each other. have been designed with small dimensions of few nanometers using semiconductors, metals and individual molecules. It made up of a tiny conducting island which is coupled with source and drain guided by tunnel junctions and coupled capacitively to gates. The n-type device is fabricated on p-type, separated by oxide layer called Silicon On insulator wafer of length 10nm. Si quantum dot of size .5*1.6nm2 is used between gate and island. The device structure is shown in table 2.1:

Region	**Substrate**	**Buried Oxide**	**Gate**	**Spacers**	**Source/Drain**	**Channel**	**Si quantum dot**
Materials Used	Silicon with boron doping	Silicon di oxide	Poly Silicon	Silicon Nitride	Silicon with Phosphorous Doping	Silicon with boron doping	Silicon
Doping Concentratio	$1e^{+15}$	-	-	-	$1e^{+19}$	$1e^{+17}$	-

n							
Dimensions	$10\times7nm^2$	$10\times2\ nm^2$	$2\times1\ nm^2$	$2\times4\ nm^2$	$4\times1\ nm^2$	$2\times0.3\ nm^2$	$.5\times1.6\ nm^2$

Table 2.1 n-type device structure.

The p-type device dimensions are same. The doping levels are changed. Source and drain are doped with acceptor impurity boron with increased doping concentration of $1e^{+20}$. Substrate and channel doping is changed but concentration remains same.

Figure 2.1 2-D view of inverter

Figure 2.1 shows the two dimensional view of inverter .In figure 2.2 dimensions of both the devices is represented.

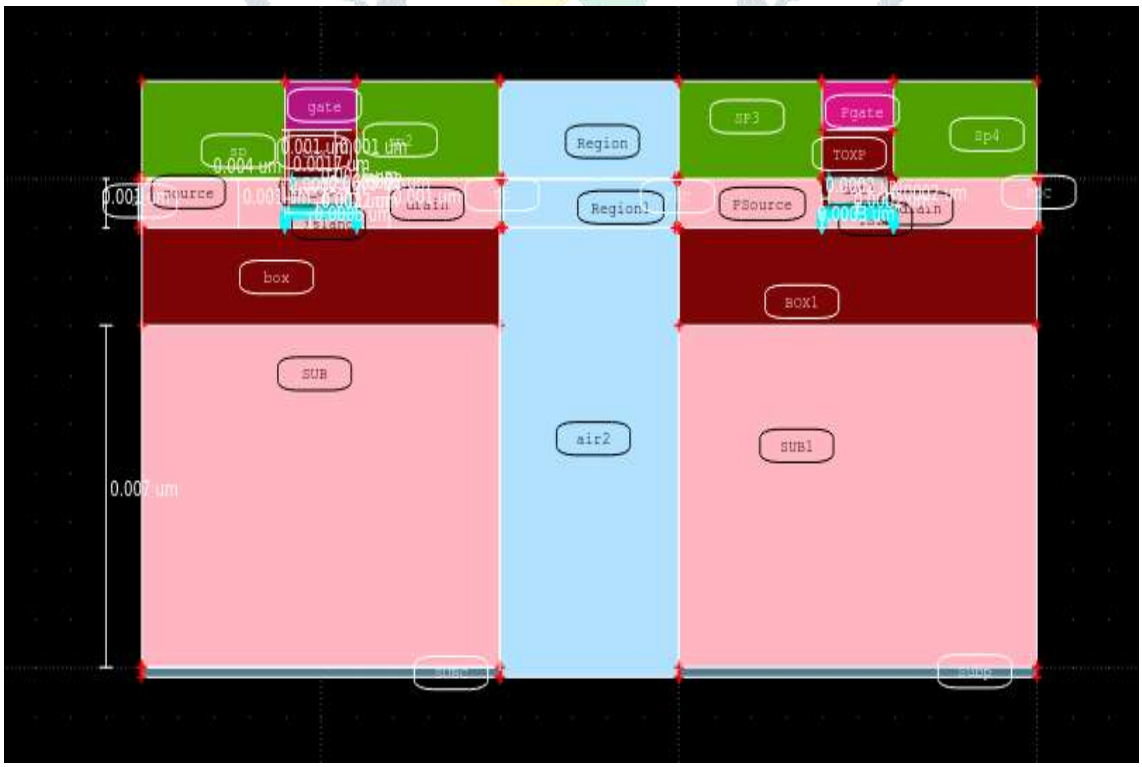

Figure 2.2 Inverter Dimensions

III. Numerical Simulation of Inverter

The numerical simulation of inverter is performed using numerical simulator Genius.

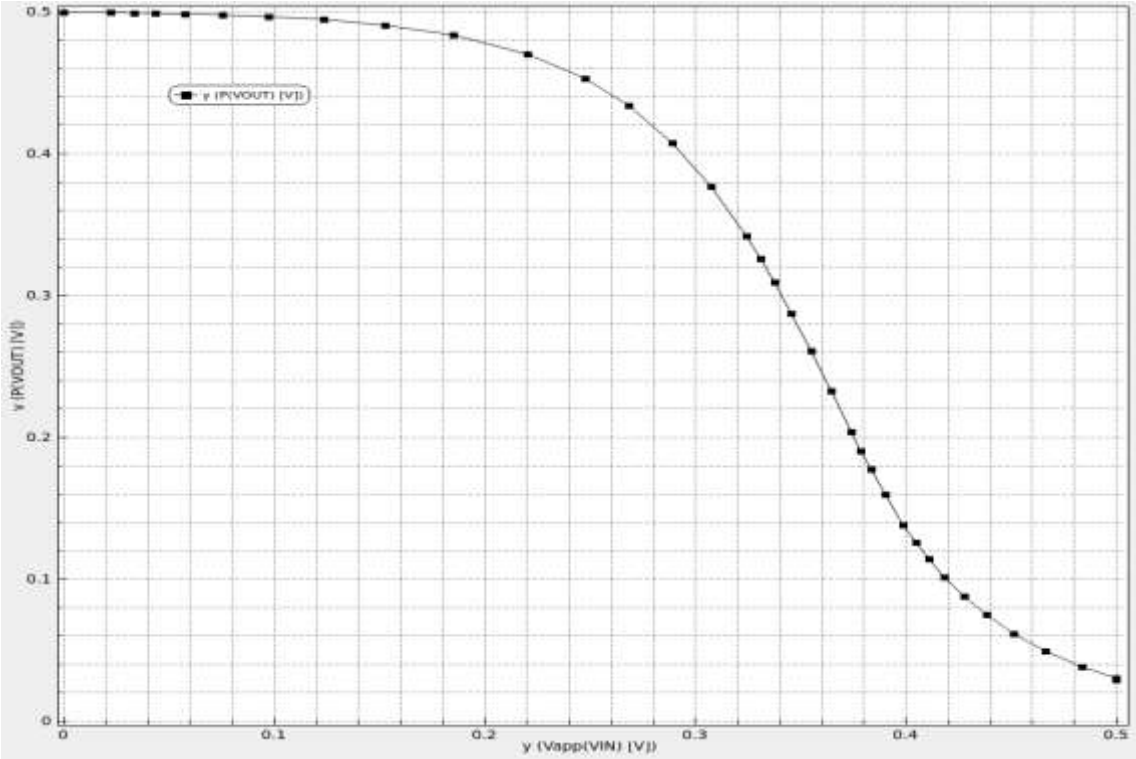

Figure 3.1 Voltage transfer characteristic of inverter

Inverter quality is often measured using the voltage transfer curve (VTC), which is a plot of output vs. input voltage. Figure 3.1 shows Voltage transfer characteristic of inverter.

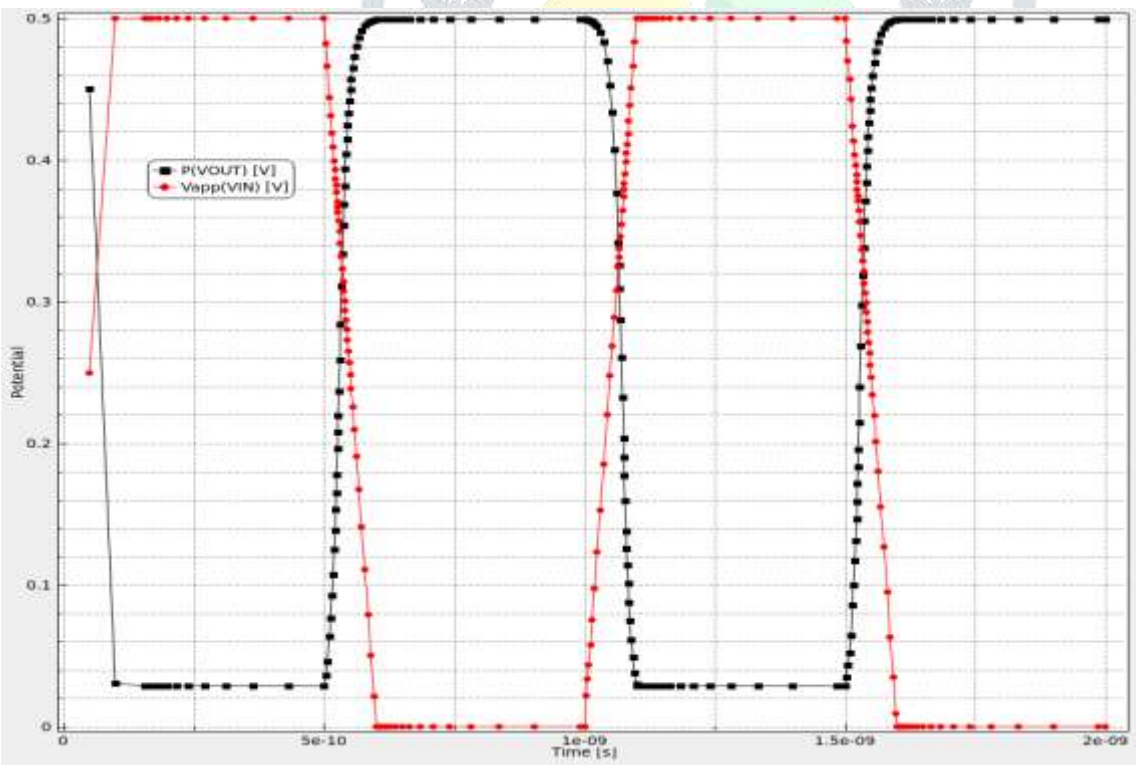

Figure 3.2 Transient characteristics of inverter

Transient response of inverter is shown in figure 3.2. It shows how output changes when input changes with time.

It is clear from figure that when output becomes high input becomes low and vice-versa.

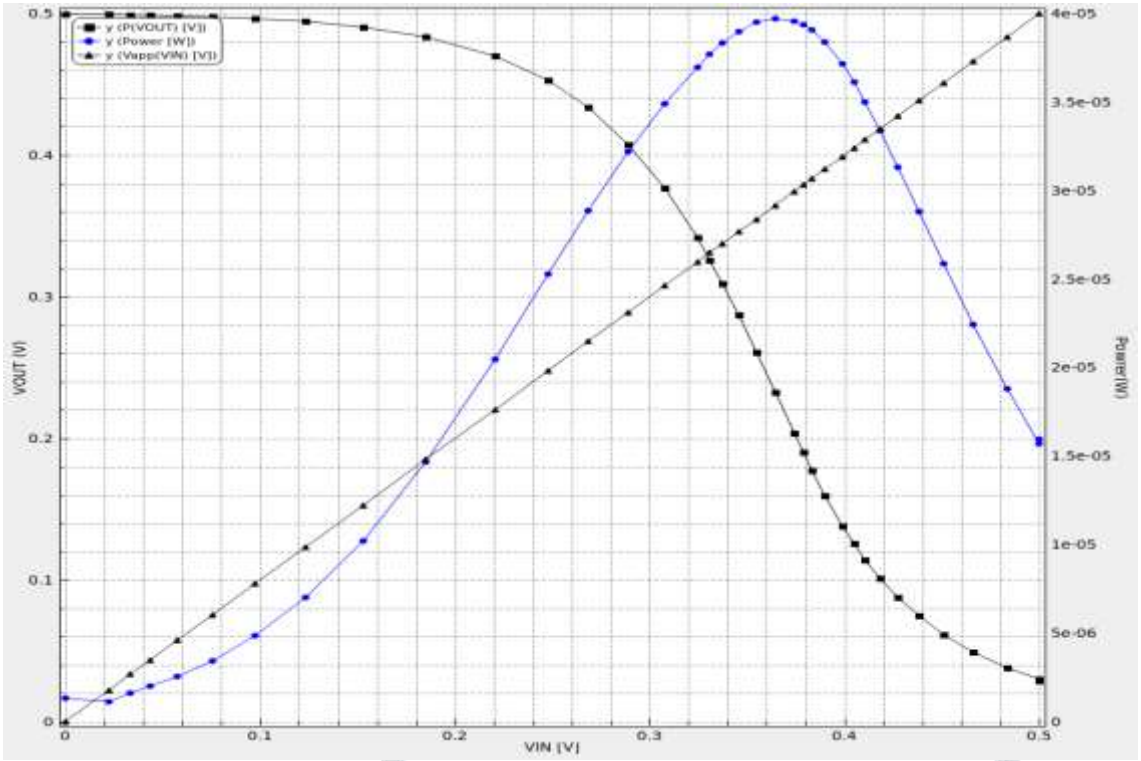

Figure 3.3 DC characteristic of inverter power

Figure 3.3 shows the DC characteristic of dissipation of power. While figure 3.4 shows the transient response of power dissipation. It is clear that maximum power consumption occurs when input is maximum or output is maximum.

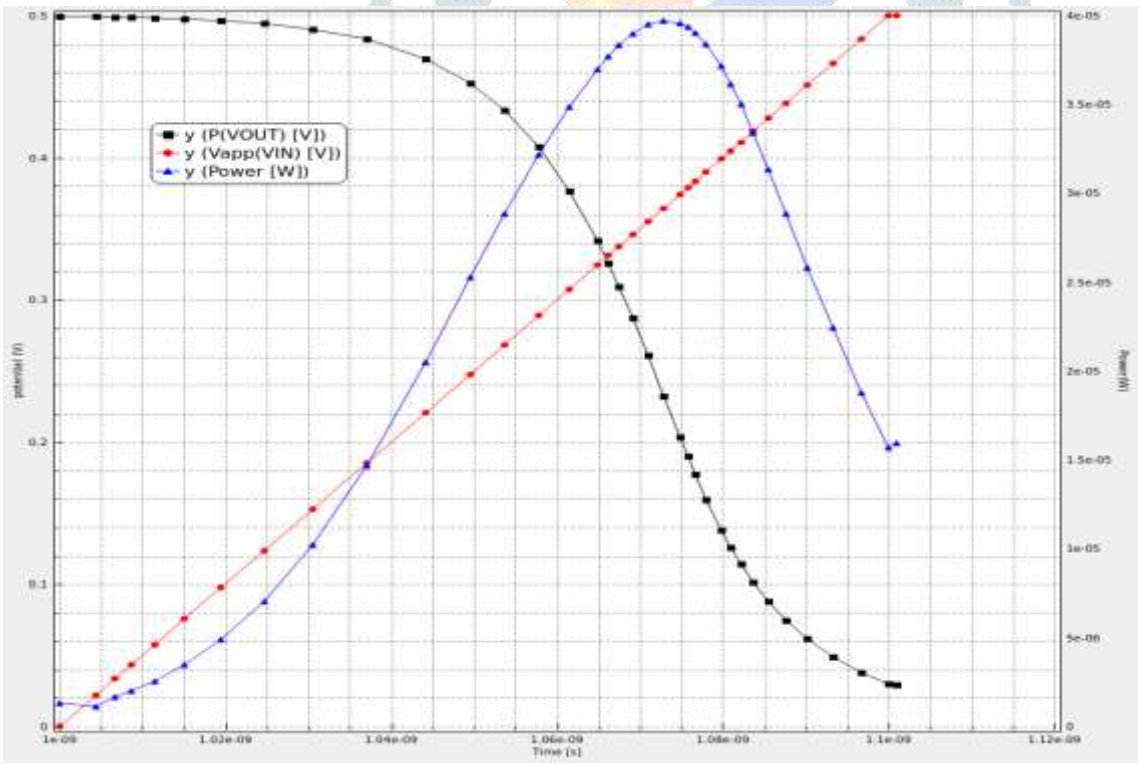

Figure 3.4 Transient power characteristic

IV. **Conclusion**

In this paper, the design and simulation of an inverter circuit is presented. An inverter is fabricated using Visual TCAD and Simulated using genius simulator. The output of inverter is verified. As power consumption of SET is very low so inverter power dissipation is also very small. Inverter is basic building block of all the logic circuits, so other logic gates and circuits can be designed using this inverter. The simulation is performed at room temperature so it can work on room temperature.

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