# A NEW TOPOLOGY ON MULTILEVEL INVERTERS WITH REDUCED NUMBER OF SWITCHES

Ahalya R
PG Student
Department of Electrical and Electronics Engineering
PRIST University, Thanjavur, India

***Abstract:*** The Multilevel inverters have been deliberated for an increasing number of application due to their high power capability. This paper discusses about a multilevel inverter topology with reduced number of switches. Switching losses can be reduced by this topology. And reduction of switches also reduces the cost. Multilevel inverters are used in industry for medium and high voltage application. The main disadvantage of this multilevel inverter is that it require complex gate driving circuit.

***Index Terms*** **– Multilevel inverter, power electronic switches, topology.**

## I. INTRODUCTION

The principle behind the multilevel inverter is to achieve a high power using series connected semiconductor switches i.e. IGBT, MOSFET etc. with the separate dc sources which helps in conversion of power from dc to ac. The output ac is in the form of staircase manner which should be nearer to sinusoidal waveform and to obtain this, proper switching angles should be generated using optimizing techniques to control switching frequencies of each semiconductor switches connected. The primary structure of MLI have been designed to obtain high power range utilizing multiple dc voltage levels, so that it can be useful for high operating voltage electrical systems. Use of transformer is not needed, which can put a pause to design of MLI because of its cost-maintenance and low distortion i.e. output containing low harmonics can be obtained. Hence the topology is most suitable for FACTS devices and many high power application systems.

Multilevel inverter are mainly used to obtain ac voltage from several dc voltages, so it can be used in integration with the renewable energy sources like fuel cells, photovoltaic cells etc. MLI"s are also best suitable for applications like VAR compensation, selective harmonic filtering, drives application etc. The integration of MLI with renewable energy sources will be advantageous because of its availability, faster response, and self-controlling capability. The real and reactive power flow can be controlled from the renewable energy sources which are a very attractive feature for low power quality problems.

MLIs are mainly classified into three types i.e. (a) Cascaded H-Bridge type which can be series or parallel connected and more advantageous to use than other topologies. (b) Diode clamped type which provides different voltage levels by connecting series bank capacitors and the number of levels that are being limited to three levels because of the voltage balancing issues. The main disadvantage of using this topology is the use of more number of diodes. (c) Flying capacitor type which is designed by series connection of capacitor clamped switching cells and disadvantageous to use because of the more number of use of capacitors.

Multilevel inverter helps in synthesizing desired staircase output voltage waveform from several dc sources used as input for the multilevel inverter. Increase in the number of dc source leads closer to the pure sinusoidal voltage waveform.

## II. PROPOSED TOPOLOGY ON MULTILEVEL INVERTER

The proposed topology is modeled in order to reduce the number of switches and dc sources to get the increased output levels. Here the Thirteen level inverter with asymmetric sources is modeled to verify its efficiency and working.

The proposed model for thirteen level inverter consists of ten switches and three asymmetric dc sources. The switches from S1 to S6 contributes towards the level increment whereas the switches from S7 to S10 aids in achieving positive and negative halves.

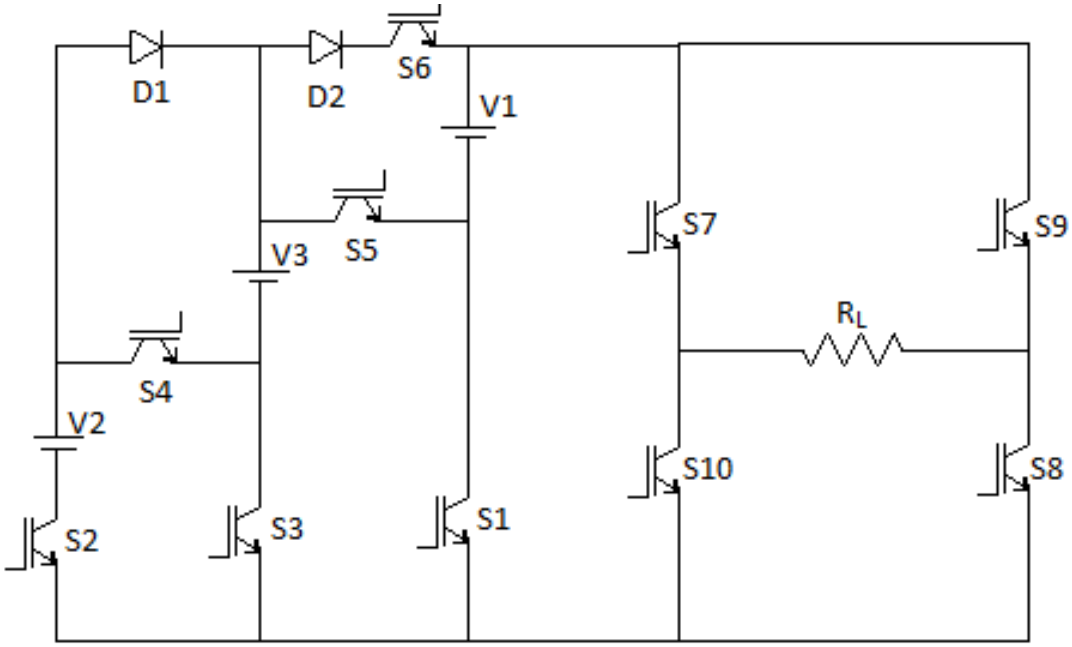


Fig1: Thirteen Level Inverter Topology

## III. MODES OF OPERATION

MODE 1:

In mode1 the switch s1 is turned on to produce v1 voltage across the load.

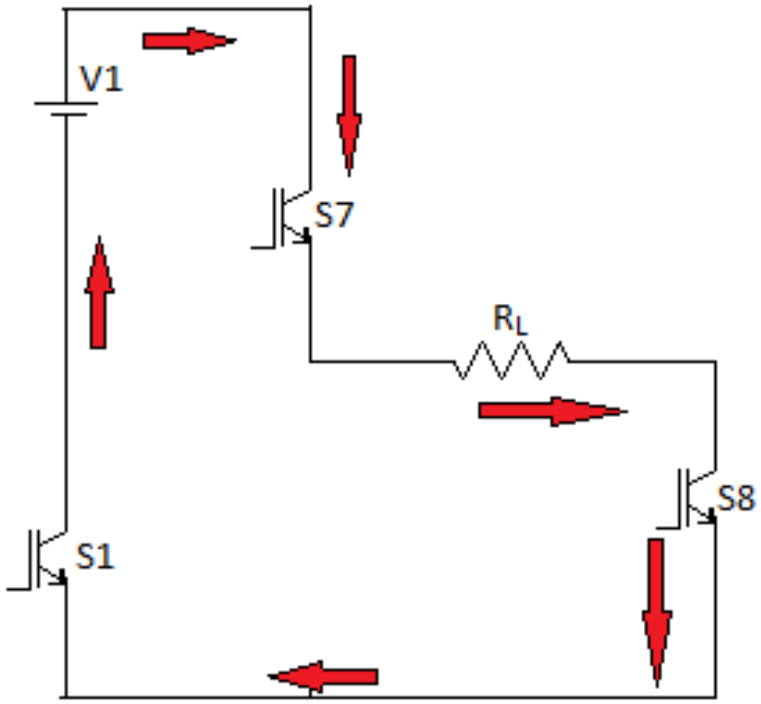


Fig2: Mode 1

MODE 2:

In Mode2 the switches S2 and S6 are turned on to produce V2 voltage across the load.

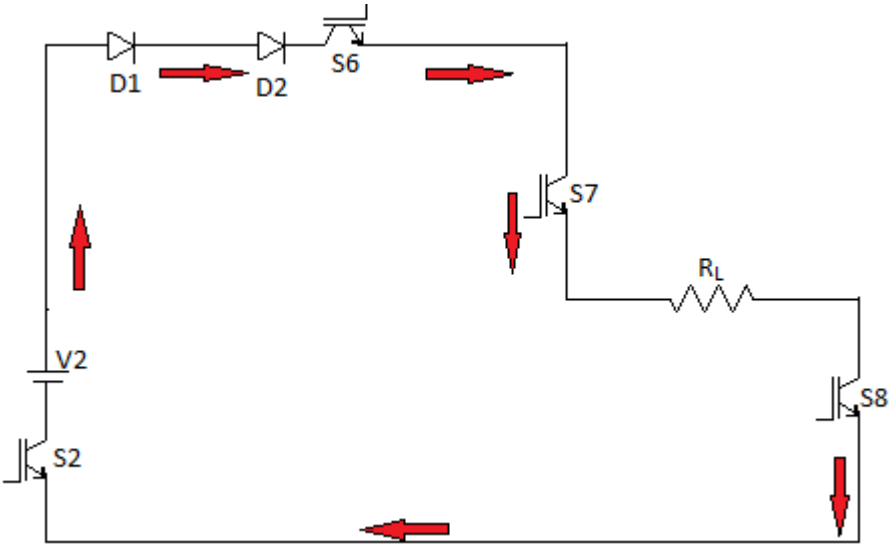


Fig3: Mode 2

MODE 3:

In Mode3 the switches S3 and S6 are turned on and Diode D2 conducts to produce V3 voltage across the load.

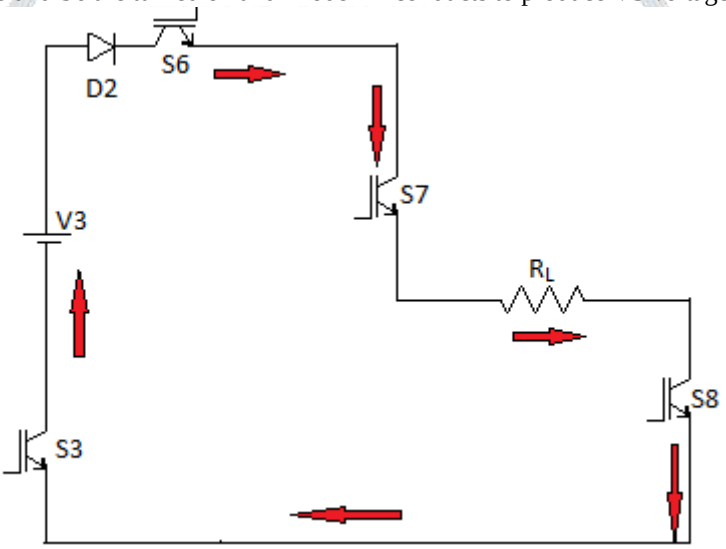


Fig4: Mode 3

MODE 4:

In Mode4 the switches S3 and S5 are turned on to produce V4= (V1+V3) voltage across the load.

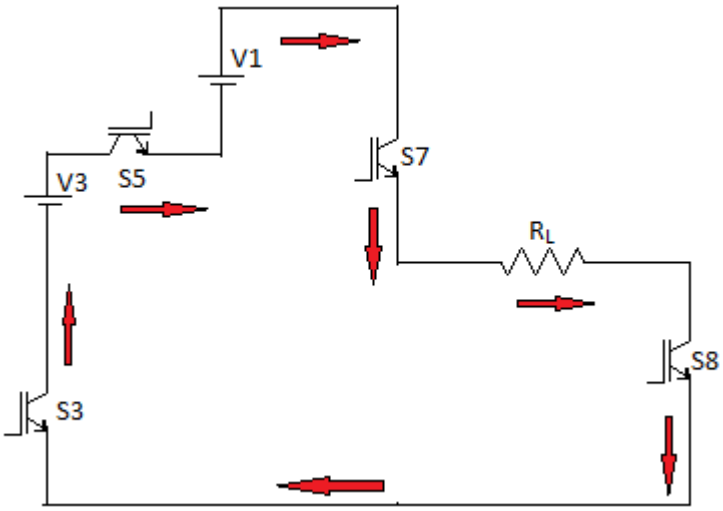


Fig5: Mode 4

MODE 5:

In mode5 the switches S2, S4 and S6 are turned on and Diode D2 Conducts to produce V5= (V2+V3) voltage across the load.

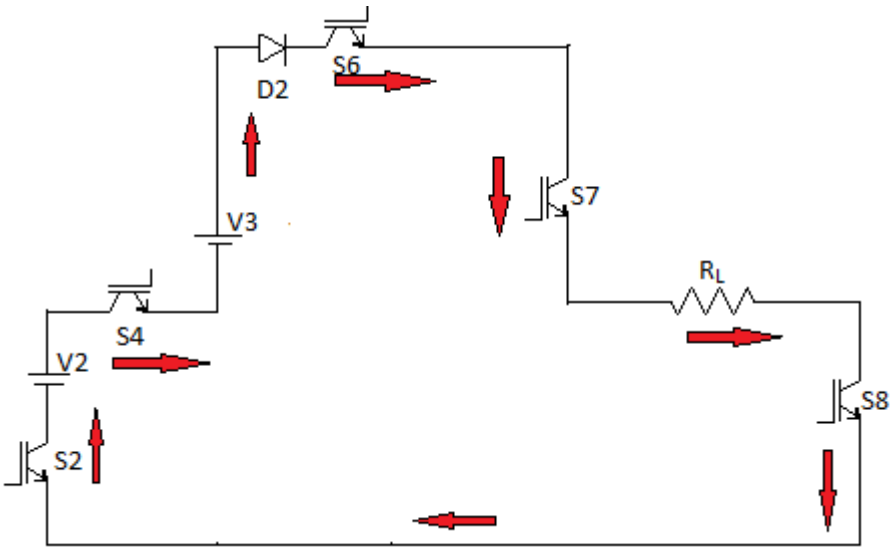


Fig6: Mode 5

MODE 6:

In mode6 the switches S2, S4 and S5 are turned on to produce V6= (V1+V2+V3) voltage across the load.

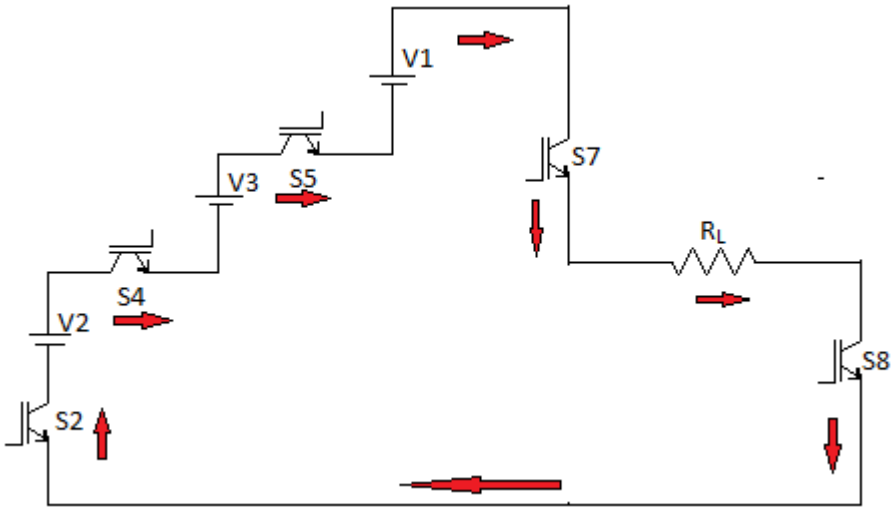


Fig7: Mode 6

The positive voltage levels are obtained by turning on S7 and S8 switches.

The negative voltage levels are obtained by turning on S9 and S10 switches.

Thus totally 0v, V1, V2, V3, (V1+V3), (V2+V3), (V1+V2+V3), -V1, -V2, -V3, - (V1+V3), - (V2+V3), - (V1+V2+V3) voltage levels are obtained at the output.

TABLE 1: Switching Table

| OUTPUT VOLTAGES | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 |
|---|---|---|---|---|---|---|---|---|---|---|
| V1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| V2 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| V3 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| V4= (V1+V3) | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| V5= (V2+V3) | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| V6= (V1+V2+V3) | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -V1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| -V2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| -V3 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| -V4 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| -V5 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| -V6 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

## IV. SIMULATION RESULTS

The simulation of the proposed Thirteen level Inverter is simulated using MATLAB Simulink software.

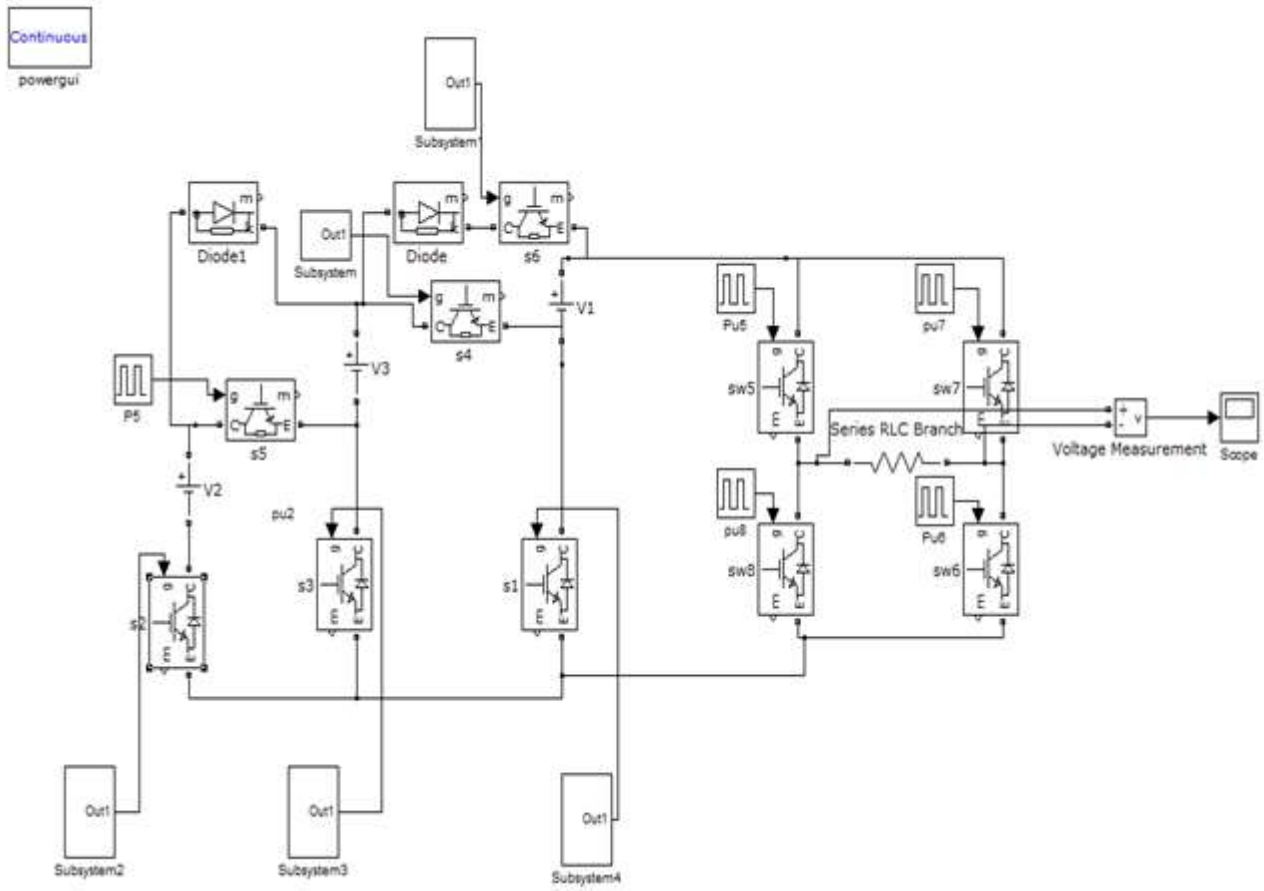


Fig 8: Circuit diagram in MATLAB Simulink

The Output voltage of the proposed thirteen level inverter is in following figure.

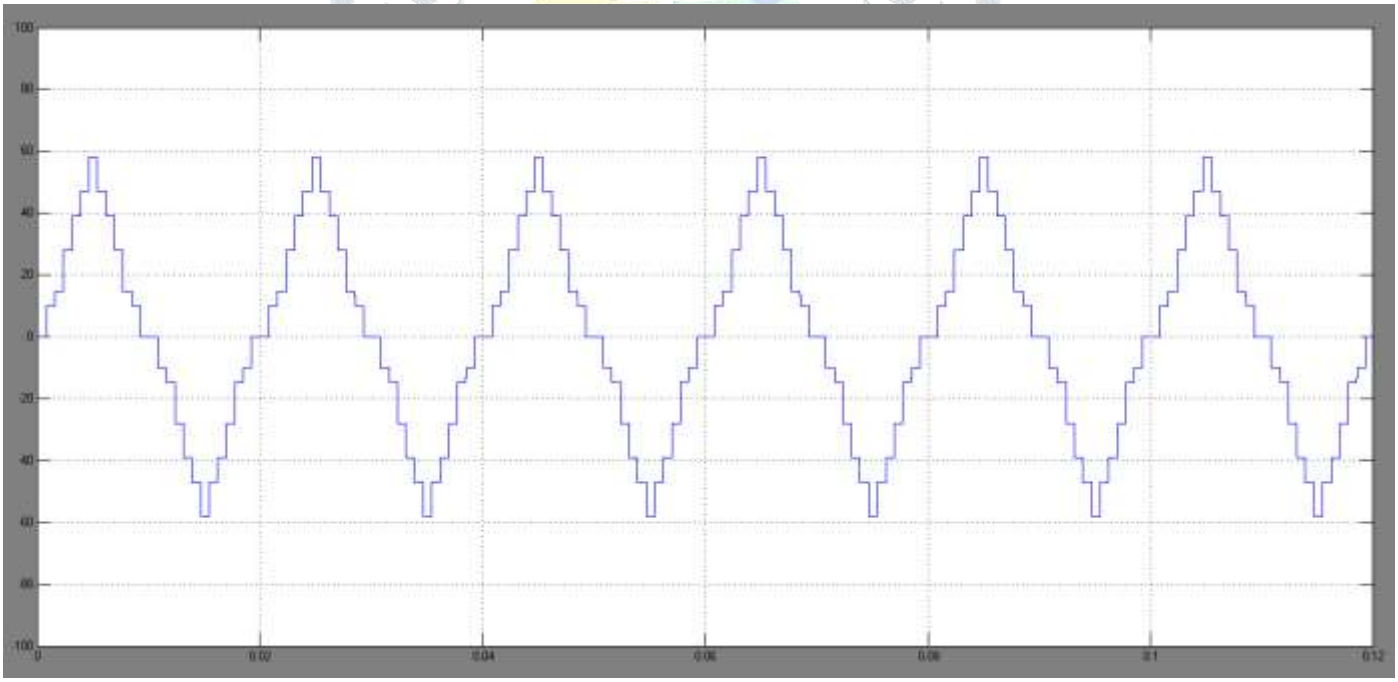

Fig 9: Waveform of output voltage

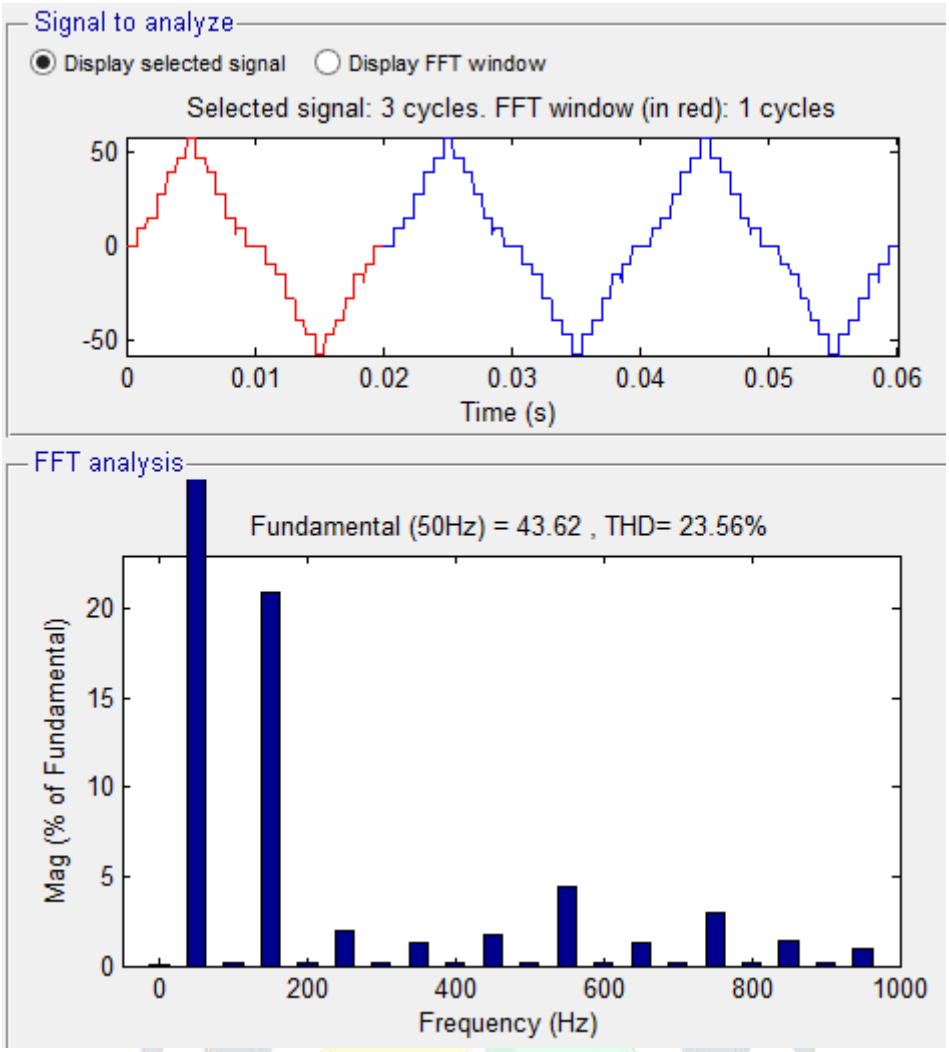


Fig 10: FFT Analysis of the output voltage (without filter)

TABLE 2. COMPARISON OF NUMBER OF PARAMETERS AMONG VARIOUS TOPOLOGIES OF THIRTEEN LEVEL INVERTER

| Parameters | Diode clamped | Capacitor clamped | Cascaded H-Bridge | Proposed model |
|---|---|---|---|---|
| **Switches** | **24** | **24** | **24** | **10** |
| **Clamping diodes** | **132** | **0** | **0** | **2** |
| **Balancing capacitors** | **0** | **66** | **0** | **0** |

## V. CONCLUSION

The new proposed model of the multilevel inverter is modeled and its working is analyzed. The topology proposed in this paper is also compared with the conventional topologies and it is found that the number of switches are reduced than that from the conventional and pre-proposed topologies.

The simulation results are also produced to showcase the success of the proposed topology. The output waveform is the stepped waveform with 13 levels. As a result, the switching loss is significantly reduced. All the merits and the feasibility of the pro-posed topology are evaluated by the simulation software and their results illustrate that the proposed inverter is a preferable topology to implement PV power sources and etc.

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