Design and Simulation of 2:1 MUX using Various CMOS logic at different level of Technology

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Abstract

In this paper, we demonstrate a low power high speed 2:1 MUX design using a Static CMOS logic and Pseudo NMOS logic at 180nm, 90nm and 45nm a technology. In order to suppress the degradation of signals and to increase the operation speed, we designed interconnection for the circuit; the implementation is done in VLSI technology as it has features like small size, low cost, high operating speed and low power. The circuit shows rise and fall times of about 1ns and consumes low power according to the design and number of transistor used in the circuits. The static CMOS logic and pseudo NMOS logic based 2:1 MUX is the most efficient design because the average power consumption is low and reduced leakage current. The designed circuits is realized in a standard 180nm, 90nm and 45nm process technology and uses 1.8V, 0.7V and 0.7V supply voltage. Our optimization circuitry using the proposed method reduces power consumption and leakage current by significant amount of multiplexer circuit.

Key Words: MUX, Pseudo NMOS logic Low Power, Static CMOS logic, Pseudo NMOS logic Low Power, Leakage Current, Cadence.

1. Introduction

SERIAL DATA communication frameworks are working at throughputs up to 0.4 TB/s have been connected to expand the transmission limit. As of not long ago, correspondences integrated circuits (ICs) working at such high speeds have required the utilization of specific rapid advances, for example, GaAs, InP, or SiGe [1]– [2]. Forceful innovation scaling in CMOS forms, nonetheless, over these compound semiconductor advances get various points of interest. In spite of all these advantages, one key apprehension, namely lower unity-gain frequency, for use in high-speed IC design makes CMOS typically demanding. Many bandwidth enhancement techniques have been developed to push the operating speed of CMOS circuits near the unity-gain frequency maximum value. Recently, numerous researchers have designed diverse building blocks of a 40-Gb/s transceiver in CMOS technology. In a 120-nm CMOS innovation a 40-Gb/s half-rate 2:1 multiplexer (MUX) and 1:2 de-multiplexer (DEMUX) joining shunt and arrangement inductive cresting were planned and created [3]. In [4], a 0.18-m CMOS process a 40-Gb/s enhancer and electrostatic release (ESD) insurance circuit was executed, including shunt and arrangement topping. All the more as of late, a 40-Gb/s handset in 0.13-m CMOS was accounted for in [5]. MUX is an information selector that chooses one of a few simple or advanced info flags and advances the chose contribution to a solitary yield line. A multiplexer of two i/p has n such select lines, those are required to pick which i/p line to deliver to the yield [6].2:1 MUX is an essential square of the "switch logic" [7].It has

two information lines An and B, one select line S and one yield solitary Y[8] as appeared in Fig 1. Reality table of 2:1 MUX is given in Table; the logic work is

$$Y = \sim s.A + s.B$$

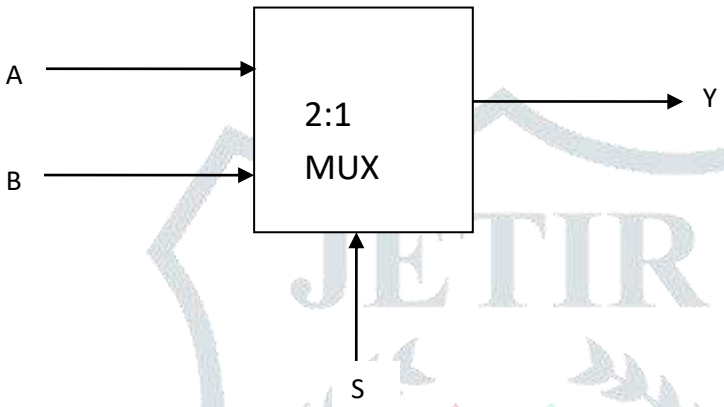

Fig 1. Symbol Diagram of 2:1 MUX

Table I. Truth Table of 2:1 MUX

Select Line	Input		Output
~s/s	A	B	Y
1/0	X	0	0
1/0	X	1	1
0/1	0	X	0
0/1	1	X	1

2. Gate Level Based 2:1 MUX

In electronics, a multiplexer is a device that chooses one of a few simple or digital input signals and advances the chose contribution to single line. Multiplexer of 2n inputs having n number of selected lines, those are required to pick which of the input line to deliver to yield. Multiplexers are principally used to expand the measure of information that can be sent over the system inside a specific measure of time and transfer speed. A Multiplexer is likewise called the information selector. They are utilized in CCTV, and relatively every business that has CCTV fitted, will claim one of these. An electronic multiplexer create it useful for a couple of signs to share one contraption or resource, for example one A/D converter or correspondence line, as opposed to having a device for every data flag. An electronic multiplexer could be well thought-out as a multi input, a yield switch. In broadcast communications and flag preparing, a simple time division multiplexer (TDM) may take a few examples of particular simple flag and join them into one pulse amplitude modulated (PAM) wide-band simple flag. Then again an advanced TDM multiplexer may consolidate a predetermined number of consistent bit rate digital information streams into one information stream of a higher data rate, by forming information outlines comprising one timeslot per channel.

In Digital circuit outline, the selector wire is of advanced esteem. If there should be an occurrence of 2-to-1 multiplexer a rationale estimation of 0 would associate with I0 to the yield while the rationale estimation of 1 would interface I1 to the yield.

A 2-to-1 multiplexer has a Boolean condition where An and B are two information sources Sel (S) is the selector information and Vout is the yield

$Vout = (A.S_0) + (B.S_1)$

A direct acknowledgment of 2-to-1 MUX would require 2 AND entryway, an OR gate and a NOT gate. Image Diagram of 2:1 MUX is appeared in Fig 1, Schematic of traditional 2:1 MUX is appeared in Fig 2 and the yield waveform of regular 2:1 MUX has appeared in Fig 3.

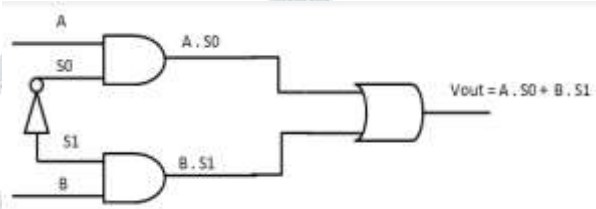

Fig 1. Gate level Diagram of 2:1 MUX.

3. Proposed 2:1 MUX

In this work, the 2:1 multiplexer has been designed using Static CMOS logic and Pseudo NMOS logic has been simulated shown in below figures. The transistor sizing for the 2:1 MUX designed and estimated results and comparison are shown is below Tables.

I. Static CMOS Logic

Working of Static CMOS Logic is with the help of Pull up network also known as (PUP) & (PDN) which is Pull down system. The limit of the PDN is to give a relationship between the yield and VDD when the yield of the method of reasoning entryway assembled is 1. So also, the PDN interfaces the yield to ground when the yield is required to be 0. The PUN and PDN systems are developed in a totally unrelated way with the end goal that either PDN or PUN is leading in relentless state. One of the major advantages of Static CMOS logic is that they have zero quiescent power dissipation, where for any applied input state either the PUN or the PDN remains off. The problem with this type of implementation is that more area is required in implementing logics.

Analysis and Simulated Results

Static CMOS logic is designed consists of select pins S, SBAR, two inputs A and B and output pin VOUT. The static CMOS based 2:1 MUX has been designed using a PUN consisting of 4 pMOS and a PDN consisting of 4 nMOS. The PUN is developed utilizing two parallel pMOS circuits associated in arrangement. The PDN is built utilizing two arrangement nMOS circuits associated in parallel. The output of the Static CMOS logic is connected to an inverter to obtain the correct output. Vdd is associated with the

draw up circuit to give control supply and the ground is associated with the draw down circuit. The input to the circuit is provided with the help of Vpulse which is set according the truth table of 2:1 MUX. The schematic of static CMOS logic is shown in Fig.3 and and its Transient Response is shown in Fig.4

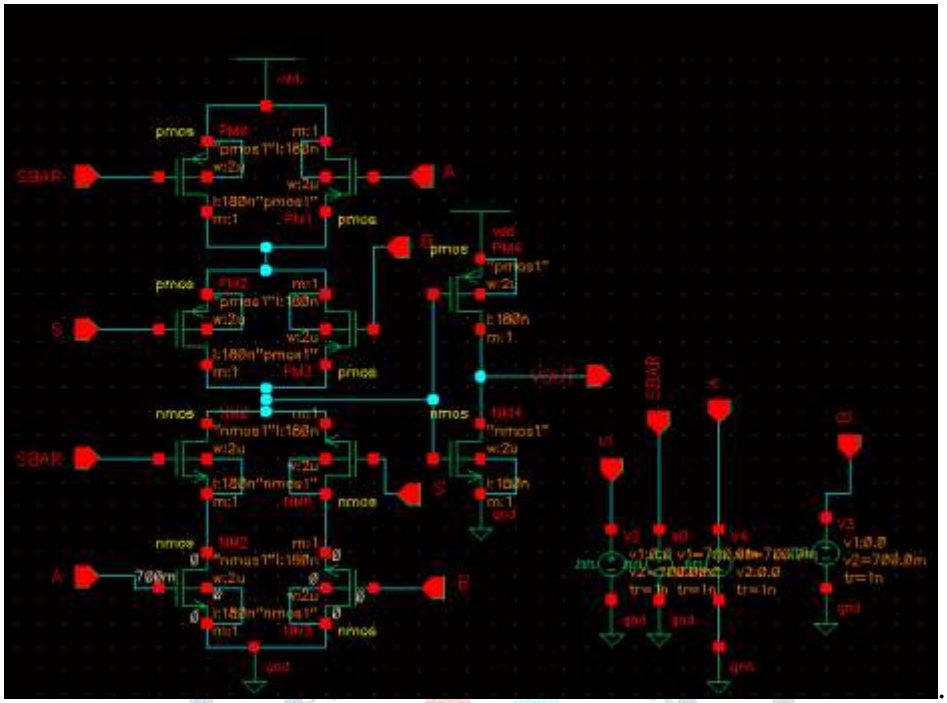

Figure3.Schmetic of Static CMOS logic

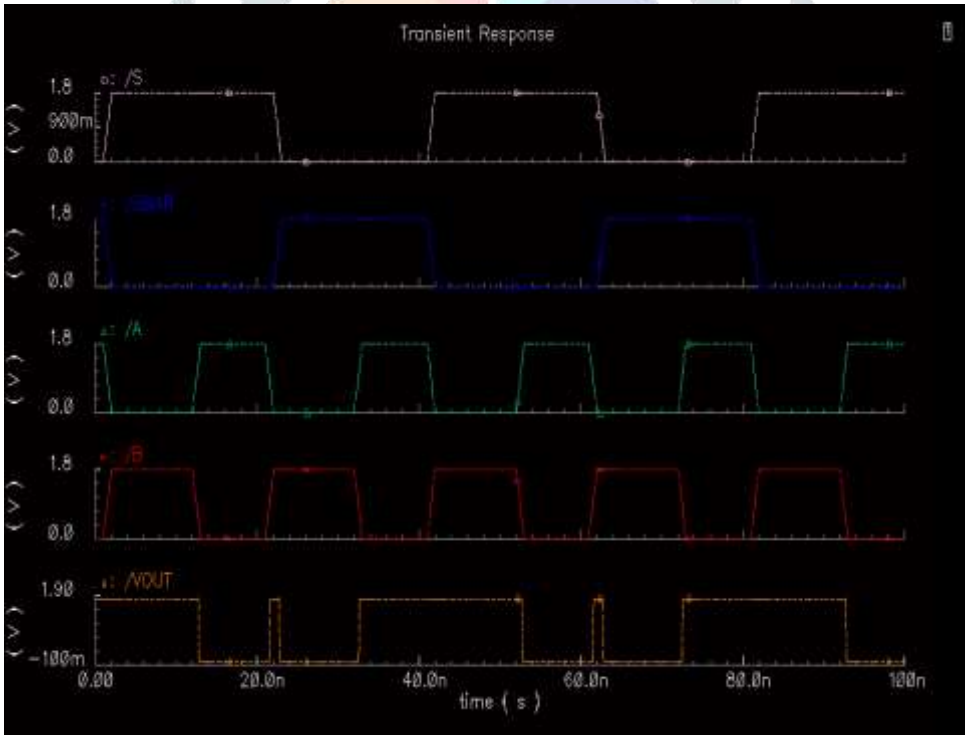

Figure 4.Transient Response of Static CMOS logic

Static CMOS logic is designed consists of select pins S, SBAR, two inputs A and B and output pin VOUT. The static CMOS based 2:1 MUX has been designed using a PUN consisting of 4 pMOS and a PDN consisting of 4 nMOS. The PUN is developed utilizing two parallel pMOS circuits associated in

arrangement. The PDN is built utilizing two arrangement nMOS circuits associated in parallel. The output of the Static CMOS logic is connected to an inverter to obtain the correct output. Vdd is associated with the draw up circuit to give control supply and the ground is associated with the draw down circuit. The input to the circuit is provided with the help of Vpulse which is set according the truth table of 2:1 MUX. The schematic of static CMOS logic is shown in Fig.5 and its Transient Response is shown in Fig.6. Simulated Result Summary is shown in Table1.

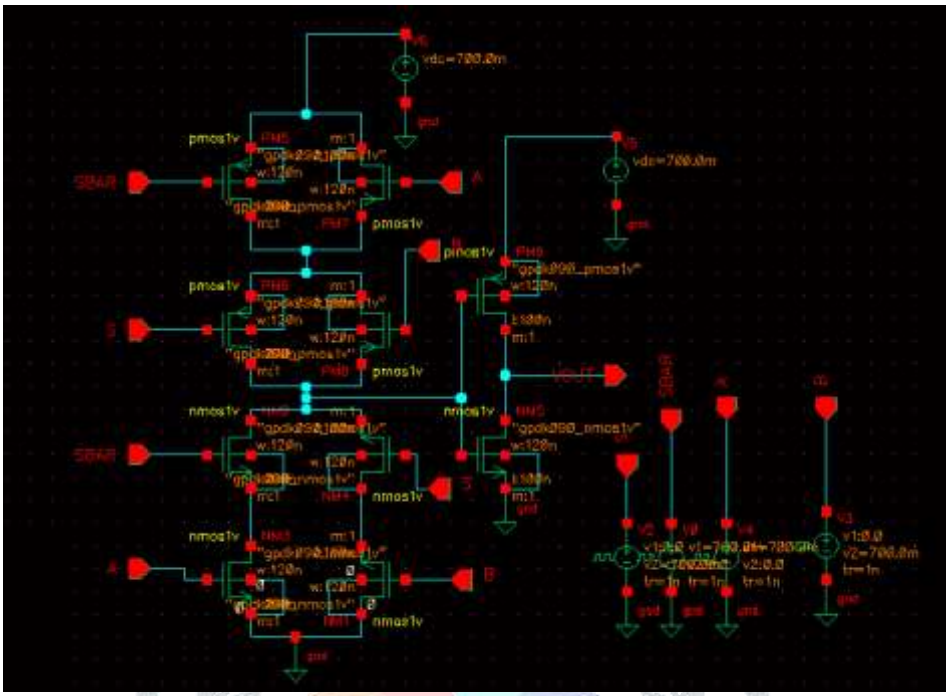

Figure5.Schmetic of Static CMOS logic

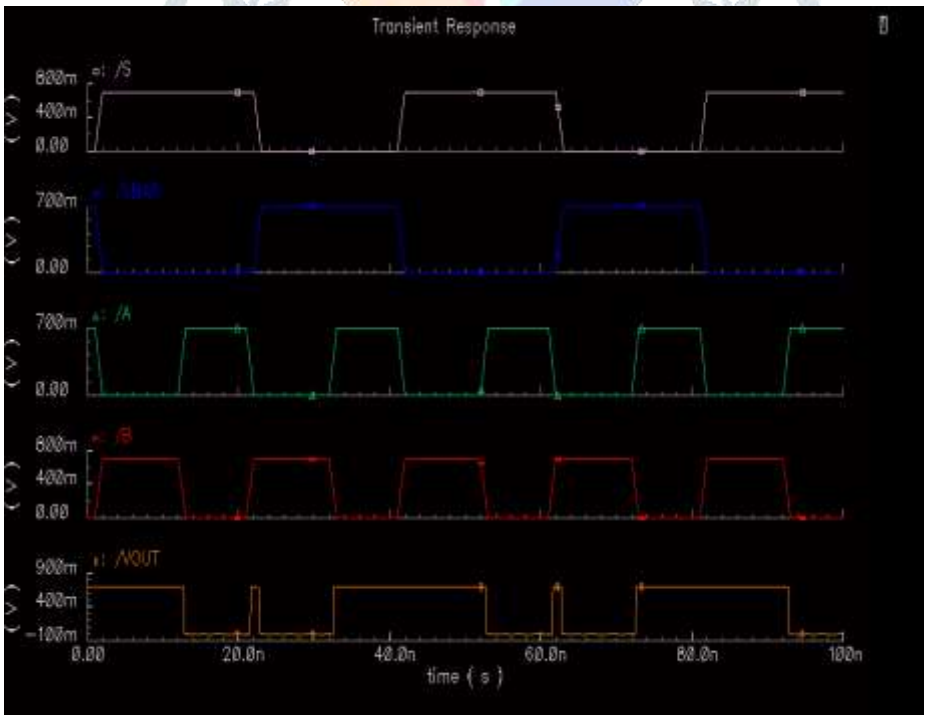

Figure 6.Transient Response of Static CMOS logic

TABLE 1. Simulated Result Summary

Performance parameter	Static CMOS Logic at 180nm Technology	Static CMOS Logic at 90nm Technology	Static CMOS Logic at 45nm Technology
Transistor Sizes	W= 200nM and L=180nM	W=120nM and L=100nM	W=120nM and L=100nM
Temperature	27ºC	27ºC	27ºC
Supply Voltage	1.8 V	0.7 V	0.7 V
Rise time	1ns	1ns	1ns
Fall time	1ns	1ns	1ns
Leakage Power	2.30nW	9.33pW	4.23pW
Leakage Current	7.45nA	8.85pA	3.42pA

II. Pseudo NMOS Logic

In **Pseudo NMOS Logic** the PDN resembles that of a normal static gate; however the PUN has been supplanted with a solitary pMOS transistor that is grounded so it is dependably ON. The pMOS transistor widths are chosen to be around 1/4 the quality of the nMOS PDN as a tradeoff between clamor edge and speed; this best size is process-subordinate [9]. In this way the area required to implement logics have been reduced which in turn increases the speed.

Analysis and Simulated Results

Pseudo NMOS logic is designed consists of select pins S, SBAR, two inputs A and B and output pin VOUT. The design of 2:1 MUX using Pseudo NMOS logic is similar to Static CMOS logic except that the entire PUN is replaced by a single pMOS transistor and grounded permanently to decrease the transistor calculate. The output of the Pseudo NMOS is connected to an inverter to obtain the correct output the schematic of Pseudo NMOS Logic is shown in Fig 7and and its Transient reply is given away in Fig.8. The power supply is presented by Vdc at 1.8V connected to the pullup circuit and the circuit inputs are given with the help of Vpulse as per the truth table of 2:1 MUX.

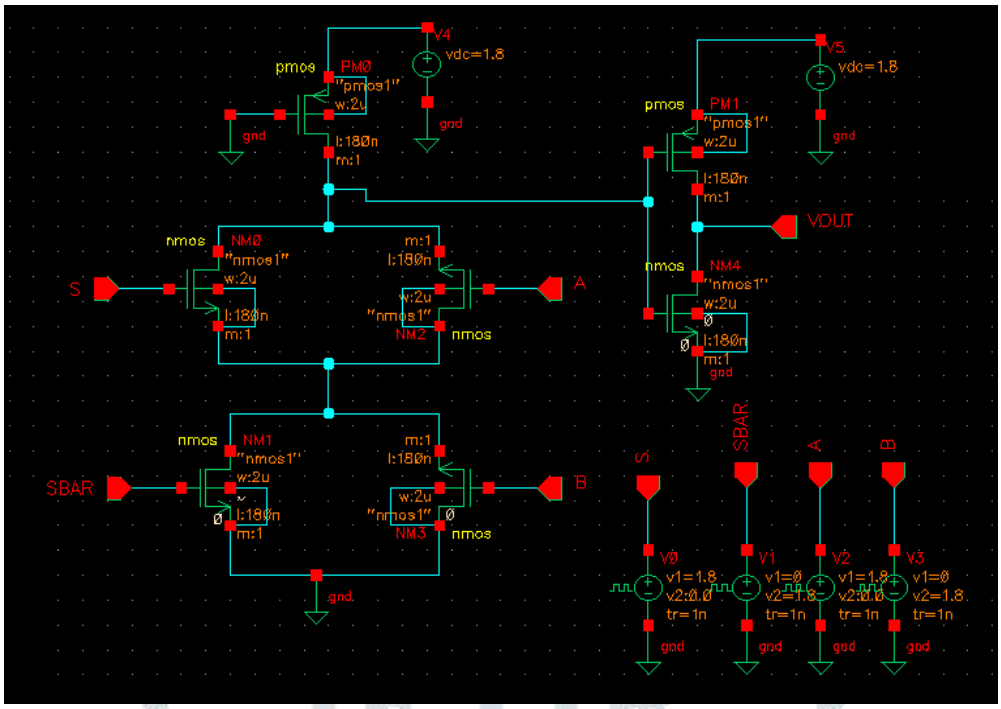

Figure7.Schmetic of Pseudo NMOS Logic

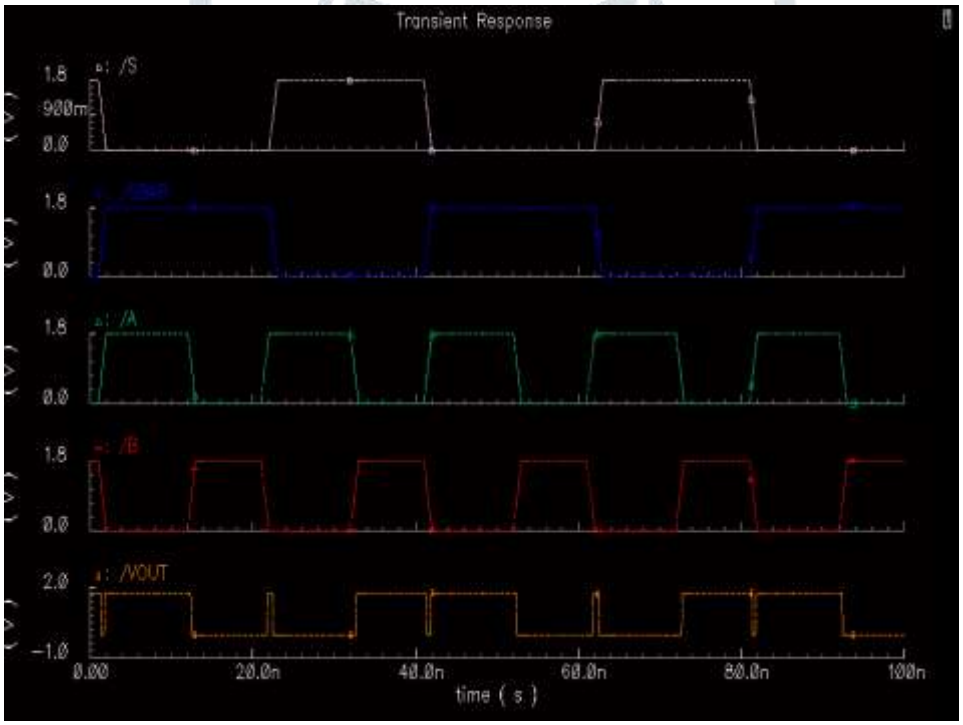

Figure 8.Transient Response of Pseudo NMOS Logic

Pseudo NMOS logic is planned consists of select pins S, SBAR, 2 inputs A and B and output pin VOUT. The design of 2:1 MUX using Pseudo NMOS logic is similar to Static CMOS logic except that the entire PUN is replaced by a single pMOS transistor and grounded permanently to decrease the transistor calculate. The output of the Pseudo NMOS is connected to an inverter to obtain the correct output the schematic of Pseudo NMOS Logic is shown in Fig 9and and its Transient reply is display in Fig.10. The power supply is given by Vdc at 0.7V connected to the pullup circuit and the circuit inputs are given with the help of Vpulse as per the truth table of 2:1 MUX. Simulated Result Summary is shown in Table2.

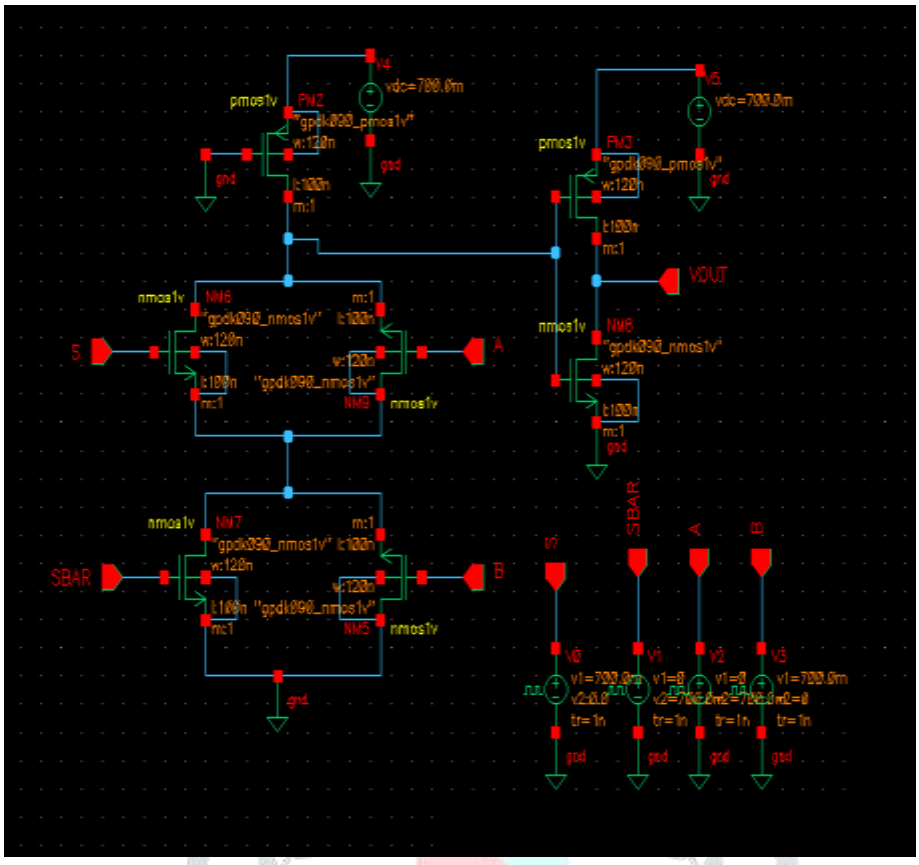

Figure9.Schmetic of Pseudo NMOS Logic

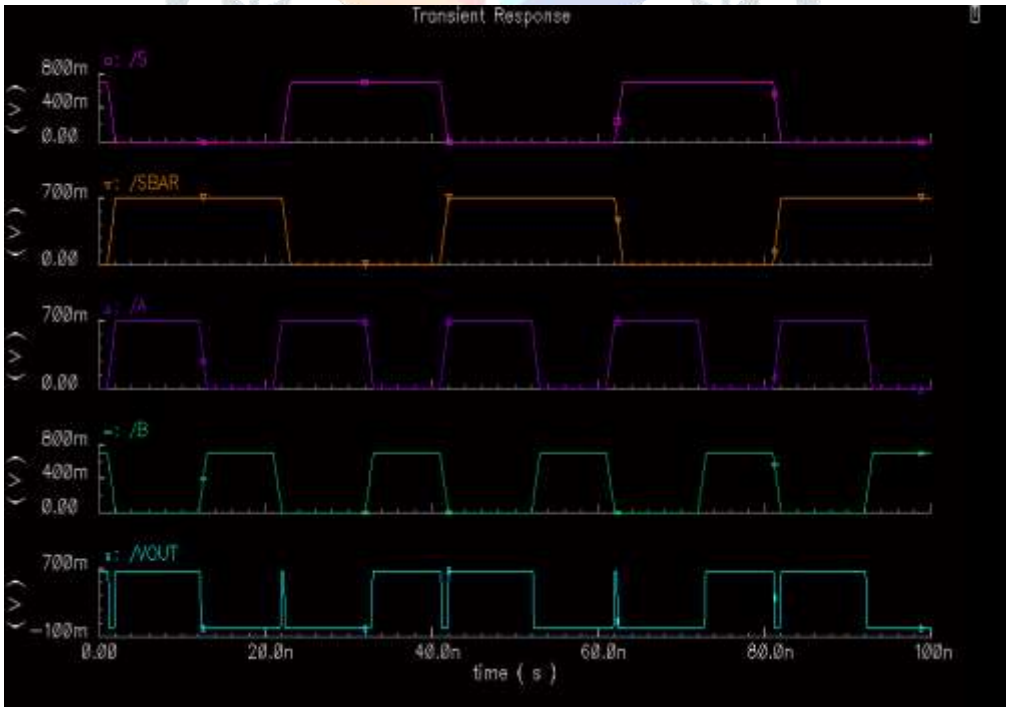

Figure 10.Transient Response of Pseudo NMOS Logic

TABLE 2. Simulated Result Summary

Performance parameter	Pseudo NMOS Logic at 180nm Technology	Pseudo NMOS Logic at 90nm Technology	Pseudo NMOS Logic at 45nm Technology
Transistor	W= 200nM and	W=120nM and L=100nM	W=120nM and

Sizes	L=180nM		L=100nM
Temperature	27ºC	27ºC	27ºC
Supply Voltage	1.8 V	0.7 V	0.7 V
Rise time	1ns	1ns	1ns
Fall time	1ns	1ns	1ns
Leakage Power	1.33nW	8.29pW	1.24pW
Leakage Current	1.27nA	7.33pA	1.42pA

Comparison among Static CMOS logic & static Pseudo NMOS logic on basis of diverse approaches is given below in table 3.

Table 3 Comparison Result Summary

Performance Parameter	**Static CMOS Logic**	**Pseudo NMOS Logic**	**Static CMOS Logic**	**Pseudo NMOS Logic**	**Static CMOS Logic**	**Pseudo NMOS Logic**
Technology used	**180nm**		**90nm**		**45nm**	
Transistor Sizes	**W(Width)=200nm, L(Length)=180nm**		**W(Width)=120nm, L(Length)=100nm**		**W(Width)=120nm, L(Length)=100nm**	
Leakage Power	**2.30nW**	**1.33nW**	**9.33pW**	**8.29pW**	**4.23pW**	**1.24pW**
Leakage Current	**7.45nA**	**1.27nA**	**8.85pA**	**7.33pA**	**3.42pA**	**1.42pA**

Conclusion

In this paper a 2:1 MUX using Static CMOS logic and Pseudo NMOS logic was fabricated and measured result in 180nm, 90 nm and 45nm CMOS technology. The simulation proves that it operates well at 1.8V, 0.7V and 0.7V supply voltage and under 27ºC temperatures with low power consumption. In this paper, a 2:1 MUX is executed utilizing different Static CMOS rationale and Pseudo NMOS and it's implemented metrics are analyzed. It is clearly inferred that, 2:1 MUX designed using Pseudo NMOS is the most efficient design because the reduction in average power consumption and leakage current estimated to Static CMOS and the transistor count up is also decrease. The significance of a Multiplexer is that it can be used in Parallel to Serial convertor (which a major application of MUX) to reduce wide parallel busses to serial signals in the field of Telecommunication, Data communication, Satellite and Military applications. Therefore, based on all the performance analysis made in this work it is proved that MUX designed using Pseudo NMOS logic can be used in various applications to obtain better performance.

References

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