Design and Performance Comparisons of CMOS based and Pass Transistor based 1:2 DEMUX at 90nm and 45nm Technology

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Abstract

This research paper analyzes the performance of De-Multiplexer (DEMUX) using CMOS based DEMUX, Pass Transistor based DEMUX. Moreover, an evaluation among the exhibitions of both the setups as far as power dissemination, chip region, power supply and leakage current are evaluated. In order to restrain the deprivation of signals and to increase the operation speed, we designed interconnection for the circuit; the implementation is done in VLSI technology as it has features like small area, low cost, reduction in leakage current and low power. The circuit shows rise and fall times of about 1ns and consumes low power according to the design and number of transistor used in the circuits. The composed circuit is acknowledged in a standard 90nm and 45nm process technology and utilizations 0.7V supply voltage. Our optimization circuitry using the proposed method reduces power consumption and leakage current by significant amount of DEMUX circuit.

Key Words: DEMUX, CMOS Based DEMUX, Pass Transistor Based DEMUX Low Power, Leakage Current, Cadence.

1. Introduction

Multiplexers and de-multiplexers are regular building blocks of information ways and are utilized broadly in various applications including processor transports, organize switches and computerized flag handling stages fusing asset sharing. The decrease of the power utilization by any VLSI circuit essentially relies upon the a few parameters viz. reducing the number of transistor, reducing the size of the transistor, input re-ordering, reducing the capacitance etc. It is for the most part trusted that low power plants need least transistor estimate. Most of the low-power design techniques are effective only for specific types of circuits and applications. Delay and power dissemination of a circuit have additionally developed as real worries of architects and rely upon the quantity of transistors utilized in the circuit. At the point when the quantity of transistors is increasingly the capacitance is more because of which the postponement is more [1-2] so here our point is to decrease the deferral and power dispersal. Symbol diagram of 1:2 DEMUX is shown in Fig1.
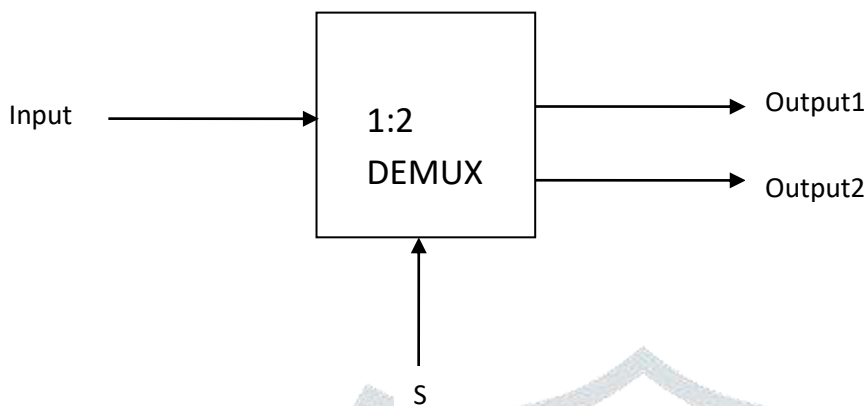
Fig 1. Symbol Diagram of 1:2 MUX

Digital computers process and move enormous measure of digital signal. It is restrictive to make isolate straight wire associations for the exchange of this information inside the PC with the strategy of multiplexing; a solitary wire is utilized to exchange information from different sources from the sending end. Presently at the less than desirable end this information from different sources should be isolated for conveyance to expected beneficiaries. The gadget cooking this need is a de-multiplexer. [3-4]. A de-multiplexer (DEMUX) is a combinational digital circuit that has one info and in excess of one yield. It is utilized when a circuit wishes to send a flag to one of numerous gadgets [5]. In this paper, the impact of progress in design of 1:2 DEMUX as far as power scattering, chip region, supply voltage and yield current is broke down. The schematic chart and trademark table for 1:2 DEMUX is appeared in Table I and door level outline is appeared in Fig. 2. It is seen from the graph that 1:2 de-multiplexer has one information line IN and one select line S, though, OUT1 and OUT2 are the two yields. At the point when S is in rationale state 1 (high) yield line OUT2 is chosen and reflects contribution at terminal A. So also, when S is rationale 0 (low) yield line OUT1 is chosen and contribution at IN achieves yield line OUT1. The 1:2 de-multiplexer rationale is actualized utilizing entryway level setup that incorporates two-rationale door and one inverter circuit [5]. The watched result shows that the power scattering, chip zone, yield current level and different parameters shift with change in transistor innovation hub or architecture.

Table I. Truth Table of 1:2 DEMUX

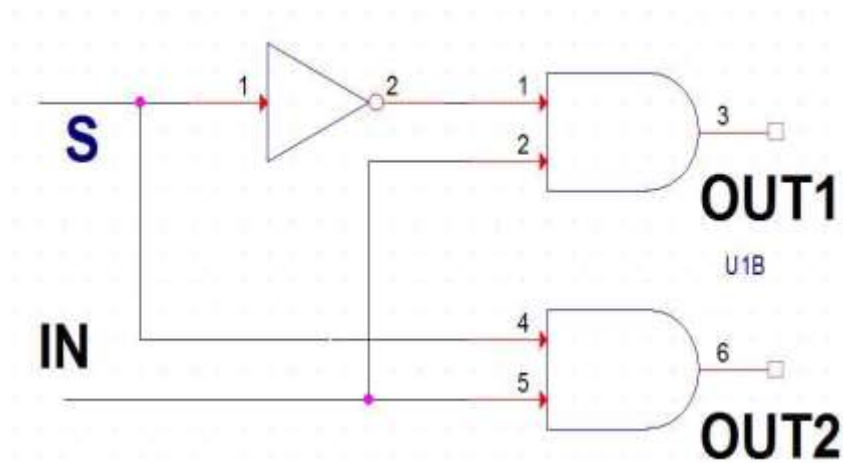| Select Line S	Input	Outputs	
		Output1	Output2
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1

Fig2. Gate Level Diagram of 1:2 DEMUX

2. Proposed 1:2 DEMUX

In this work, the 1:2 De-multiplexer has been designed using CMOS based DEMUX and Pass Transistor based DEMUX has been simulated at 90nm technology shown in below figures. The transistor sizing for the 1:2 DEMUX designed and estimated results and comparison are shown is below Tables.

I.   Implementation of CMOS Based DEMUX

CMOS logic architecture is a standout amongst the most usually utilized rationale arrangement utilized in digital circuit outlining yet it has its own merits and demerits. Maybe a couple is portrayed here, for example, vast quantities of transistors are required even to actualize straightforward circuits like essential rationale doors and inverter circuit. Fig.3 delineates CMOS design of 1:2 de-multiplexers [6] and its transient reaction is appeared in Fig.4. It is obvious from the chart that 14 transistors are required to execute this gadget. Six transistors for each AND gate and two for NOT gate, where S is selection line. The INPUT is input that is applied to both the AND gates. VOUT1 and VOUT2 represent output lines. The selection of these lines is dependent on terminal S.DC Response of 1:2 DEMUX using CMOS based is shown in Fig.5.Static noise margin improves the performance of the system and leakage current waveform is shown in Fig.6. It can likewise be comprehended from the assume that huge number of interconnects are utilized in this way to deal with interface various transistors. Along these lines, CMOS rationale is anything but difficult to plan yet extremely asset expending [7].

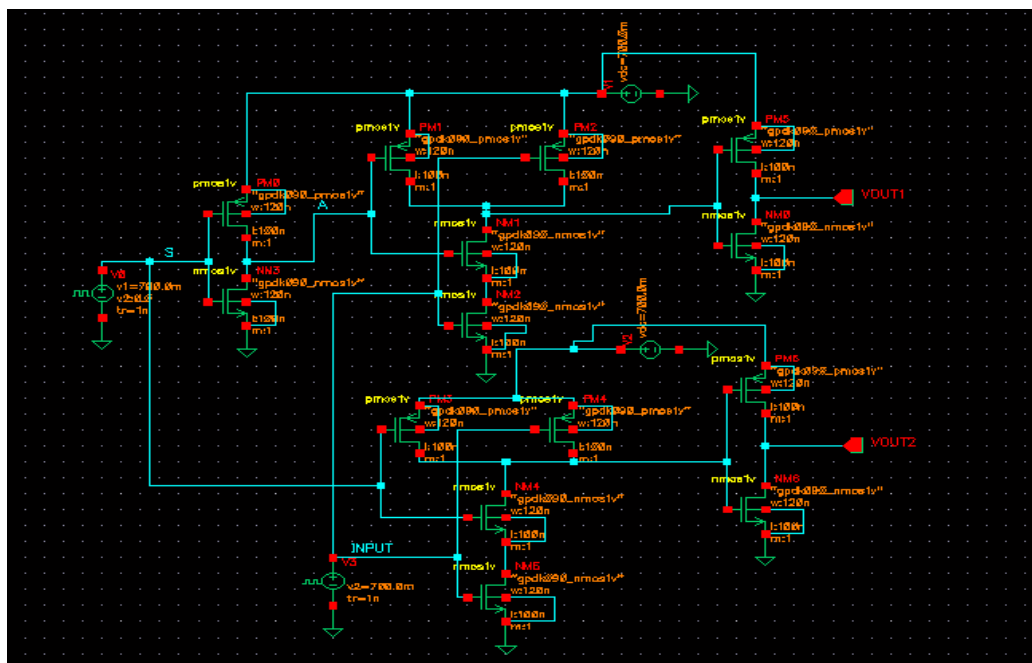**Analysis and Simulated Results**
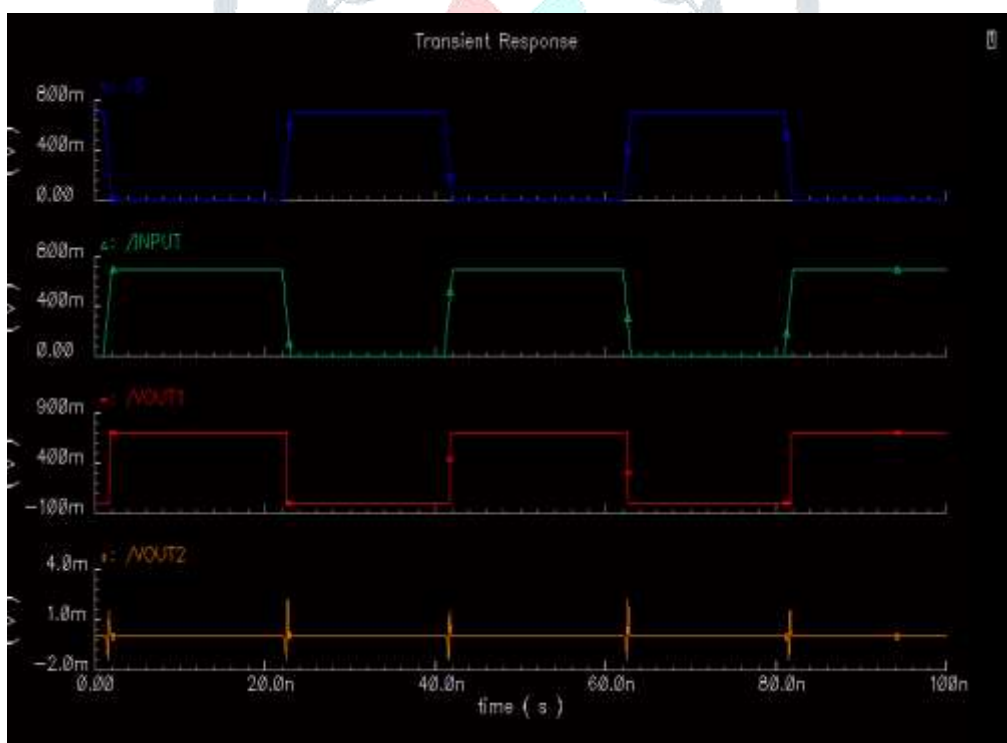

Fig.3 Schematic of CMOS based DEMUX

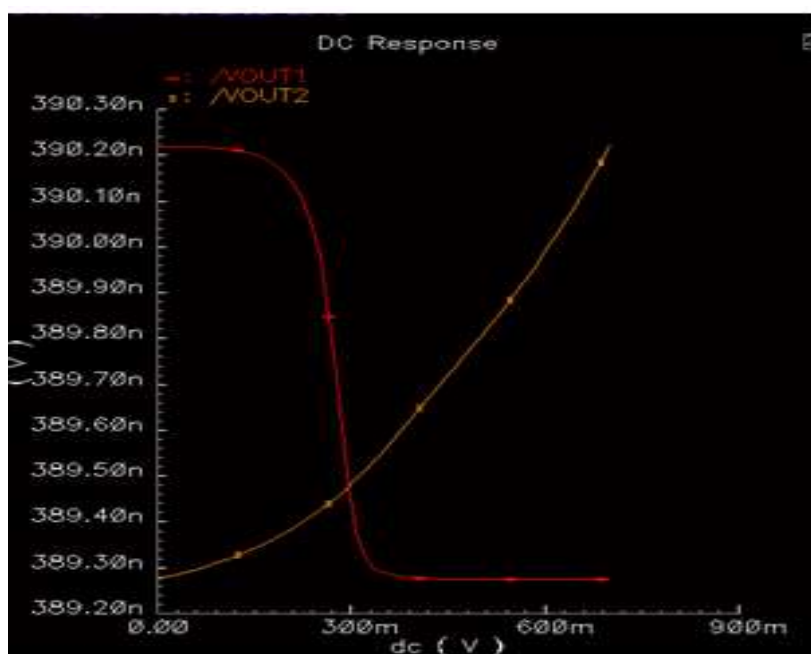Fig.4 Transient Response of CMOS based DEMUX
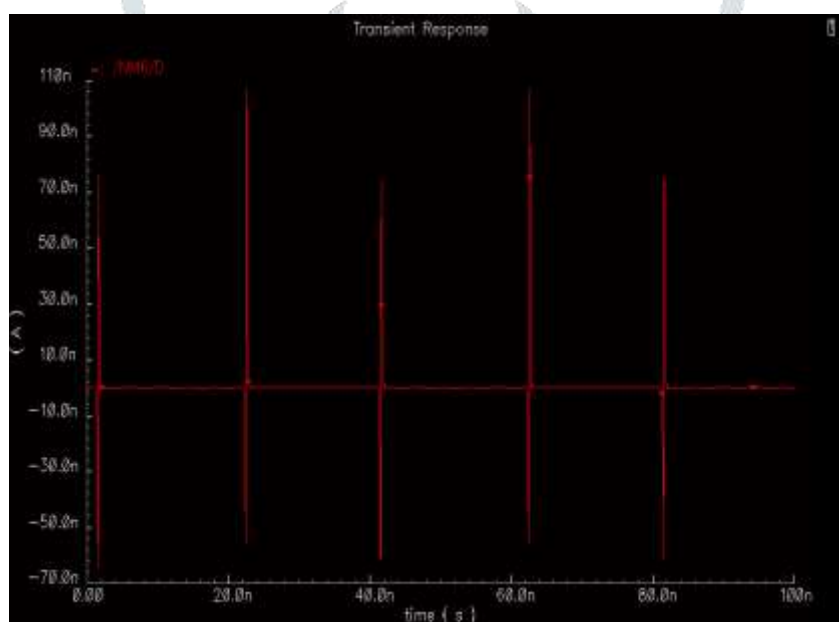
Fig.5. DC Response of CMOS based DEMUX

Fig.6 Leakage Current Waveform of CMOS based DEMUX

II.   Implementation of Pass Transistor Based DEMUX

The usage of 1:2 DEMUX utilizing pass transistor depend designs is required just six transistors to execute the complete logic architecture. This means that number of transistors used in pass transistor depend DEMUX architecture is less than 50% (Half) of the transistors utilized in CMOS depend DEMUX architecture. Therefore, it is evident from the facts stated. Fig.7 and Transient response is shown in Fig.8. It demonstrates that the aria utilization is half less utilizing pass transistor founded DEMUX design. In addition, lesser interconnect lengths and less transistors permits a decrement in manufacture cost as well. Additionally, the manufacture steps and assets are likewise diminished/devoured less in pass transistor based DEMUX usage. Along these lines, results saw in both the engineering

are certified that pass transistor based DEMUX design is more region effective than customary CMOS based DEMUX architecture [2-8].

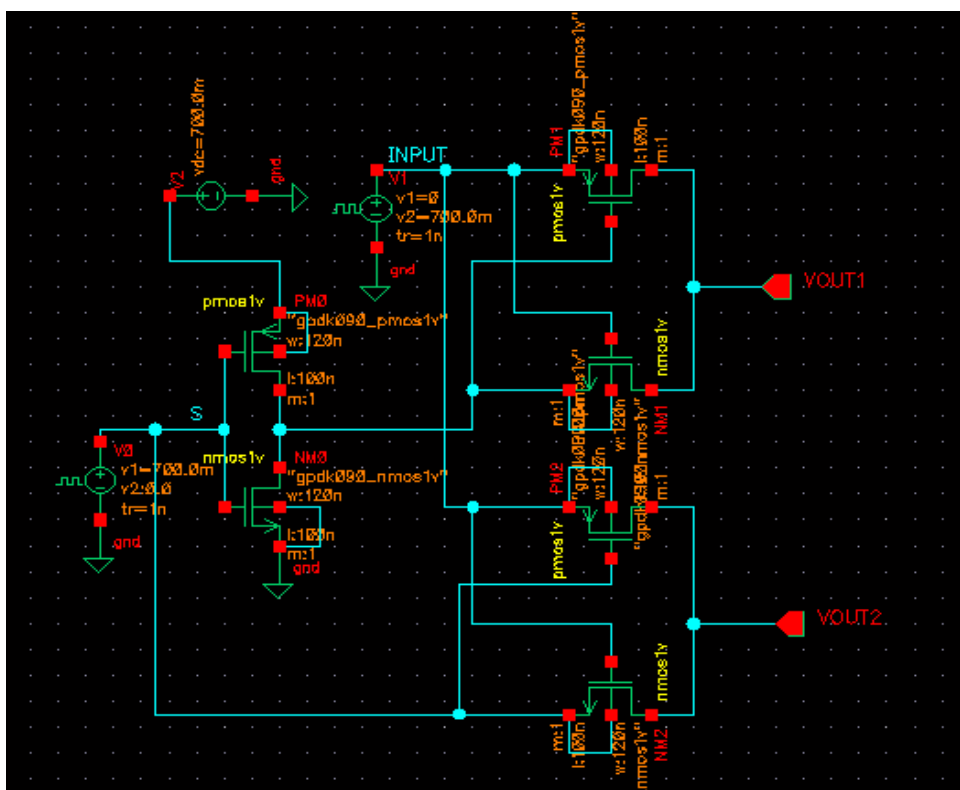**Analysis and Simulated Results**

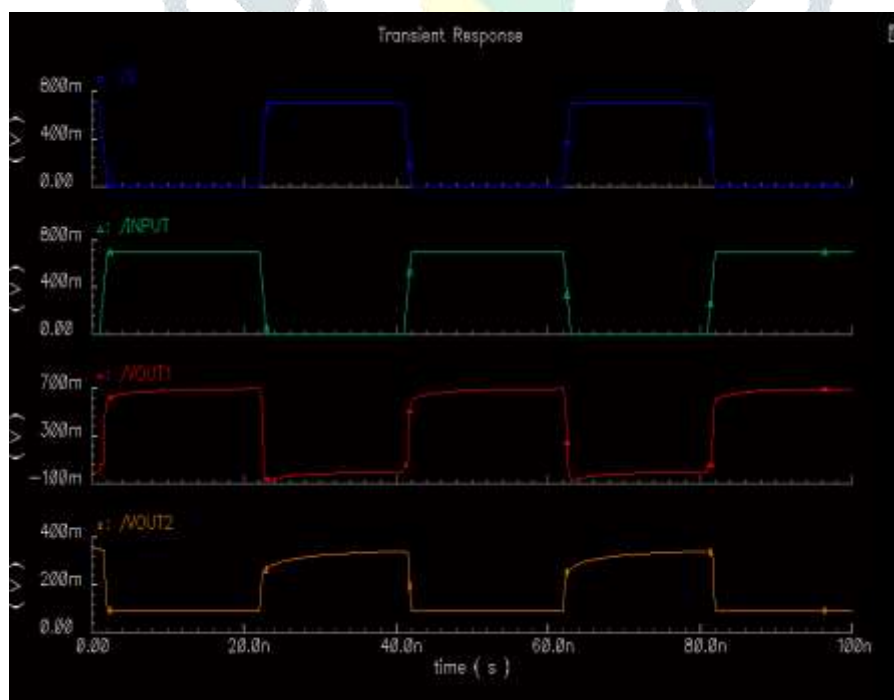Fig.7 Schematic of Pass Transistor based DEMUX

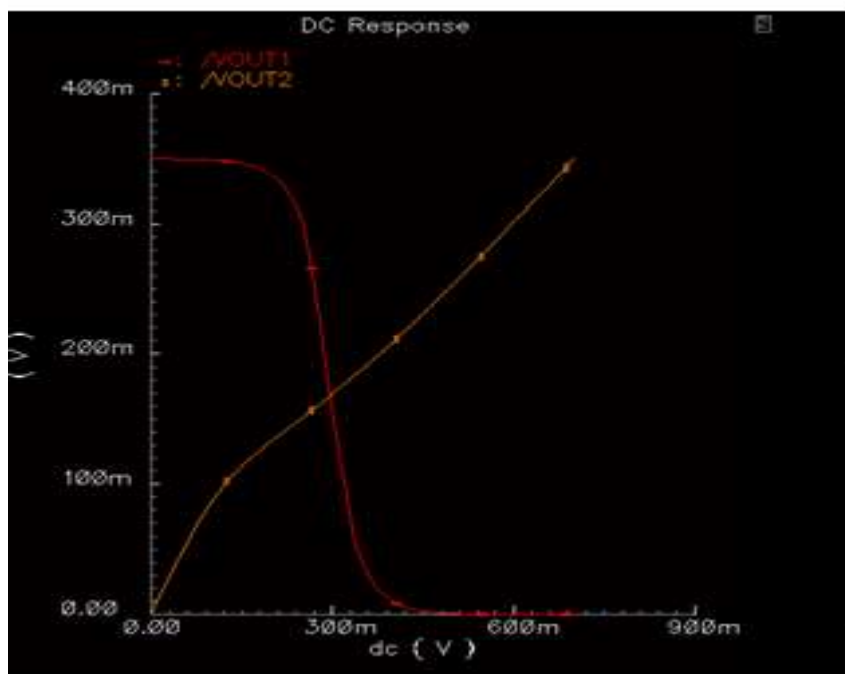Fig.8 Transient Response of Pass Transistor based DEMUX
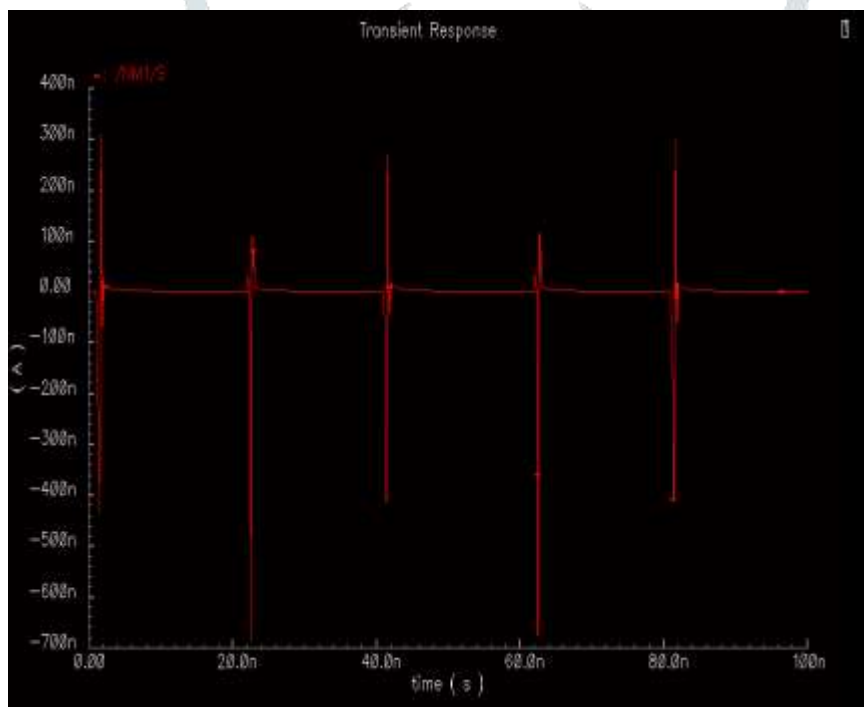
Fig.9. DC Response of Pass Transistor based DEMUX

Fig.10 Leakage Current Waveform of Pass Transistor based DEMUX

Table 3 Comparison Result Summary

Performance Parameter	CMOS based 1:2 DEMUX	Pass Transistor based 1:2 DEMUX	CMOS based 1:2 DEMUX	Pass Transistor based 1:2 DEMUX
Technology Used	90nm	90nm	45nm	45nm
Supply Voltage	0.7V	0.7V	0.7V	0.7V
Power	9.69.nW	5.8nW	6.86.pW	4.43pW

Dissipation				
Leakage Current	7.57nA	3.35nA	6.76pA	4.56pA
Transistor Count	14	6	14	6
Chip Area	large	less	large	Less

Conclusion

Analysis the performance of De-Multiplexer (DEMUX) using CMOS based DEMUX, Pass Transistor based DEMUX. Besides, a correlation between the exhibitions of both the setups as far as power dissemination, chip zone, control supply and spillage current are evaluated. The outcomes saw that roughly half of chip territory is spared by utilizing the Pass Transistor based DEMUX as just six transistors (6-T) are utilized to execute the 1:2 de-multiplexer while fourteen transistors (14-T) are make use of in CMOS founded DEMUX plan. The composed circuit is acknowledged in a standard 90nm and 45nm process innovation and utilizations 0.7V supply voltage. Our optimization circuitry using the proposed method reduces power consumption and leakage current by major amount of DEMUX circuit. This paper analyzed the performance parameter of 45nm process technology is more efficient than 90nm process technology 1:2 DEMUX using CMOS depend DEMUX, Pass Transistor based DEMUX. The power supply is decreased by seen because of procedures with pass transistor rationale. In addition, decrease in power dissemination is broke down with pass transistor. Along these lines, it very well may be presumed that the Pass Transistor based DEMUX execution of 1:2 DEMUX gives better execution and devours less chip zone in correlation to CMOS based DEMUX architecture.

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