Design and Analysis of 4 bit Barrel Shifter using nano-scale CMOS Technology

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Abstract

This paper Proposes 4 bit Barrel Shifter (BS) acting an important role in the data shifting (DS)and data rotation. It is having application in many areas. The BS is mostlyutilized for generalization of DS. The Arithmetic & Logical Shifters can also be exchange by BS cause by rotation of data it also gives application data right, left shifting either arithmetically or logically. The principle of this paper is to propose4 bit BSutilizing universal gates with assist of CMOS logic. The additionalsuperioredition of BS is 4 bit DS that is also projected here. The paper analyzes, optimizes and compares delay andpower of the 4 bit Barrel Shifter using 90 nm and 45nm technologies. Bit-wise function is pivotal whenprogramming hardware registers in embedded method.There are many instances where we need to change only onebit of a complete register, in this case, changing the wholeregister value can be time consuming and undesirable. Bitshifting is one of the many useful bit operations one canperform. In paper it have presents 4 BS which is used in right-shift, left-shift, depending on what user approach&considered its distinctiveness. The simulationresults are carried out using Cadence.

Key Words:CMOS, Low Power, Delay,Barrel Shifter, PMOS, NMOS, Cadence.

1. Introduction

DS is one of significantneed ofseveral key computer functions, from address creationto arithmetic operations. Shifting of individual data bit onefield at time can be slow produce. This iswhere BSarrives in. BS is combinational circuit with n data inputs & n dataoutputs with control inputs that identify shifting ofinput data as output & bit BSneedn, n bit multiplexers. But n-bit BS need namount of n-bit multiplexers. If n is raised circuitcomplexity also rises i.e., circuit over head, it leadsto occupy more area and high power consumption andalso shows the effect on speed of the operation [1]. Thecurrent technology utilized for building integratedcircuits is Complementary metal oxide semiconductor(CMOS). The technology is being utilizedin many digital& analog logic circuits like highly integratedtransceivers, data Converters &image sensors (CMOS sensor)for various kinds of applications [2]. BS is furtherutilized for shifting operation such asshift left arithmetic, right rotate, shift rightlogical, left rotateand shift rightarithmetic &shift left logical. The design ofBS can be madeviautilizing multiplexers. Soto plan shifter, we need to plan multiplexer 1st.Normally 2:1, 4:1, 8:1 mux trees are utilized for designingof shifter. In presented paper itintendedBS utilized universal gates & 90 nm technology. Theconsequencesinvolveevaluationamongvariousmethodologies to diminish Power consumption in ALUplan [3].A Shifter is mainlyvaluable for arithmeticfunctionas shifting is comparable to multiplicationby powers of 2. Floating point arithmetic is example of shifter. Currently there are huge amountof shifters are

in use. The easiest shifter is shiftregister that shift by one location per clock cyclebut normally there is requirement to shift numerous bits in 1cycle & to differ length of shifts. The Shifterscan be classifying as Level Shifter (LES), Arithmetic Shifter (AS),BS,Funnel Shifter(FS)&Logical Shifter (LS). LS can shift data to left or right. Data is shiftedin direction of left & right viacertain logic &vacantposition are full by 0's. AS is similar as LS in case of left shifting. But in case of rightshifting vacantposition or mainimportant bits willbe as similar sign bit. BS can present nbit shifts in individual combinational operation or in individual clock cycle &haveproficient layout. BS isalso called as Rotator because it rotates data in cycle likevacant spots are filled by bitsshifted off another side. A FS can do overall 6kind of shifts that are presentedviaearlierdeclared shifters. LES are utilized to changelogical signal from 1 voltage to other voltage. Separatelyfrom this LES are utilized at pad ring & coreof chip interface where low voltage signal via chipcore are shifted to high voltage [4].A BS is combinational rationale hinder that will shift substance of transport determined quantity of location left or large via control word. This is crucial capacity in PCs &various sign organize ICs. Frequently, whileshifting to 1part, locationvacant will be loaded with character from left, or if no character isavailable, then loaded with zeros also while no character are available, vacant location may be filled evaluation of most critical piece (MSB) [5]. A little shifters actuallyrevolve substance of transport filling slightest critical bits (LSBs) with previous substance of MSBs for shift left &anotherdirection around for shift right.

Researchers are exploring low power and high speedareas including subthreshold regions [6]. A barrel sifter is a circuit, digital by nature. It may shift data word having or preciseamount of bits in individual cycle. This is executed as series of multiplexer (Mux). In thisimplementation, the input of next multiplexer is connected tooutput of one multiplexor. All this connected in such way thatis dependent on shift distance.It has n data inputs, and n data output. Also it has set of inputs which are control input that tells how to shift the data ininput and output. If a barrel sifter is a part of a microprocessorCPU, it can tell the direction of a shift (left or right), the typeof shift weather logical, arithmetic or circular. Also it can tell,the amount of shift, be it 0 to n -1 bits or 0 to n bits [7]. Barrel shifter is required in many applications e.g. bit indexing, floating point adder & variable length coding. BSisgenerally in both digital signal processor & general purpose processor. Mux tree is designed with the helpof 2:1 mux as a basic building block. Shifter is an importantmodule in DSP and graphics [8].New approach has been presented for synthesis of a fast barrel shifter, which is usefulwith reduced delay but not much increased area [9].

2. BSArchitecture

There are 4 kinds of shifters:
a. Logical Shifter (Shift Right / Shift Left)
b. Arithmetic Shifter
c. Barrel Shifter
d. Funnel Shifter (Combination of above threeShifters)

a) Logical Shifter: Left Shift (LS)& Right Shift (RS)Operation)

As it is visible in Fig.1, LShave shifting input bits to left & 0 is appended at Least Significant Bit(LSB).The Most Significant Bit(MSB) of input is discarded or it can be saved for auxiliary use. By, shifting input 1 time to left it normally multiplying input by 2.

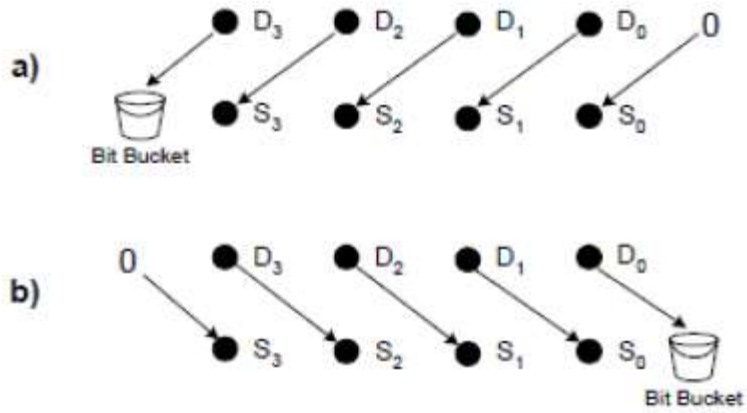

Fig.1 Logical Shifter

a. Left Shift (LS) Operation
b. Right Shift (RS)Operation (RSO)
In RSO, input bits are SR & 0 is appended at MSB.The LSB of input is discarded or saved for differentauxiliaryfunctions. By, shifting the input right one timewe are actually dividing the input by 2.

b) Arithmetic Shifter

So far awayithas no path to agreement with sign bit whilepresentingRS on signed data. In another words, we cannot do an arithmetic RS. For logical RS, zero is complete at left. Every of circuits beneathdo this. For an AS, leftmost bit of input is taken as sign bit. It may move to right &also copied to leftmost bit of output. The plan for such shifter is presentsbeneath Fig.2. A fourth control line is additional for arithmetic RS. An OR gate drives the RIGHTcontrol line when either an arithmetic or a logical right shiftis commanded. A second OR gate drives the copy functionfor the leftmost bit when an arithmetic right shift iscommanded.

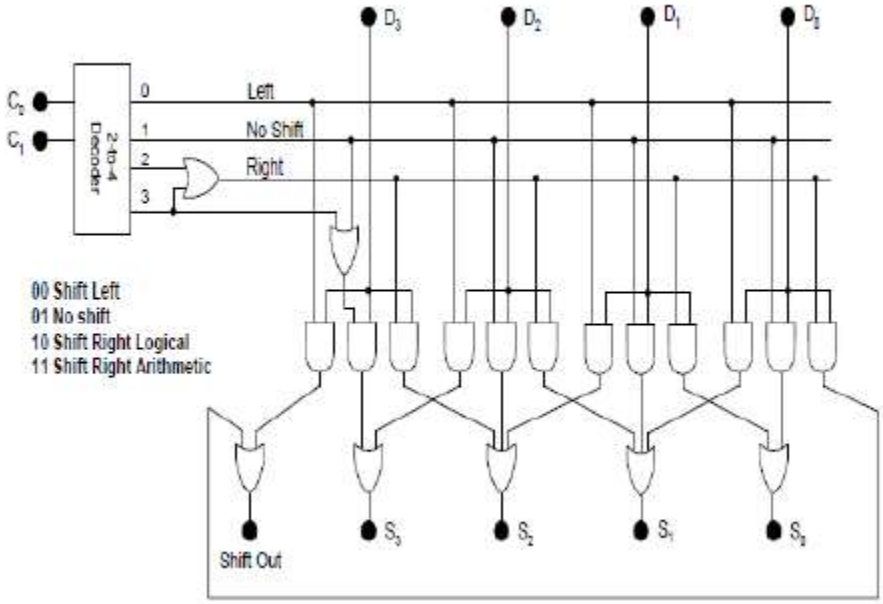

Fig.2 Arithmetic Shifter

A decoder is utilized to create control lines (CL). This means that control unit has to create only 2 bits to identify shifting &ensure that 1& only 1 set of CL within shifter is dynamic at any time. The codes utilized for 4 kinds of shifts are arbitrary.

c) Barrel Shifter

A BS is section of microprocessor CPU thatclassicallyidentifypath of SL or SR, kind of shift circular, arithmetic, or logical & quantity of shift (normally 1 to n-1 bits, but sometimes 1 to n bits). BSiscommonlyutilized for digital signal processors & general purpose processors to operate data. A BS is digital circuit that can move data word by particularamount of bits in 1 clock cycle. It mayexecute as seriesof multiplexers (mux) &in such an execution output of 1 mux is linked to input of further mux in way that depends on shift distance. BSadmits 2n data inputs & n control signals, producing n data outputs. [10]

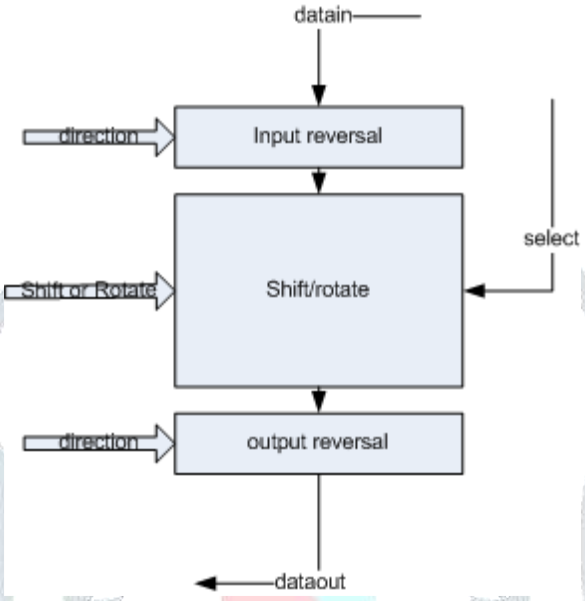

Fig.3 Block diagram of Barrel Shifter

It is mostsignificantsection of combinational Logic Block. It has capability to shift data work in individual functionbeneath standard SL or SR registers that use more than 1 clock cycle. It revolves numbers in cycle like that vacant spots are filled with bits shifted of another end.
Example: Barrel SR– 1100 subsequent to shift function will become 0110
Barrel SL – 1010 subsequent shift function will become 0101

As it is visible in diagram below, both Left Shift and the Right Shift is being done in the same circuit depending on one of two control lines. Inspect AND gates at extreme left & at extreme right, If LEFT control line is active, leftmost AND gate send its output to “bit bucket.” If RIGHT CL is active, another AND gate of pair sends signal D3 to output S2 via OR gate. Every left pairs of AND gates can send their outputs either left or right, depending on thatCL is active. Also it is worth noting that we are not storing LSB, MSB of input bits for Left, RS functioncorrespondingly.

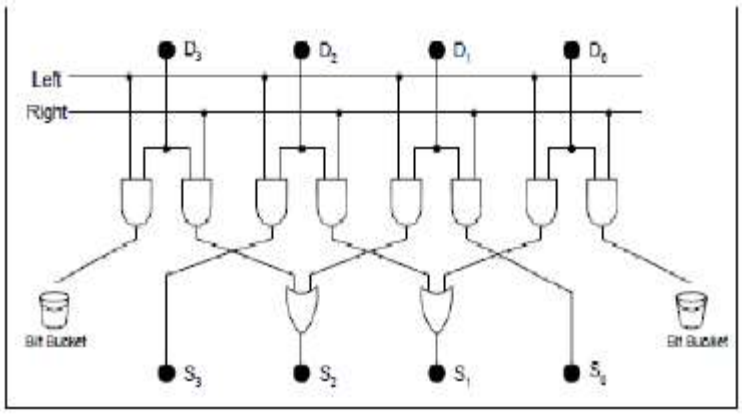

Fig.4 General Structure of 4-bit Barrel Shifter

3. Proposed 4-bit Barrel Shifter

A main issue in beneathnormalorganization was that bit that was moved out was not saved. As, bit shifted (BtS) out is of significance. In RS, it is remainssubsequent to division by 2. In SL, it can be examined for importance so that output of LS may calculate for authority. The BtSout are accessible from AND gates at extreme left & right of circuit. In the below figure, this issue is resolved such that both shifted out bits are given input to the OR Gate. For circuit presented, this will be D3 for LS or D0 for RS. FurtherBtSout is stored in CARRY flag.

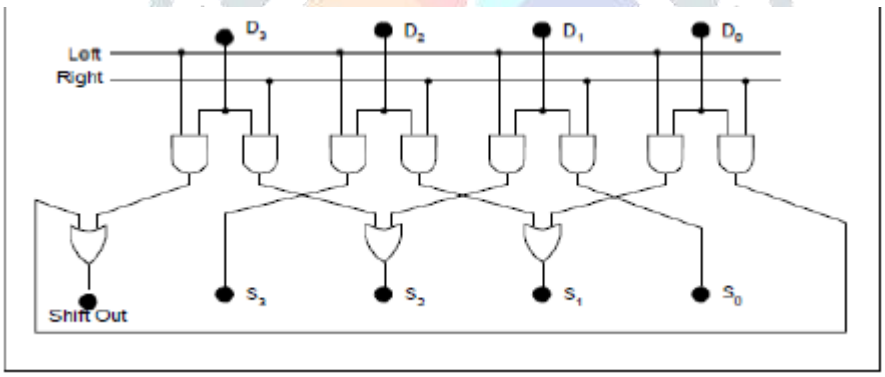

Fig.5 Modified Structure of 4-bit Barrel Shifter

Analysis and Simulated Results

We have planedprojected 4 bit BS Schematic is presented in Fig.5. Vpulse is input that we have shown to shifter. There are 4 inputs namely D0, D1, D2, D3.Here D0 is takenas LSB & D3 is taken as MSB of input bits.

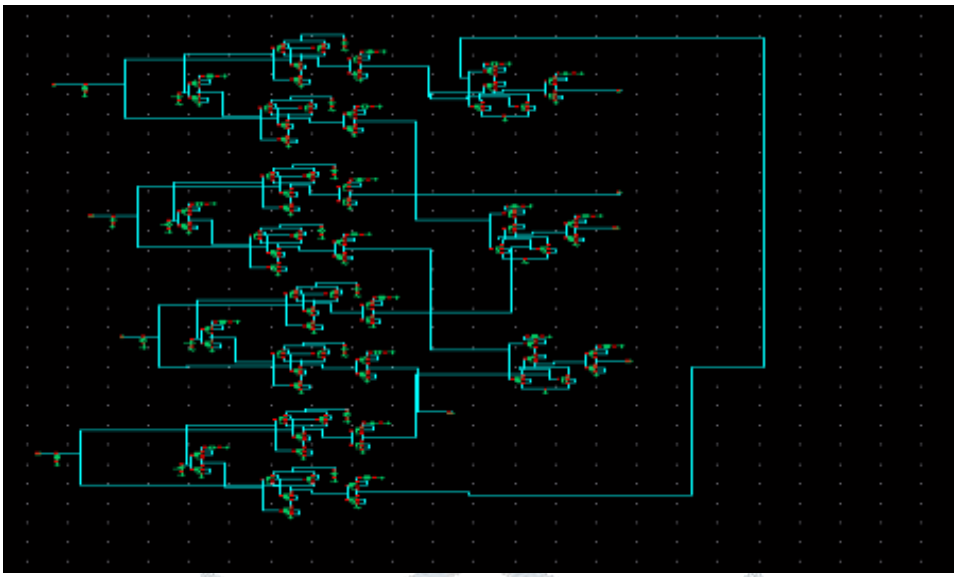

Fig.5 Schematic of Modified 4-bit Barrel Shifter

Now if we choose LS as functionutilizing control bits (0,0) in multiplexer we get beneath output. If S0,S1,S2,S3 are taken as outputs &taking S0 as LSB & S1 as MSB, then in LS S0 is assumed as 0 & DO,D1,D2 are moved to S1,S2,S3 correspondingly. The similar we have got in output.S0 bit has 0 values&overall another bitisimmediately shifted edition of input.

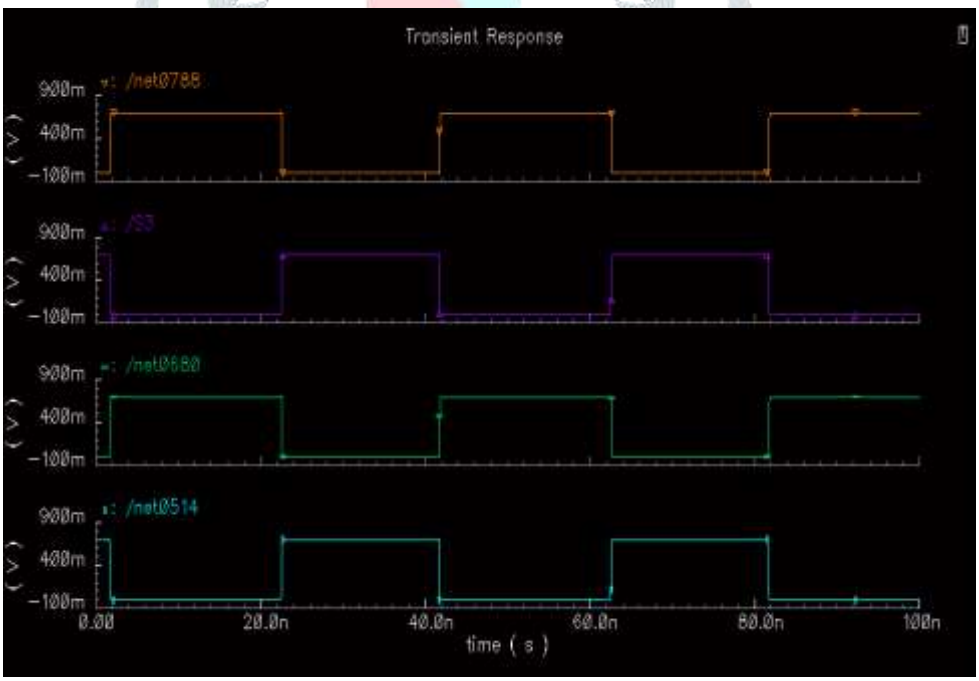

Fig.**6 Left Shift**

Now if the control bits are (1, 0) then Right ShiftOperation is performed on the input.0 is moved to S3 & D3, D2, D1 is moved to S2, S1,& S0 correspondingly. The output of RS isvisible in Fig.7and as we can see S3 has 0 value and allthe other bits are shifted version of the input.

Figure 14:

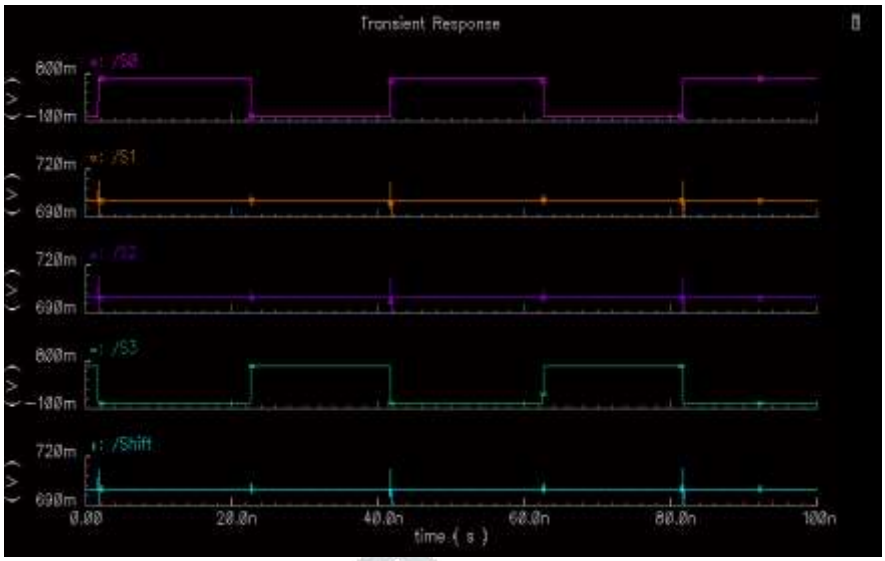

Fig.7 Right Shift

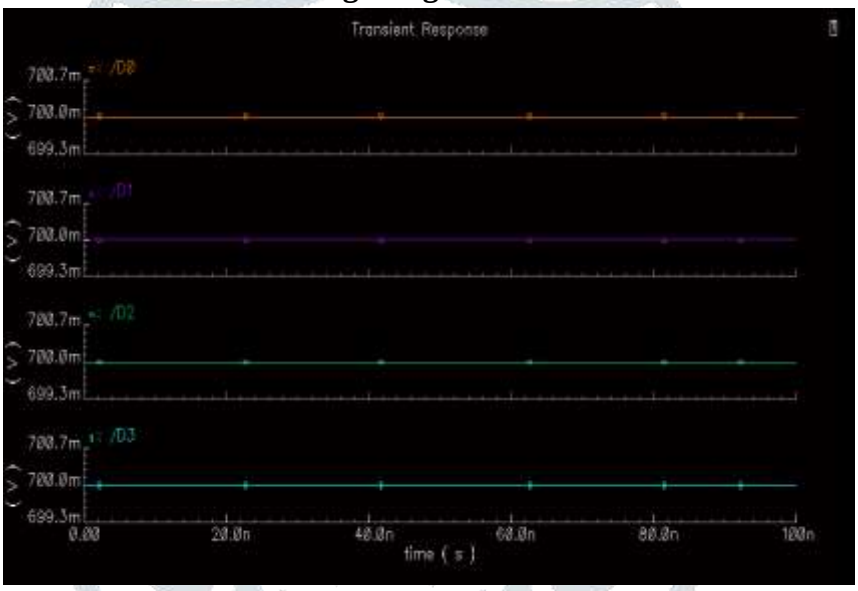

Fig.8 Output of 4-bit Barrel Shifter

A. Power Analysis

Power Analysis in the 4-bit Barrel Shiftereither the transistors are in off mode or in on mode due to the early switching of opposite level, for the 90 nm and 45nm technology, as shown in figure.9 and figure 10, with 4-bit Barrel Shifterin consumes a power off 5.6 µW at 1.5 V supply voltage, it consumes power 2.4 µW at 1.2 V supply voltage, so, achieved a power reduction is less in case of both supply voltage. But in case, we reduces supply voltage more it reduces power more 1.3µW.And also varied supply voltage and shows the change in power for 90 nm and 45nm technology.

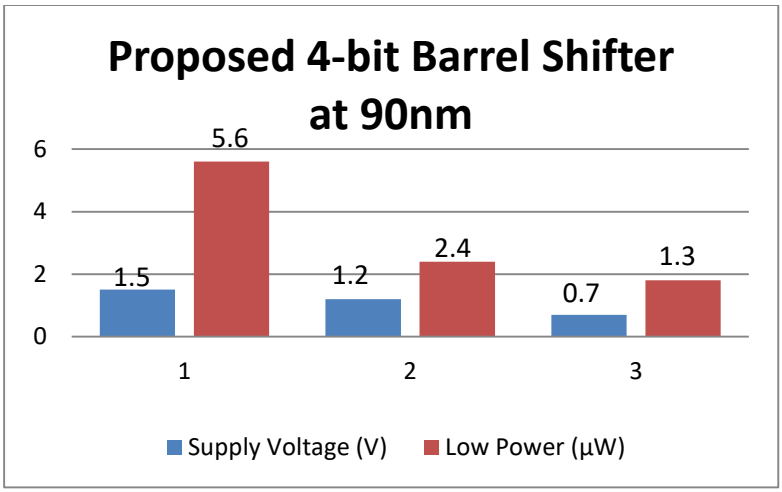

Fig.9 Comparison of Low Power at 90nm

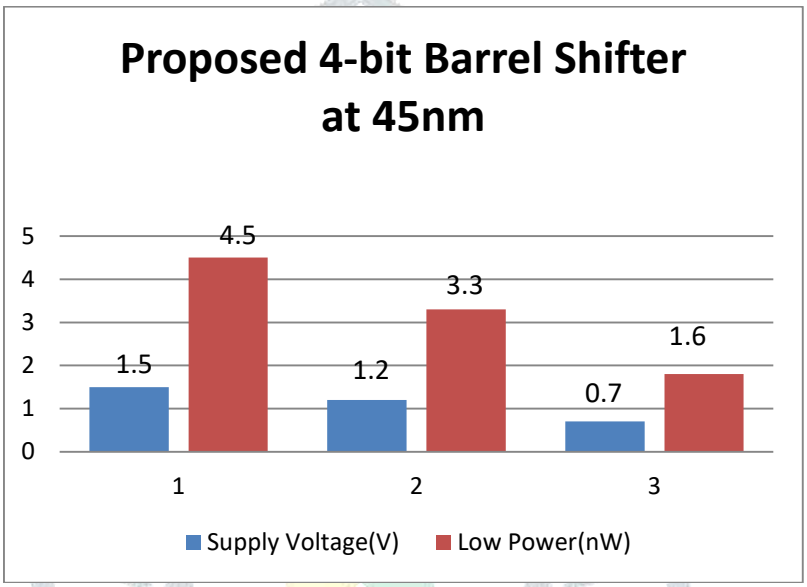

Fig.10 Comparison of Low Power at 45nm

B. Propagation Delay

Proposed 4-bit Barrel Shifteris used in place of Arithmetic and the LogicalShifters and reduce delay as well as power consumption. Therefore a Proposed 4-bit Barrel Shiftercan bedesigned to switch faster than Arithmetic and the Logical Shifters leading to a reduction in delay, the adjustable low-voltage threshold of 4-bit BS function at changeable supply voltage. The time in use for a 4-bit Barrel Shifterlogic gateoutput to change after one or more inputs have changed isknown as propagation delay. Propagation Delay of 4-bit Barrel Shifter at 90nm and 45nm are shown in Figure11 andFigure12.

The Delay of the through during a signal transition is given as:

$$Delay = 0.69R_{eq} \times C_L$$

Where in equationis the R_{eq} resistance that isimplemented using the feed through cell and $C_L$is the loadcapacitance.

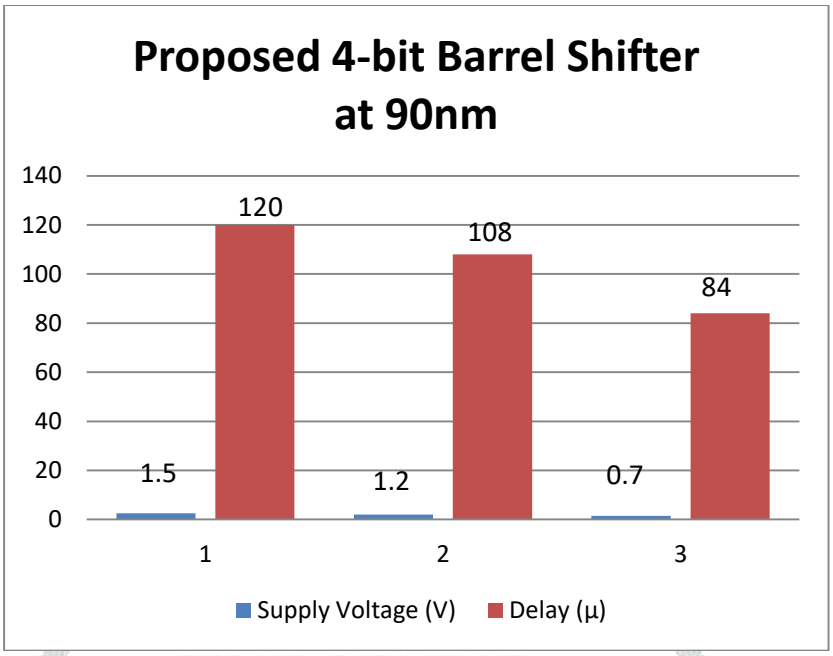

Fig.11 Comparison of Delay at 90nm

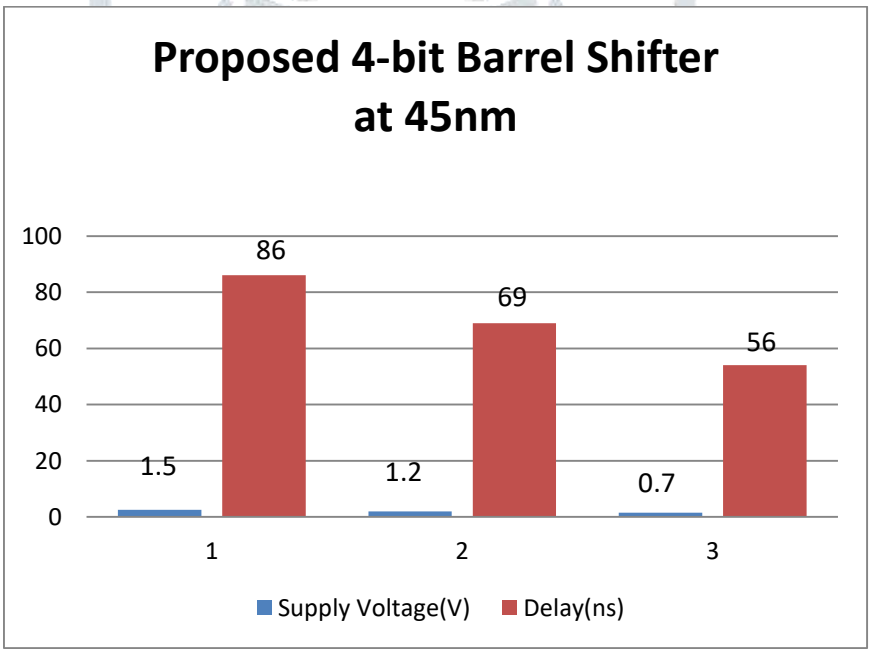

Fig.12 Comparison of Delay at 45nm

Estimated Result Analysis of 4-bit Barrel Shifteron the basis of different supply voltageis shown below table 1 and table 2.

Table 1 Simulated Result Summary

Performance Parameter	**Proposed 4-bit Barrel Shifter**

Technology used	90nm		
Transistor counts	68		
Transistor Sizes	W(Width)=120nm, L(Length)=100nm		
Supply Voltage	1.5V	1.2V	0.7V
Low power	5.6µW	2.4 µW	1.3µW
Delay	120µs	108µs	84µs

Table 2 Simulated Result Summary

Performance Parameter	**Proposed 4-bit Barrel Shifter**		
Technology used	45nm		
Transistor Sizes	W(Width)=120nm, L(Length)=100nm		
Supply Voltage	1.5V	1.2V	0.7V
Low power	4.5nW	3.3nW	1.6nW
Delay	86ns	69ns	56ns

Conclusion

This paper proposes the transient response analysis of shift bit and estimated Power and Delay of Proposed 4-bit Barrel Shiftercircuit whichwill give noisy input signals with less noise response and also applicable for low power.68Transistorused CMOS 4-bit Barrel Shifterhave been simulated on cadence tool, low power requirement of VLSItechnology for battery operated circuits power reduction isimportant key factor, so we are configured low power high performance 4-bit Barrel Shifter.The BS is commonlyutilized for generalization of DS. The AS&LS can also be exchangedviaBS as with revolution of data it also require application DR, LSwhichever arithmetically or logically. The function of this paper is to plan4 bit BS utilizing universal gates with help of CMOS logic. The additionalcomplexedition of BS is 4 bit DS, that is also projected here. The paper compares delay, optimizes &analyzes & power of projected 4 bit BS.

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