Performance and Analysis ofResilient 6T SRAM cell For Low Leakage and high speed CMOS

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Abstract—Low power VLSI system**,** Static random access memory (SRAM) is crucial circuits**.**In this paper leakage current and leakage power of conventional 6T cell at90nm technology has been estimated and circuit techniques to reduce Leakage in deep sub micronlike Sizing of transistor & Power Gating has converse&functional on conventional 6T SRAM cell. By sizing of transistors in 6T SRAM cell an optimized 6TCache memory cell is attain&evaluated&set up for additionalcapable than conventional 6T SRAM Cell. Afterthat Power Gatingis applied on the optimized 6TSRAM cache memory Cell and it is establish to be most efficient interms of leakage current and leakage power&develop speed of circuit.

Keywords**:** ***SRAM 6T Cell, Leakage Power Leakage Current, Power Gating, Cadence tool***

INTRODUCTION

Minimum feature size scaling driven by Moore's law ledto enhance count of transistors & so functionality of chip. Severallatest applications emerged like smart phones, tablet devices&wireless sensors. In these devices,prolong the battery life is the fundamental design issue.SRAM arrays engageadditional than 90% of die region inmodern SOCs as per to ITRS predictions [1], so its powerdominates all power utilization. Supply voltage (SV) scaling is most effectualbehavior to diminish power consumption of digital circuits &system is motivating for SRAM designer as there are vast amount of literatures thatspotlight on near or sub threshold SRAM cell plan. Conventional 6T SRAM cell formation has better density, presentation& reliability for 180 nm, 90 nm &65 nm CMOS systems at SV greater than 0.8 V [2]. Low supply voltage (LSV)functionraise sensitivityto all kinds of variations &region severe duress on SRAMfunctionality likebad read stability & write ability (WA),small on / offcurrent ratio, etc. [2]-[3]. Various systems have been presented to resolve challengeof 6T SRAM cell function at LSV. Forexample, weakening positive feedback is utilized to improveWA [4], [5]. In [4], writer utilizes one NMOStransistor among back-to-back inverters. Turning off thistransistor in write functionuse positive feedback weak&improveWA.

A low power characteristic based layout design of 6T[6] architecture. In this Operational circuit has 2 stable states&evaluate to logical "0" & "1" states. Theseother transistors are used for operating such as

implementing extra ports in a register file, etc for the SRAM memory cell. Operational Concept of SRAM memory cell shown in figure1.

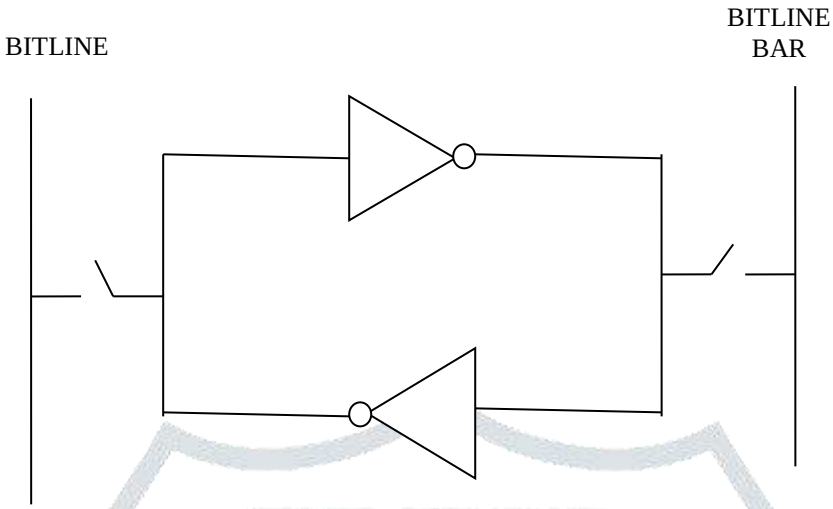

Figure1. Operational concept of SRAM Cell

As presented in exceedingdiagram inverters are linkedflipside to form latch. These are connected by two bit line and bit line bar. Access transistors are connected between bit line and bit line bar, to read or write the data in memory. While any three terminal switch device can be used in an SRAM, MOSFETs and in particular CMOS technology is usually used to make certain that very low levels of power consumption are achieved. With semiconductor memories enhancing to very large proportions, each cell must achieve very low levels of power consumption to make certain that the overall area of chip does not dissipate additional power. Power reduction can be achieved by diverse methods like, dual threshold based operation of SRAM circuit [7], by using a customized architecture that reduces the power in data write [8] operation or data read operation, etc.

1. Architecture of 6T SRAM Cell

The Architecture of standard cell have6transistor as presented in fig.2 nMOS access transistors (AT) (N3 and N4) located at ends of circuit & pair of back to back inverters engage of memory cell. The nMOS element (N1 and N2) of latch are driver transistors, while pMOS (P1 and P2) are pull-up transistors. The ATfunctionswhile word line (WL) is raised, for read or writes function, linking cell to bit lines (BL) (Bitline, Bitline bar). Therefore, cell cannot be accessed and two cross-coupled inverters will continue to feed back each other, as long as they are connected to the supply, and data will hold in latch. The read operation beginsvia pre-charging BL high, then permitting them to float. Then, WL is asserted, turning on all AT. The data stored in nodes are driven onto BL. Voltagedissimilarity is grownamong BL & sense amplifier detects value of cell.

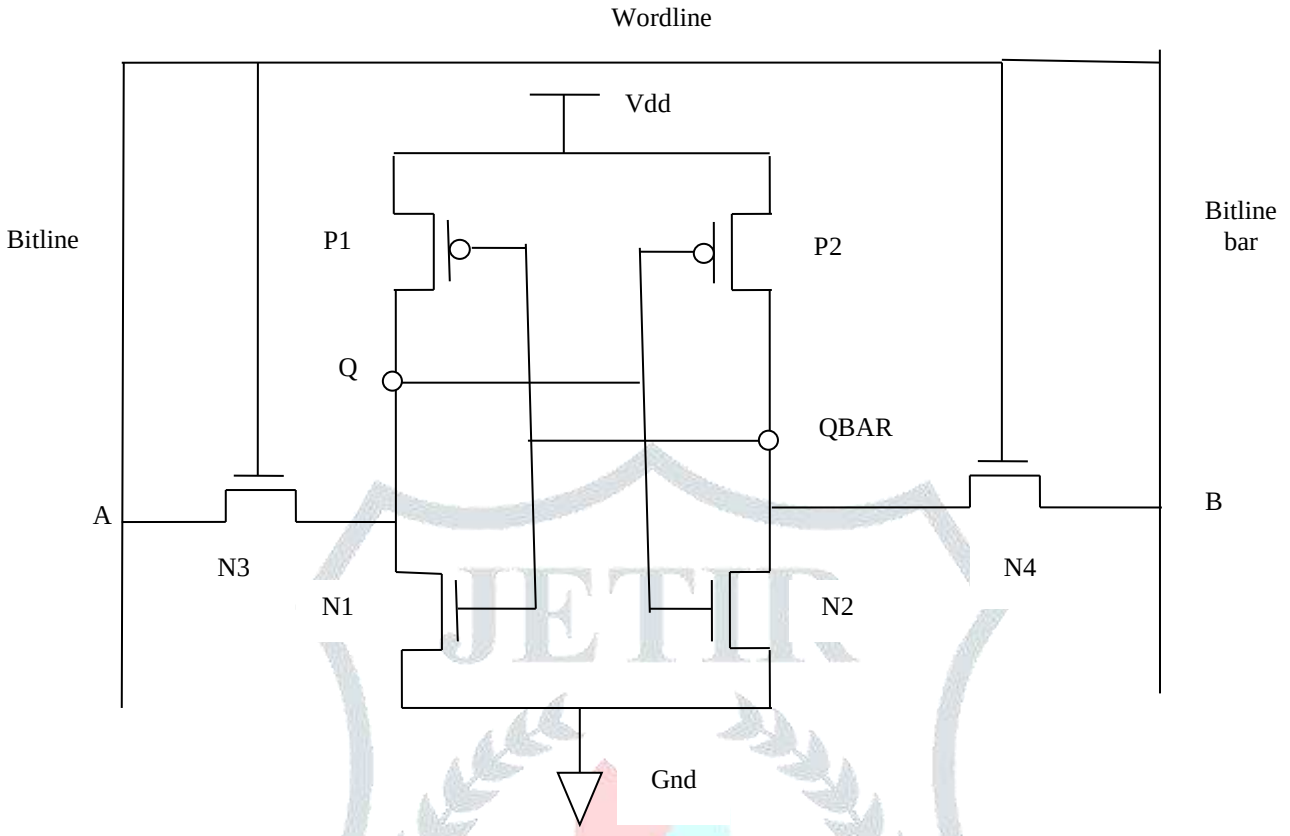

Figure2. Standard Architecture of 6T SRAM Cell

During write operation, BL are resolute to complementary voltage levels & then WL is improved. The data to be written in cell are resolute on BL & one of storage nodes is discharged thruAT. The back to back inverters enhance the voltage on the opposite storage node and latch the cell. Thus, the new data overpowers the back to back inverters. The crucialdispute in SRAM plan are reducing its size &ensure that circuitry handlingsituation is weak adequate to be overpowered whenwrite cycle(write ability), yet strong sufficient not to be disturbed while read cycle (read stability).

To read a "A=0", whileWL at 0V, mutually AT are in off mode. Pre-charge mutuallyBLhigher then WL will go higher.If a "A=0 B=1" is stored, then Wordline is High causes N3 to pass 0V to N2/P2, Vdd to N1/P2 Charge flow P2>N4, thus charging the bit line voltage. Charge flow A1>N1, so discharging BL voltage.

To read a "A=1", WL at 0V, mutuallyAT transistors are in off mode. Pre-charge equallyBL maximum Vdd then WL will go maximum. If a "A=1 B=0" is stored, then Wordline=High causes N3 to pass Vdd to N2/P2, 0V to N1/P1,Charge flow N4>N2, thus discharging the bit line voltage. Charge flow P2>N3, so charging BL voltage.

To write a "1", initially at a "0", WLline at 0V, mutually AT are in off mode. Pre-charge one bit line high (D=B=Vdd), the other low (D=B=0V) then the wordline will go high. Source (B) of N3 goes to 0>Vdd-Vt, and drain (B) of N4 goes to Vdd>0V. Positive feedback takes over &cell stores a "1" on A.

To write a "0", initially at a "1" WL at 0V, mutually ATin off mode. Pre-charge one BL maximum (B=Vdd), another to ground (B=0V) then WL will go maximum. Source (B) of N3 depart to VDD>0V &drain (B) of N4depart to 0> (VDD-Vt), Positive feedback takes over &cell stores a "0" on A.

- **CIRCUIT TECHNIQUE TO REDUCE LEAKAGE IN DEEP SUB MICRON**

Among the emerging leakage reduction techniques, some mustvariation of the performance of the circuit and proceduresystem, attain leakage diminutionwhile fabrication/design stage, as another are considered on circuit-level optimization system that attain architectural support, and in some cases, technologysupport as well, but are applied at run-time(dynamically).In this section various circuit level leakage reductiontechniques in deep sub micron have been discussed that have been proposed and are being used to reduce the static power dissipation in SRAM cell [9-10].

A. Sizing of SRAM Cell

The subthreshold leakage (STL) is draining supply current oftransistor operating in weak inversion region (IR).As like strong IR in thatsub threshold (ST), drift current dominates conduction is because of diffusion current of minority carriers in channel for MOS tool. The magnitude of ST current is operation of device size, temperature, process parameters&supply voltage out of which threshold voltage (TV) plays dominant role. In current CMOS system, STL current (STLC), ISUB, is greatlybigger than other leakage current components. This mostlydue of relatively low VT in modern CMOS tools. ISUB is evaluatedvia utilizing following formula:

ST current happensamong drain &supplywhile transistor is operating in weak IR that is the gate voltage is lower than the V_{th}. The STLCfor MOSFET tool can be uttered as:

$$I_{subthreshold} = I_0 e^{\frac{(Vgs-Vth)}{nV_T}} [1-e^{-(\frac{V_{ds}}{V_T})}]$$

Where,

$$I_0 = \frac{W \mu_0 C_{OX} V_T^2 e^{1.8}}{L}, \; V_T = \frac{KT}{q}$$

is TV, $V_{th}$is threshold voltage, $V_{ds}$and $V_{gs}$are drain-to-source & gate-to-source voltages correspondingly. W &L are effectual transistor width & length, correspondingly. $C_{ox}$is gate oxide capacitance, μ_0 is carrier mobility &n is ST swing coefficient.

As it is visible that STLC,Isub depends on Width & Length of transistors.So by havingsuitablevalues for TVit will get relation for width & length to attainsmallest leakage power & leakage current.

B. Power Gating Technique

Power Gating enables a cache to "turn off" the supply voltage and eliminate virtually all the leakage energy dissipation in the cache's unused sections. The key thought is to initiate an extra transistor viamaximum VT in supply voltage (VDD) or ground path (gnd) of cache's SRAM cells while rest all transistors of the cell have low VT shown in Figure3.

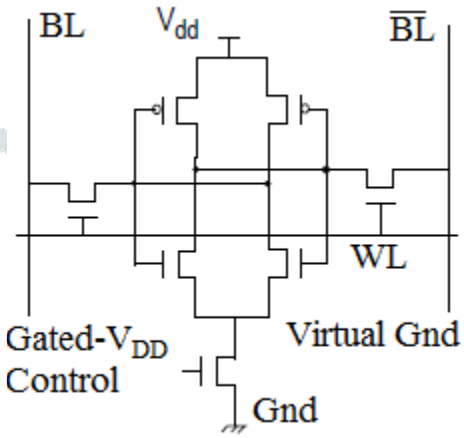

Figure3: SRAM cell with an NMOS Power Gating

The extra transistor is turned on in utlizingpart&turned off in unused part. Thus, the cell"ssupply voltage is "gated." Power Gating sustainpresentationbenfits of lower supply &TV whendropping leakage & leakage energydissipation.

CIRCUIT SIMULATION & RESULT ANALYSIS

The Conventional 6T SRAM Cell at 90 nm system is consider in conditions of leakage power (LP) dissipation& leakage current& performance. Later thandiverse circuit level leakage reduction techniques have been applied and analyzed. LP in cell has been estimatevia keeping WL low to cut off cell fromBL. 2 module of leakage have been consider, 1leakage inside cell &other leakage to BL.CadenceAnalog Design Environment atGPDK 90nm technology is used for schematic Circuit designand simulation purpose. The waveforms of the transientanalysis and DC Response have been showed in this section. The results areshown in the terms of leakage Current and leakage Power.

i.Conventional 6T SRAM Cell

Diagram 4showsillustration of Conventional 6T SRAM Cell. Itintendedrequire2 cross-coupled CMOS inverters &2AT, linking cells to BL.

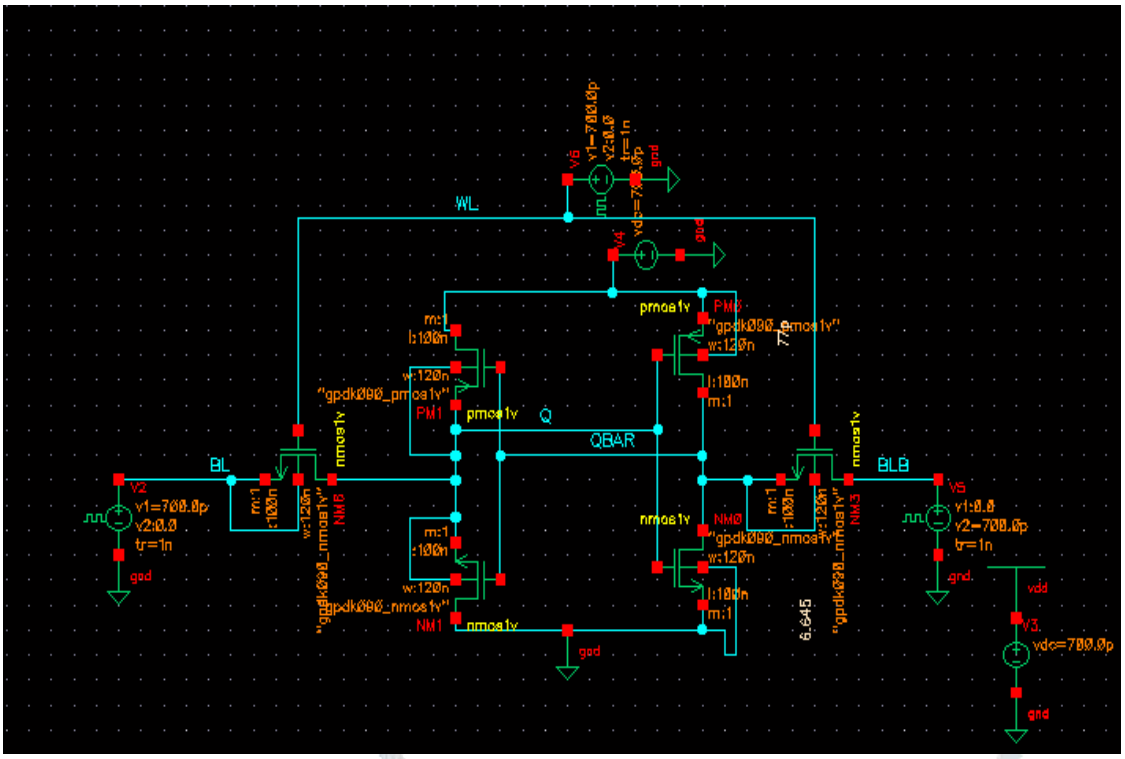

Fig. 4: Schematic of Conventional 6T SRAM Cell

Transient Analysis (TA)

Diagram 5 showsTAwaveform& DC response of Conventional 6T SRAM Cell.For the simulation purpose, supply voltage of0.7 V is used. The Leakage Current and Power is calculated for the giveninput stateand estimated results have been shown in table1.

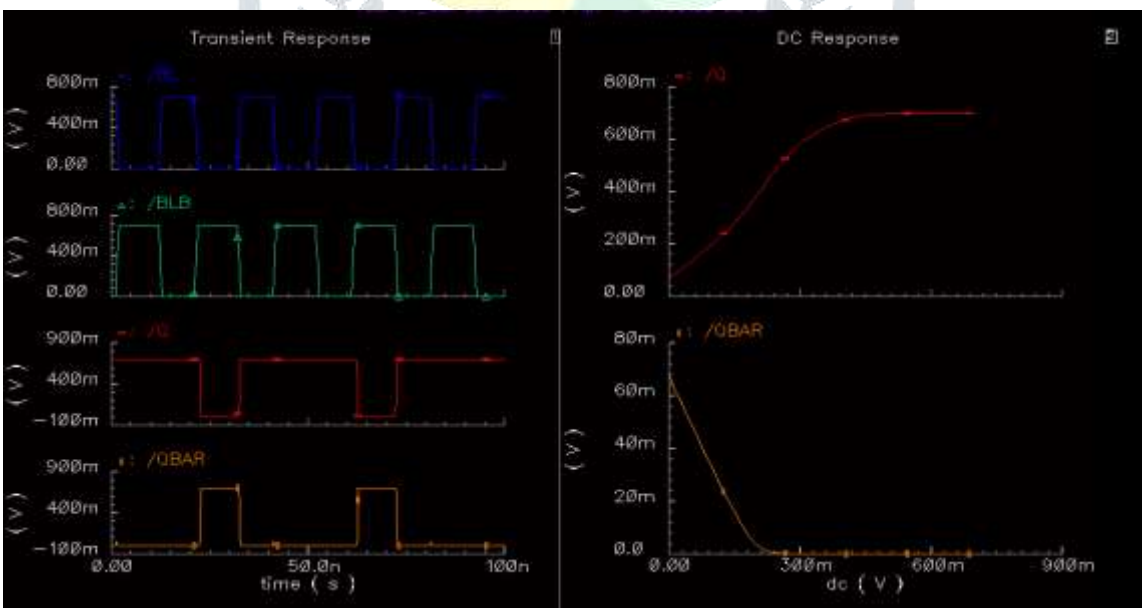

Figure 5 shows the transient analysis waveform and DC response

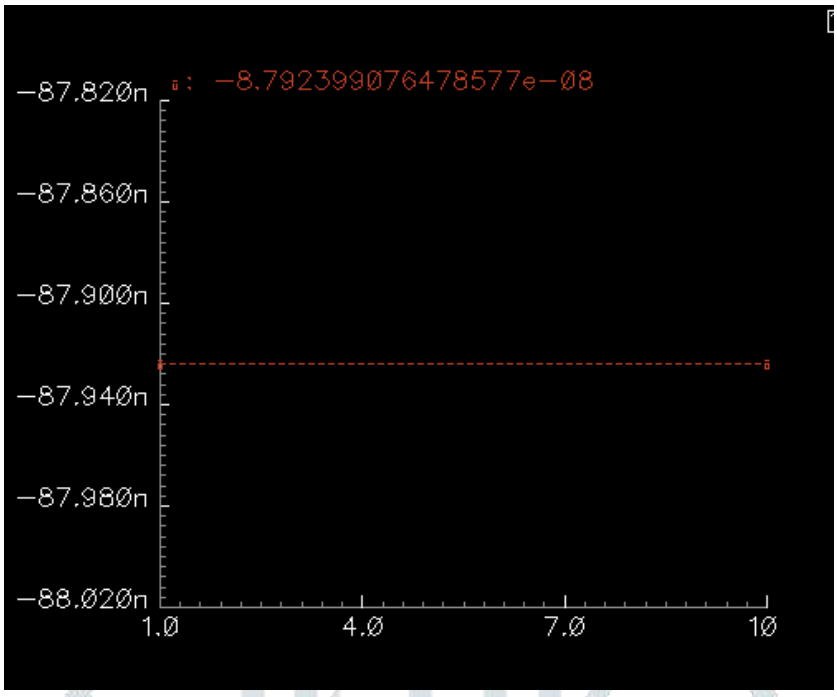

Figure 6. Leakage Current Waveform

Table 1: Results obatinedby Transient analysis ofConventional 6T SRAM Cell.

Technology		GDPK 90nm	
Power Supply		.7 V	
Temperature		27º C	
Run Time		100ns	
Sizing of Transistor	PMOS (Inverter)	W=120 nm	L=100nm
	NMOS (Inverter)	W=120 nm	L=100nm
	NMOS (Access Transistor)	W=120 nm	L=100nm
Leakage Current		0.85nA	
Leakage Power		0.59nW	

ii.Power Gating6T SRAM Cell

Fig. 7 shows the schematic of the Power Gating 6T SRAM Cell. Its systemhave2 Back to Back CMOSinverters, 2 AT, linking AT to BL& BL bar& NMOS transistor in ground direction of 2 Back to Back CMOS inverters.

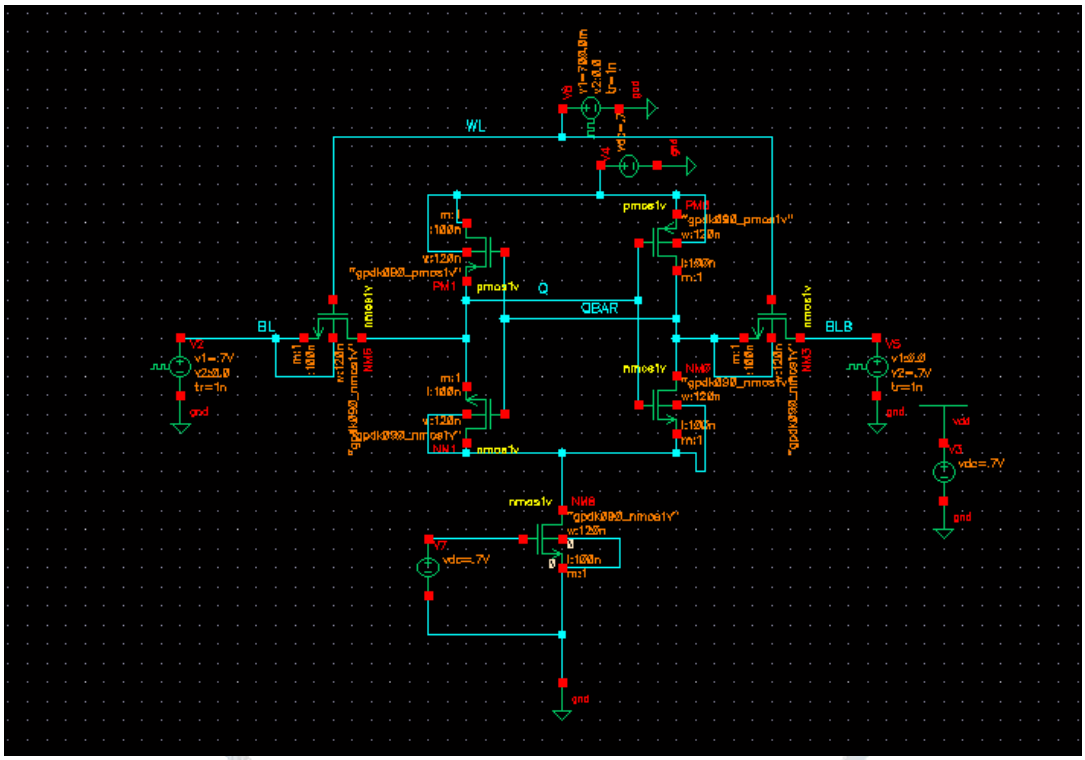

Fig. 7: Schematic of Power Gating 6T SRAM Cell

Transient Analysis

Figure 8 shows the transient analysis waveform and DC response of Power Gating 6T SRAM Cell.For the simulation purpose, supply voltage of 0.7 V is used. The Leakage Current and Power is calculated for the giveninput stateand estimated results have been shown in table2.

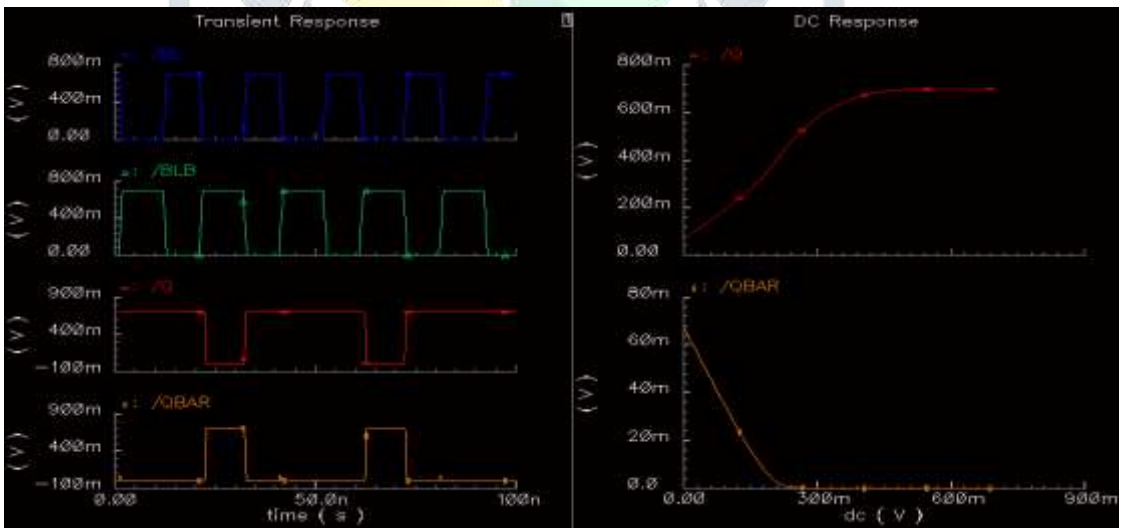

Figure 8 shows the transient analysis waveform and DC response

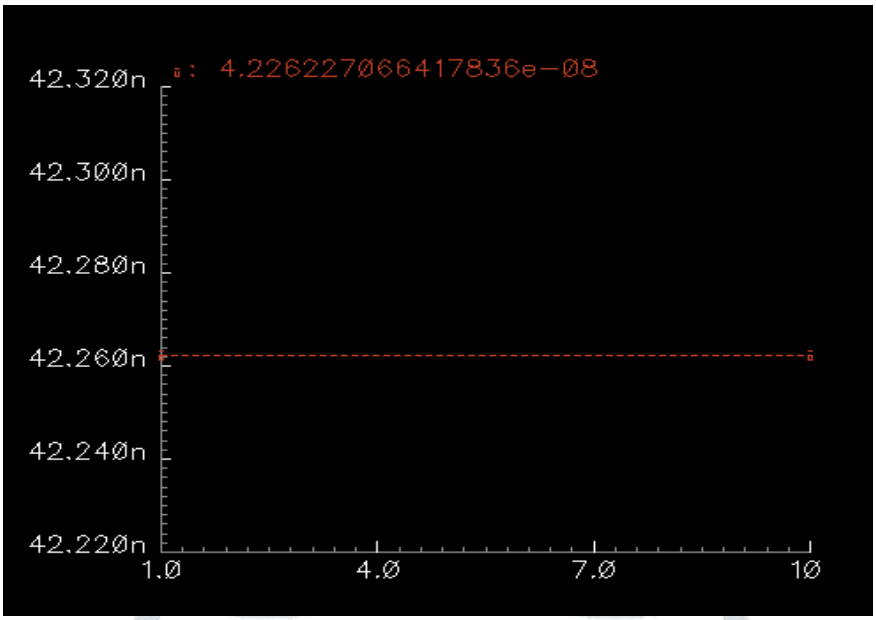

Figure 9. Leakage Current Waveform

Table 2: Results obtained from Transient analysis ofPower Gating 6T SRAM Cell

Technology		GDPK 90nm	
Power Supply		.7 V	
Temperature		27° C	
Run Time		100ns	
Sizing of Transistor	PMOS (Inverter)	W=120 nm	L=100nm
	NMOS (Inverter)	W=120 nm	L=100nm
	NMOS (Access Transistor)	W=120 nm	L=100nm
	NMOS (Gated Transistor)	W=120nm	L=100nm
Leakage Current		0.42nA	
Leakage Power		0.29nW	

iii.Optimized 6T SRAM Cache Memory Cell (CMC)

The representation of optimized 6T SRAM CMCis presentated in diagram.10. Its Schematic includes two Back to Back CMOSinverters and two access transistors, connecting access transistors to the bit-line, bit line bar and word line.

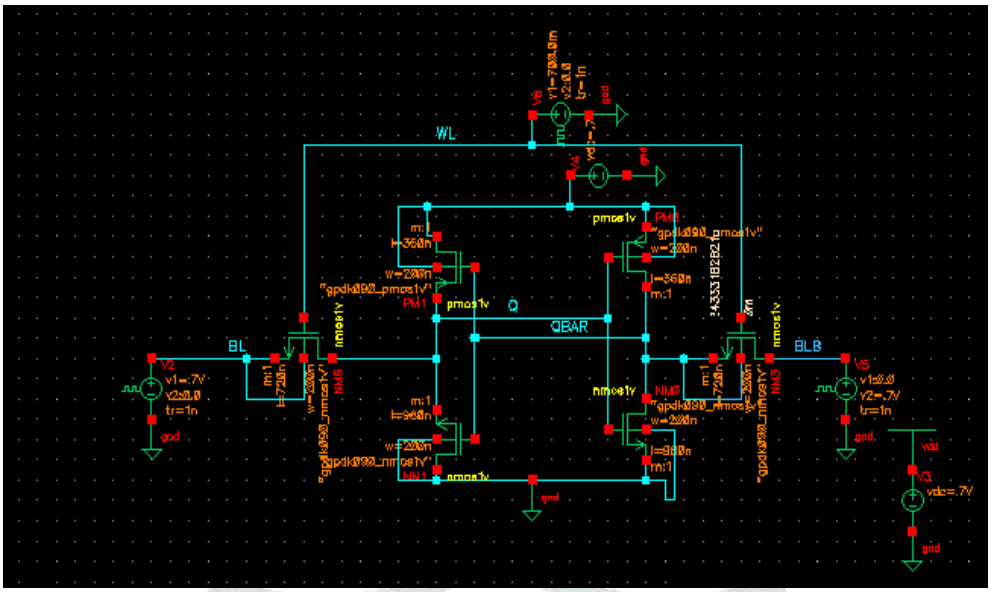

Fig. 10:Schematic of Optimized 6T SRAM CMC

Transient Analysis

Diagram 11 showsTA waveform & DC response of Optimized 6T SRAM CMC. For simulation intention, supply voltage of 0.7 V is used.The Leakage Current and Power is calculated for the giveninput stateand estimated results have been shown in table3.

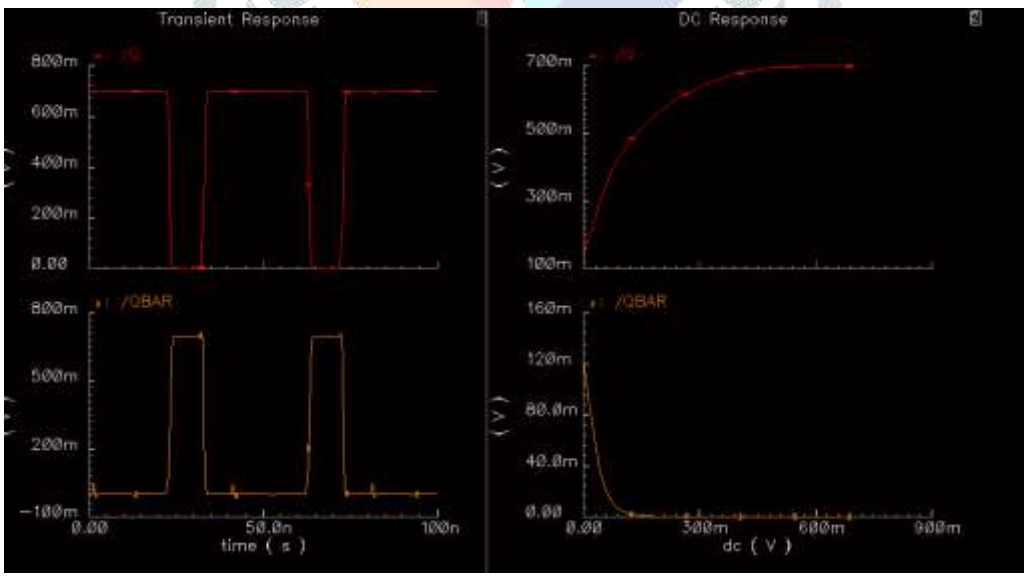

Figure 11 shows the transient analysis waveform and DC response

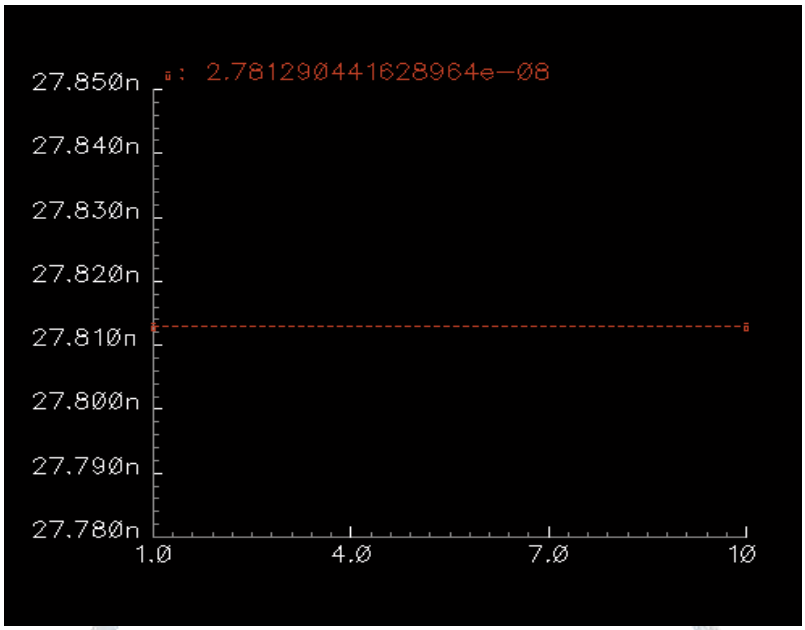

Figure 12. Leakage Current Waveform

Table 2: Resultattained from Transient analysis of Optimized 6T SRAM cache memory Cell

Technology		GDPK 90nm	
Power Supply		.7 V	
Temperature		27° C	
Run Time		100ns	
Sizing of Transistor	PMOS (Inverter)	W=200 nm	L=360nm
	NMOS (Inverter)	W=200 nm	L=960nm
	NMOS (Access Transistor)	W=200 nm	L=720nm
Leakage Current		0.27nA	
Leakage Power		0.50nW	

iv.Optimized Power Gating 6T SRAM Cache Memory Cell

Figure 13 shows the schematic of the Power Gating 6T SRAM Cache Memory Cell. Its systemhave 2 Back to Back CMOS inverters, 2 AT, linkingAT to BL&BL bar & NMOS transistor in ground way of 2 Back to Back CMOS inverters.

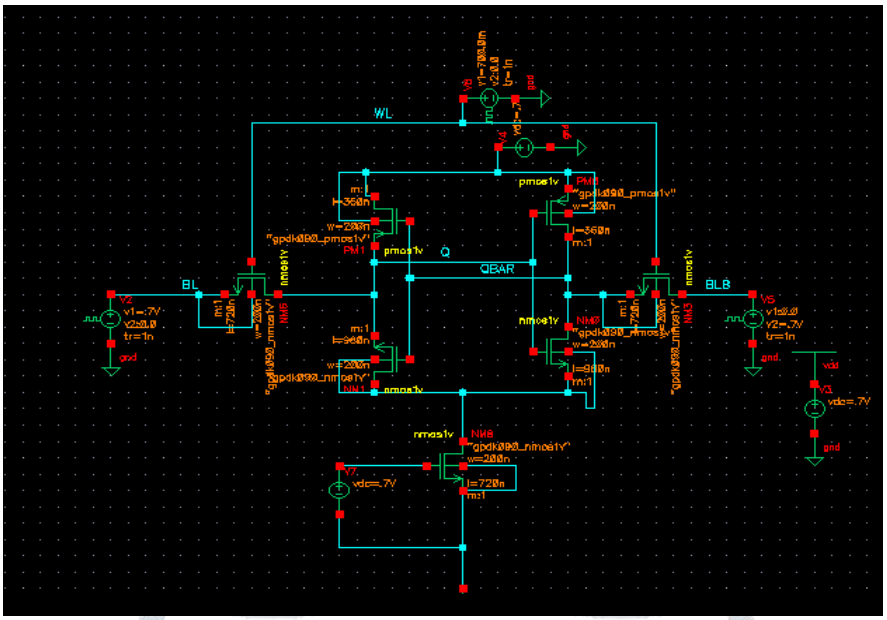

Fig. 13: Schematic of Power Gating 6T SRAM Cache Memory Cell

Transient Analysis

Figure 14 shows the transient analysis waveform and DC response of Power Gating 6T SRAM Cell.For the simulation purpose, supply voltage of 0.7 V is used. The Leakage Current and Power is calculated for the giveninput stateand estimated results have been shown in table2.

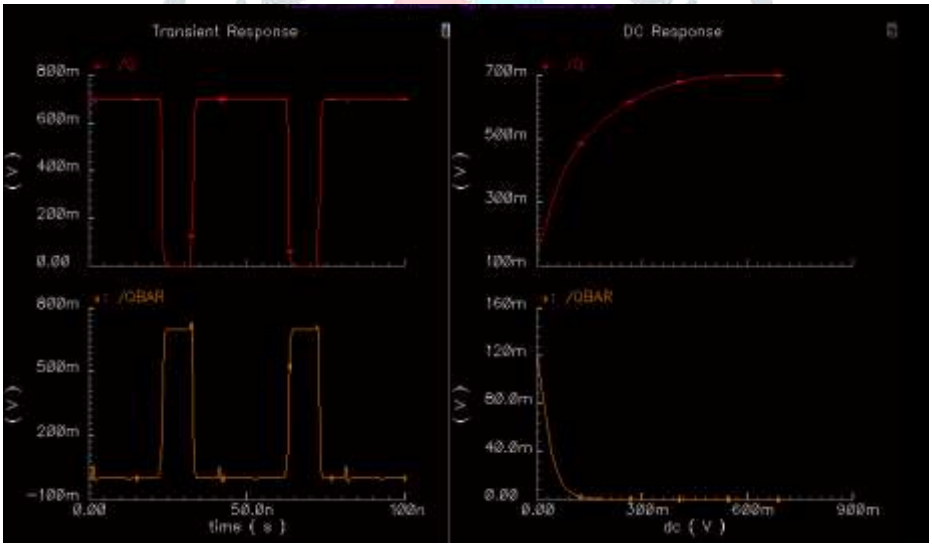

Figure 14 transient analysis waveform and DC response

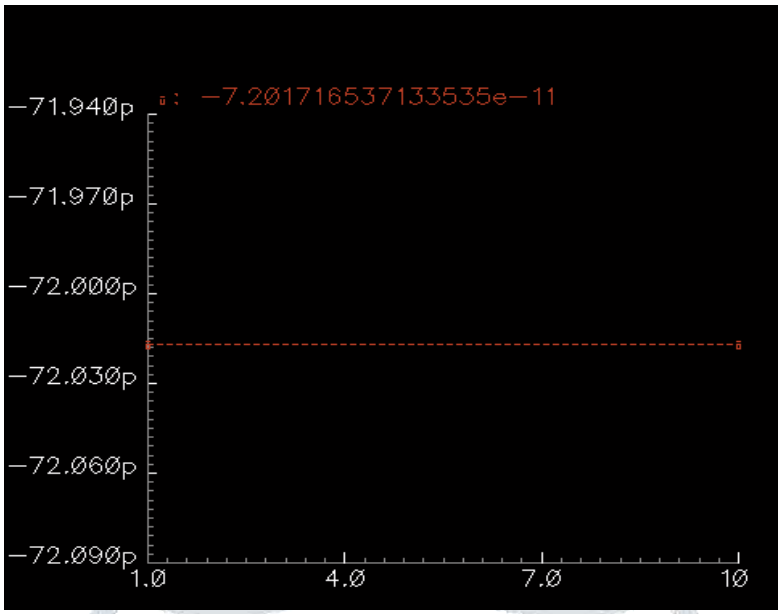

Figure15. Leakage Current Waveform

Table 4: Results obtained from Transient analysis of Power GatingOptimized 6T SRAM Cache Memory Cell

Technology		GDPK 90nm	
Power Supply		.7 V	
Temperature		27º C	
Run Time		100ns	
Sizing of Transistor	PMOS (Inverter)	W=200 nm	L=360nm
	NMOS (Inverter)	W=200 nm	L=960nm
	NMOS (Access Transistor)	W=200 nm	L=720nm
	NMOS (Gated Transistor)	W=200nm	L=720nm
Leakage Current		0.72pA	
Leakage Power		0.54pW	

Summary of Results

Later than simulating and analyzing the 6T SRAM Cell, the results comparisons havebeen summarized in table below. Table.5 presents comparison of diverse reduction system in SRAM 6T SRAM Cell.

Table 5: Comparison of leakage ReductionTechniques in 6T SRAM Cell

Leakage Reduction	Leakage Power	Leakage Current

Techniques		
Conventional 6T SRAM cell	0.59nW	0.85nA
Power Gating 6T SRAM cell	0.29nW	0.42nA
Optimized 6T SRAM Cache Memory cell	0.50nW	0.27nA
Optimized Power Gating 6T SRAM Cache Memory Cell	0.54pW	0.72pA

CONCLUSION

Circuit techniques to reduce Leakage in deep sub micron such as Sizing of thetransistor and Power Gating has been discussed andapplied on conventional 6T SRAM cellfor leakage power and Leakage Current reduction andcompared with Optimized 6T SRAM cache memory cell and its circuit speed enhances. Out of all the techniques discussed optimized Power Gating has found to be the best as it reduces more leakage comparable to Power Gating. It has originate that in conventional 6T SRAM cell greatestdiminution in leakage power& leakage current can be obatinedby utlizing circuit system to diminish Leakage in deep sub micron.Optimized Power Gating leakage reduction technique shows large reduction but due to some restrictions in the Power Gtaing SRAM Cell optimized Cache memory circuit via permitting fordifferent parameters.

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