SOLS based Reused Architecture of FM0/Manchester/Miller Encoding for DSRC Applications

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*Abstract : **The Dedicated Short Range Communication benchmarks normally embrace FM0 and Manchester codes to succeed in dc-equalization, improving the sign responsibleness. Still, the coding-assorted qualities between the FM0/Manchester and Miller codes genuinely restrict the possibility to style a totally reused VLSI outline for each. And this paper, the similitude arranged rationale improvement (SOLS) procedure is anticipated to beat this restriction. The SOLS system enhances the equipment use rate from 57.14% to 100% for each FM0/Manchester and Miller encodings. The proposed system for clock gating techniques used in FM0/Manchester and Miller encoding techniques. The clock gating reduced the dynamic power dissipation and also reduced the clock signals. This paper not singularly adds to a totally reused VLSI outline, however furthermore shows Associate in nursing sparing execution contrasted and the prevailing works.***

***IndexTerms* - FM0, Manchester, Miller, DSRC, SOLS**

I. INTRODUCTION

The dedicated short-range communication (DSRC) could be a protocol for one- or two-way medium vary communication particularly for intelligent transportation systems. The DSRC will be shortly classified into 2 categories: vehicle-to-vehicle and vehicle-to-roadside. In, the vehicle-to-vehicle DSRC permits the message causing and broadcasting among cars for issues of safety and public data announcement. the protection problems embody blind-spot, intersection warning, intercars distance, and collision-alarm. Moreover, the ETC will be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays a vital role in fashionable industry. The higher and bottom components ar dedicated for transmission and receiving, severally. This transceiver is assessed into 3 basic modules: silicon chip, baseband process, and RF front-end.
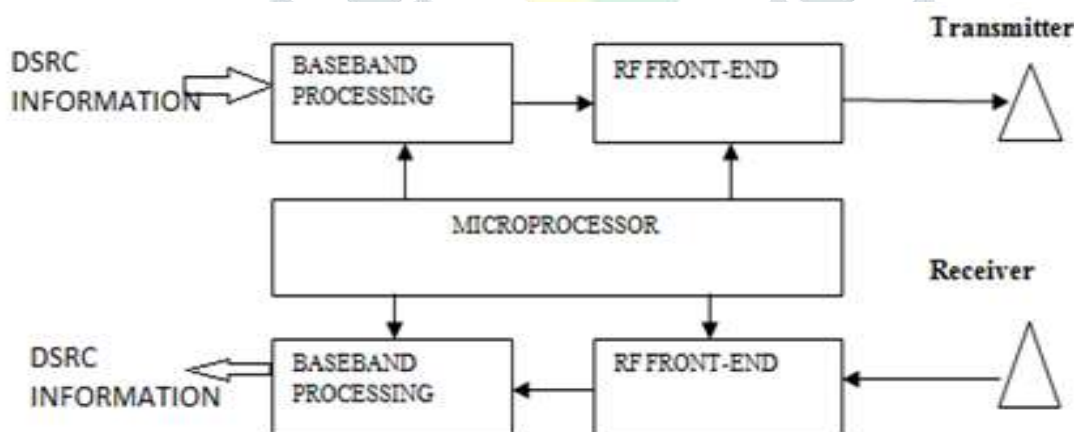

Figure1:DSRC Transreceiver.

- The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end.
- The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding.
- The RF frontend transmits and receives the wireless signal through the antenna.

The DSRC standards are established by many organizations in numerous countries. the info rate one by one targets at five hundred kb/s, 4 Mb/s, and twenty seven Mb/s with carrier frequency of five.8 and 5.9 GHz. The modulation ways incorporate amplitude shift keying, part shift keying, and orthogonal frequency division multiplexing.

In RFID system, the info communication through modulation is transmitted between the tag and reader so as to scale back error rate, gaining DC balance and improve potency, the info is encoded before being modulated. In general, the Manchester and Miller codes will be applied to telecommunication then utilized in the RFID system. The Miller code itself carries „timing" data, which might be extracted the clock signal data in different web site, that is, the code with a self-timing property. Therefore, the Miller code has higher improvement against delay error and noise interference.

II. IMPLEMENTATION

In the proposed system, Miller encoder is also implemented with FM0 and Manchester encoder. The characteristic of the Miller encoding is efficient to that of FM0/Manchester encoding so we can use the Miller encoding for Dedicated Short Range Communication.

FM0 Code: Mode1=0, CLR=1 and Mode2=0
Manchester Code: Mode1=1, CLR=0 and Mode2=1
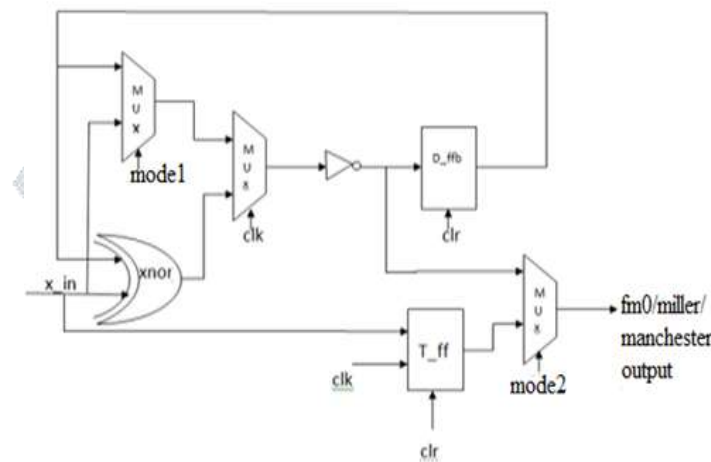Miller Code: Mode1=0,CLR=1 and Mode2=1

Figure 2: proposed system architecture.

Figure 2 shows VLSI architecture design of proposed FM0 Encoder ,Manchester Encoder and Miller Encoder This is the diagram for the FM0/Manchester and Miller encoding. Here the output of the proposed system is depend on the Mode2. If the mode2 is 1, output is FM0/Manchester encoding otherwise output is Miller encoding. For FM0 signals mode1 is 0 , clear is 1 and mode2 is 1. For Manchester signal mode is 1, clear is 0 and mode2 is 1. For Miller encoding , mode is 1, clear is 0 and mode2 is 0.
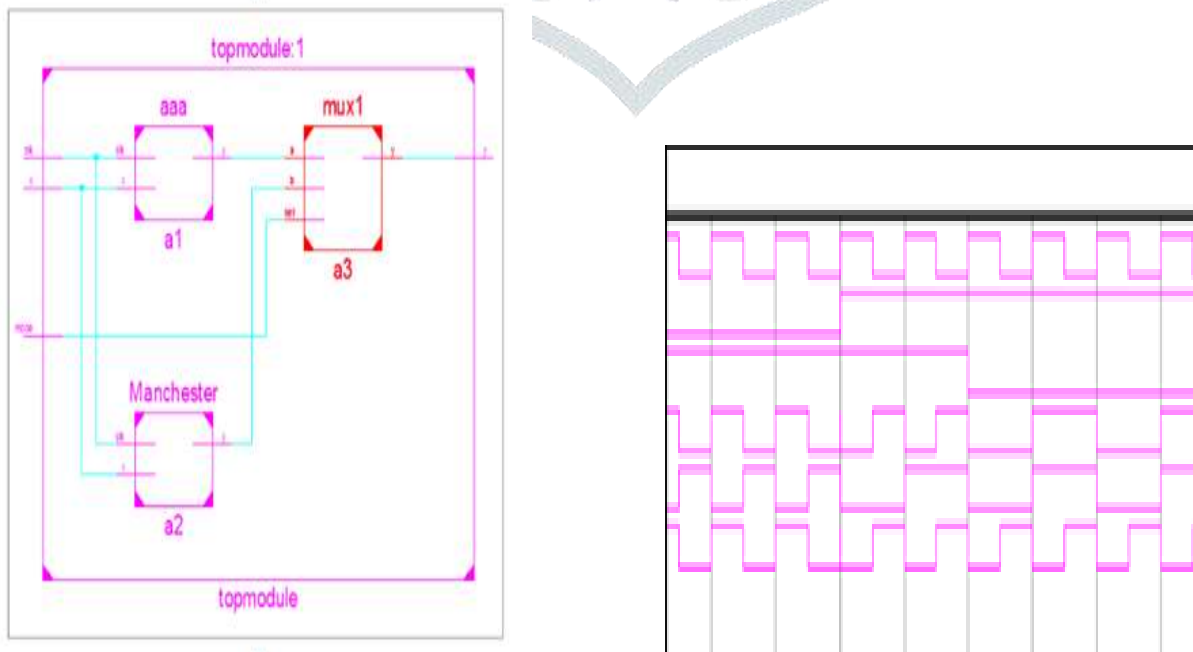
III. SIMULATION RESULTS

Figure 11: schematic of FMO/Manchester Encoding.   Figure 12: Simulation waveform of fm0/Manchester Encoder

Figure 11 and Figure 12 illustrates the implementation of FM0/Manchester Encoding and the corresponding simulation results respectively. Figure 13 depicts the inner blocks of miller coding implemented in VLSI and the corresponding simulation results are illustrated in Figure 14. The timing investigations are confirmed on Xilinx test system. The Xilinx10.1 ISE programming is used in the venture and code is composed on Verilog HDL. The objective FPGA prototyping gadget is fits in with Spartan3E family and the gadget is XC3S200S and package is FT256 which has speed evaluation of -5. The force utilization is 1.48mW and the postponement is 5.776ns. The SOLS procedure gives superior when contrasted with existing articles
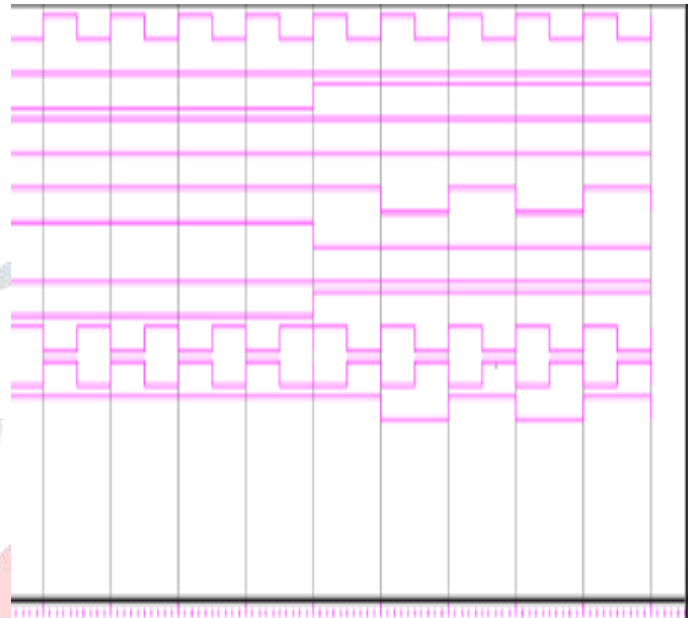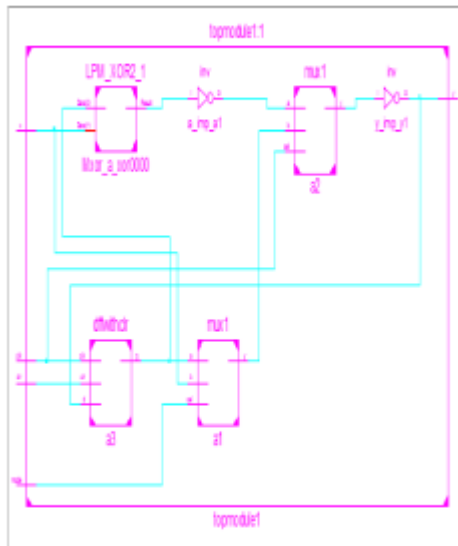

Figure 13 : Internal Blocks of Miller encoder   Figure 14: Simulation Waveform of FM0/miller/Manchester Encoder

IV. CONCLUSION

In this paper the totally reused VLSI auxiliary designing using SOLS technique for FM0/Manchester and Miller encoding. The timing investigations are confirmed on Xilinx test system. The Xilinx10.1 ISE programming is used in the venture and code is composed on Verilog HDL. The objective FPGA prototyping gadget is fits in with Spartan3E family and the gadget is XC3S200S and package is FT256 which has speed evaluation of -5. The force utilization is 1.48mW and the postponement is 5.776ns. The SOLS procedure gives superior when contrasted with existing articles. In future the configuration might actualize utilizing superior FPGA gadgets and the Nanometer might be diminished from 45nm to 32 nm CMOS innovation. The work can be extended by adding buffer of single D-flipflop to increase the driving capability mode of output. By adding buffers in the mode of output more number of outputs can be stored in the output.

REFERENCES

[1] F. Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, et al., "Vehicle safety communications—Applications (VSC-A) final report," U.S. Dept. Trans., Nat. Highway Traffic Safety Admin., Washington, DC, USA, Rep. DOT HS 810 591, Sep. 2011.

[2] J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United States," Proc. IEEE, vol. 99, no. 7, pp. 1162–1182, Jul. 2011.

[3] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich, "Design of 5.9 GHz DSRC-based vehicular safety communication," IEEE Wireless Commun. Mag., vol. 13, no. 5, pp. 36–43, Oct. 2006.

[4] A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, "A 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz," in Proc. 16th Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1–4.

[5] Y.-C. Hung, M.-M. Kuo, C.-K. Tung, and S.-H. Shieh, "High-speed CMOS chip design for Manchester and Miller encoder," in Proc. Intell. Inf. Hiding Multimedia Signal Process., Sep. 2009, pp. 538–541.

[6] Y.-C. Hung, M.-M. Kuo, C.-K. Tung, and S.-H. Shieh, "High-speed CMOS chip design for Manchester and Miller encoder," in Proc. Intell. Inf. Hiding Multimedia Signal Process., Sep. 2009, pp. 538–541.