LOW POWER AND HIGH SPEED DIVERSE DIGITAL CIRCUIT FOR SUB-THRESHOLD LEVEL

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Abstract : Day to day VLSI circuit is becoming more complex in regard of architecture and analysis point of view. A high computation design with less power consumption and miniaturization in the area is implicit to the current semiconductor industry. In these, a methodology for error-control parity generator and checker is fundamental of data communication and widely used in error control application.

In this paper is the synthesis of the parity generator and checker, which has the unique architecture in terms of architecture complexity. Efficiency in terms of the VLSI performance attributes such as delay, power, and area. Then with the use of GDI technique a new architecture of parity generator and checker is introduced, we achieved a design with low supply voltage operation. The 3-bit parity generator and checker based on GDI technique is successful, simulated and tested at 0.5V, 1V, 1.5V, 2V supply voltage and consumed power at these voltages are 5µw, 2.5µw, 3.3µw and 0.2ns, 0.3ns, and 0.8ns worst condition of delay respectively.

Keywords **- GDI (Gate Diffusion Input), Low power, high speed, delay, area, transistor count, Sub-threshold level.**

I. INTRODUCTION

Transistor was invented in the year1947. From the day when transistors were invented low consuming area, low power consumption and high speed are the main predominant issues for exploration in the digital based designs. In this newly emerged contemporary technology, low power design has an important factor from past few years due to increasing demand of compound mobile system in the VLSI circuit design. Moreover, circuit inventors have recognized the effect of power consumption on IC staging, since its reliability is straightly associate to it. The increasing request for compact devices and mobile electronics have encouraged the demand for low power, low area and high speed. Given the increasing complications of designs, power expansion should be a aware effort starting from the beginning stages of a design, where the chance to save power is at a maximum. The rapid increase of mobile and small electronics merged and with increasing packaging costs together is combined and it is forcing the circuit designers to acquire low power, low area and high speed design procedures because low power designs of application specific integrated circuits (ASIC) results in increased battery life and better reliability. Certainly, the Semiconductor Industry Association technology roadmap has identified low power design techniques as a analytic technological need. [1]

Various logic styles include Pass Transistor logic, Transmission Gate logics have been introduced for low power and high speed. [2, 3] Pass Transistor logic is the one which is most deeply used logics for low power digital circuits. The PTL (Pass Transistor Logic) is most popular for low power digital circuits. The advantages of PTL when compared with conventional CMOS design is high speed, low power dissipation as a result the number of transistors are reduced and lower interconnection effects due to a small area. But the implementation of PTL logic has problem like slow operation speed at reduced power supply as the threshold voltage drop across the single channel pass transistor results in low drive current. GDI technique is suitable for designing of fast, low power circuits using reduced number of transistors when compared to conventional CMOS design and existing PTL techniques.

In communication system, data is altered with the undesired noise. So there is more anxious for identifying and rectify the errors, further which is added to the communication channel. Therefore, for detecting and correcting the errors a concept of parity is introduced. This approach is broadly used to identify an error in the receiving message. The parity bit is an extra bit added to the message in order to make the number of 1s either even or odd. In this paper, we are concentrating on odd and even parity. We have proposed parity generator (Pg) circuit to generate the odd and even parity at the transmitter end and parity checker (Pc) circuit to justify the odd and even parity at the receiver end. [4]

This paper presents the odd, even parity generator and checker circuits using GDI (Gate Diffusion Input) technique. This paper is structured as following. Section II gives the short description about the framework of basic GDI (Gate Diffusion Input) technique. In section III, the background study associated to Pg and Pc is carried out. The present circuits of odd, even parity generator and checker design are discussed in section IV. Section V contains the obtained results and discussions of the system and it is followed by conclusion of this paper in section VI.

II. BASICS OF GDI

The basic structure of GDI (Gate Diffusion Input) cell is as shown in the Figure. 1. It looks like similar to CMOS inverter in the first flash. The difference between GDI cell and CMOS inverter is that GDI has three inputs. [5]
The three inputs are:
One input is common gate input of nMOS and pMOS (G).
Second is the input to the source or drain of pMOS (P).
Third is the input to the source or drain of nMOS (N).
Inputs of both nMOS and pMOS are connected individually or combined. The output node is the combination of both nMOS and pMOS transistors. The basic functions that can be implemented using GDI cell is shown in the Table.1 below.

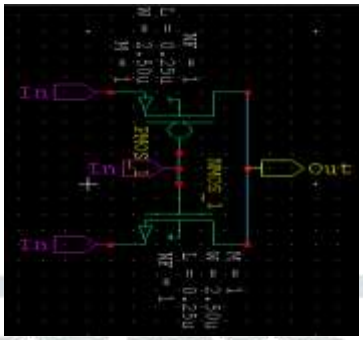

Figure.1: Basic Cell of GDI

The following are the functions used in GDI technique

N	P	G	OUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	FUNCTION1
B	1	A	A’+B	FUNCTION2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MULTIPLEXER
B’	B	A	A’B+AB’	XOR
B	B’	A	AB+A’B’	XNOR

Table.1: Functions Using GDI Cell

III. BACKGROUND STUDY

Recently advancement in VLSI technology, power, area and speed are important parameters in designing any digital circuits. [6] In this paper I am researching to reduce power, area and increasing speed of the diverse digital circuit for sub-threshold level. This can be possible by designing the digital circuit by using GDI (Gate Diffusion Input) technique. By using GDI technique in the digital circuit area, power can be reduced and speed is increased. Thus GDI technique is efficient for designing low power and high speed digital circuits. [7, 8]

Hence to reduce the area and power many techniques have been introduced like Pass transistor technique, transmission gate and GDI (Gate Diffusion Input) technique. Among them GDI (Gate Diffusion Input) technique is much efficient as it design takes less transistor for designing. Consequently area and power consumption also reduces and speed is increased.

IV. DESIGN OF THE PROPOSED ODD, EVEN PARITY GENERATOR AND CHECKER

We design the odd, even parity generator and checker circuits in this section. In sub-section (a), we present the cell layout of odd and even parity generator. In sub-section (b), a cell layout of odd and even parity checker is designed. The simulation of odd, even parity generator and checker circuits results and discussions is shown in sub-section V.

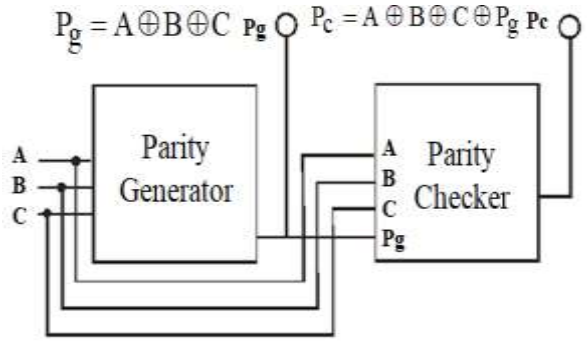

Figure.2: Block Diagram Of Parity Generator and Checker

(a). Odd and Even Parity Generator Circuit

In communication systems when binary data is transmitted, data may get corrupted due to noise, such corrupted noise can change the binary data from 1's to 0's vice versa. So in order to detect the error an extra bit is added at the end of the binary data which specify whether the no. of transmitted bits have even no. of 1s or odd no. of 1s. Therefore, this extra parity bit helps in diagnose the error. Consider there are three message bits namely A, B and C, the parity bit will be generated using the following equations where the Boolean equation is successfully replaced by the majority expressions. The truth table for generating the expression of Pg is shown in the following Table 2. From the truth table, we can observe that to make the input bits to odd and even 0 or 1 is added to it. XOR operation is performed between all the three message signals to generate the parity bit. [9,10,11]

3-bit message			Odd Parity bit generated	Even Parity bit generated
A	B	C	Pg	Pg
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

Table.2: Odd and Even parity generator truth table

$$Pg = A'B'C' + AB'C + A'BC + ABC'$$

$$Pg = A'B'C' + A'BC + AB'C + ABC'$$

$$Pg = A'(B'C' + BC) + A(B'C + BC')$$

$$Pg = A'(B \odot C) + A(B \oplus C)$$

$$Pg = A'(B \oplus C)' + A(B \oplus C)$$

$$Pg = A' \oplus B \oplus C \text{ (for odd)}$$

The following figures 3 and 4 shows the implementation of 3-bit odd and even parity generator, designed by using GDI (Gate Diffusion Input) technique.

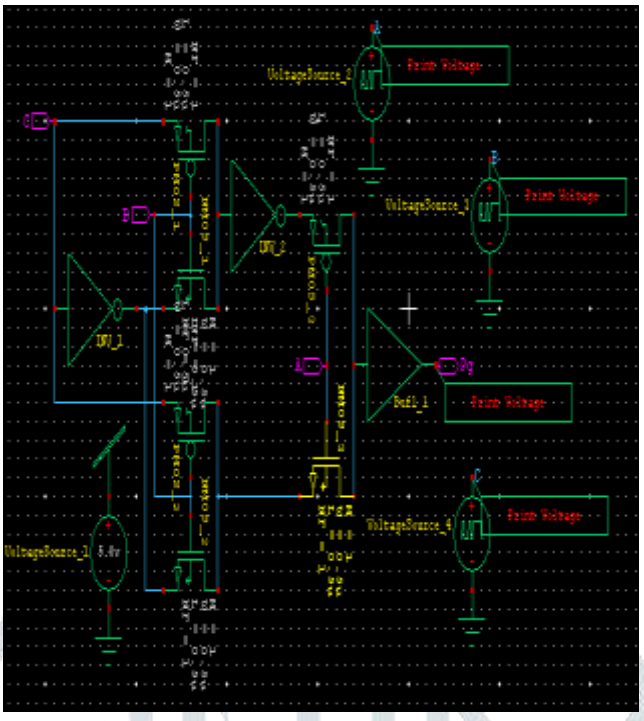

Figure.3: Schematic cell layout of odd parity generator.

$$Pg = AB'C' + A'B'C + ABC + A'BC'$$

$$Pg = A'B'C + A'BC' + AB'C' + ABC$$

$$Pg = A'(B'C + BC') + A(B'C' + BC)$$

$$Pg = A'(B \oplus C) + A(B \odot C)$$

$$Pg = A'(B \oplus C) + A(B \oplus C)'$$

$$Pg = A \oplus B \oplus C \text{ (for even)}$$

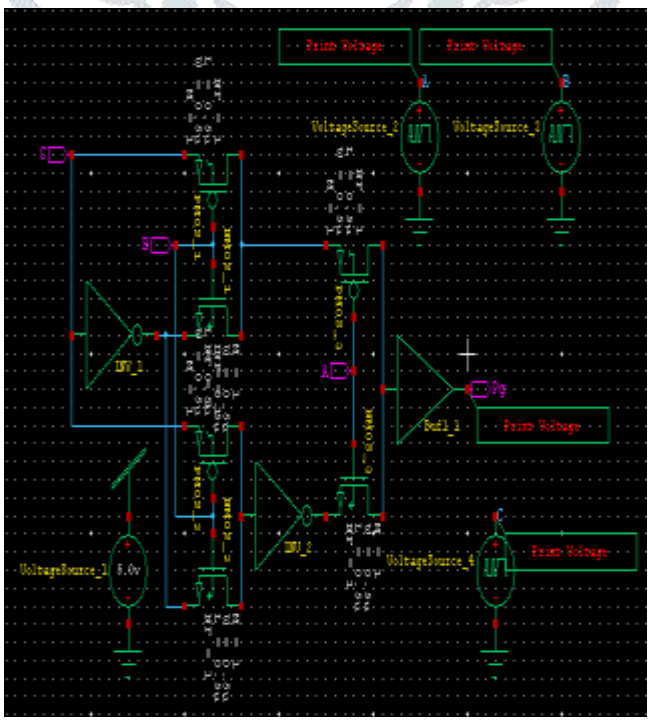

Figure.4: Schematic cell layout of even parity generator

(b). Odd and Even Parity Checker Circuit

The parity bit, Pg generated in parity generator circuit, will be transmitted along with the 3-message bits. So the four inputs A, B, C and Pg will be given as the inputs to the parity checker circuit which checks the probability of error in the received data. For instance if the data with Odd parity is transmitted, the received message must contain the Odd number of 1's and if the data with even parity is transmitted, then the received message must contain the even number of 1's. If the output of parity checker Pc, is 0 than there is no error in the transmission and if the output of parity checker Pc, is 1 than there is no error. Thus, the output of the parity checker circuit is given by following equation. [9,10,11]

$$Pc = A \oplus B \oplus C \oplus Pg' \text{ (for odd)}$$

$$Pc = A \oplus B \oplus C \oplus Pg \text{ (for even)}$$

4-bit message				Odd Parity checker	Even Parity checker
A	B	C	Pg	Pc	Pc
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	0

Table.3: Odd and Even parity checker truth table

The following figures 5 and 6 shows the implementation of 4-bit odd and even parity checker, designed by using GDI (Gate Diffusion Input) technique.

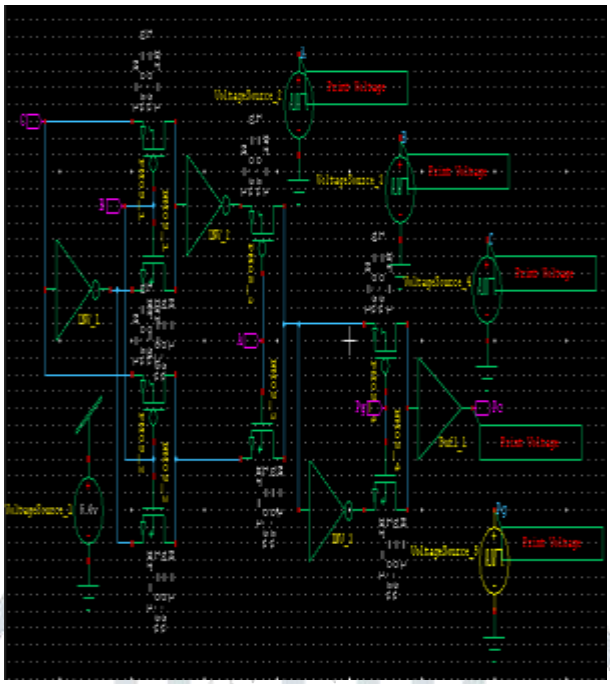

Figure.5: Schematic cell layout of odd parity checker

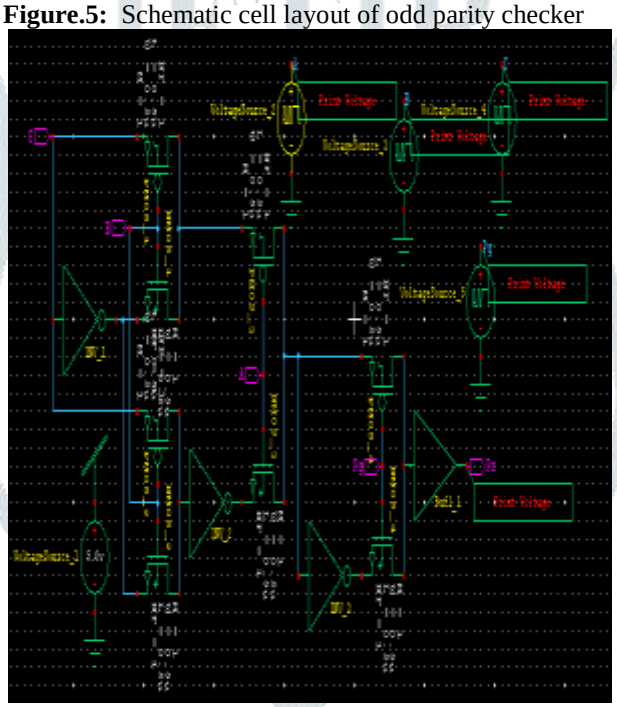

Figure.6: Schematic cell layout of even parity checker

V. RESULTS AND DISCUSSIONS

The following are the result obtained for 3-bit odd parity generator using Tanner EDA tool v16 operating at a voltage of 5v. In the results A, B, C are the inputs and Pg is the output. The results are obtained according to the truth table.

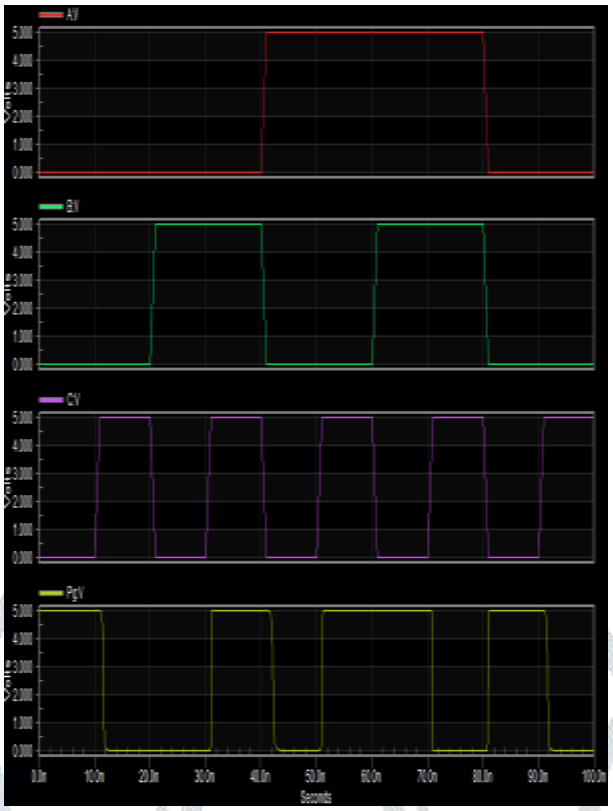

Figure.7: Odd parity generator circuit Simulation Result

The following are the result obtained for 3-bit even parity generator using Tanner EDA tool v16 operating at a voltage of 5v. In the results A, B, C are the inputs and Pg is the output. The results are obtained according to the truth table.

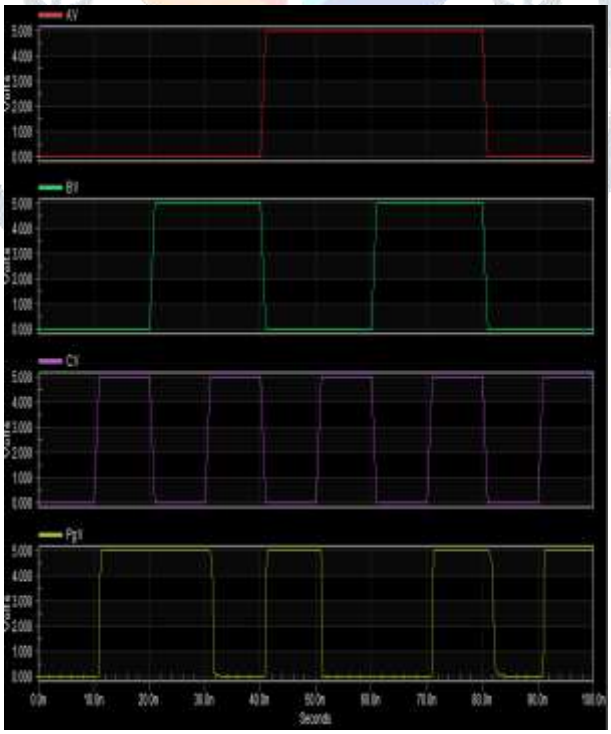

Figure.8: Even parity generator circuit Simulation Result

The following are the result obtained for 4-bit odd parity checker using Tanner EDA tool v16 operating at a voltage of 5v. In the results A, B, C, Pg are the inputs and Pc is the output. The results are obtained according to the truth table.

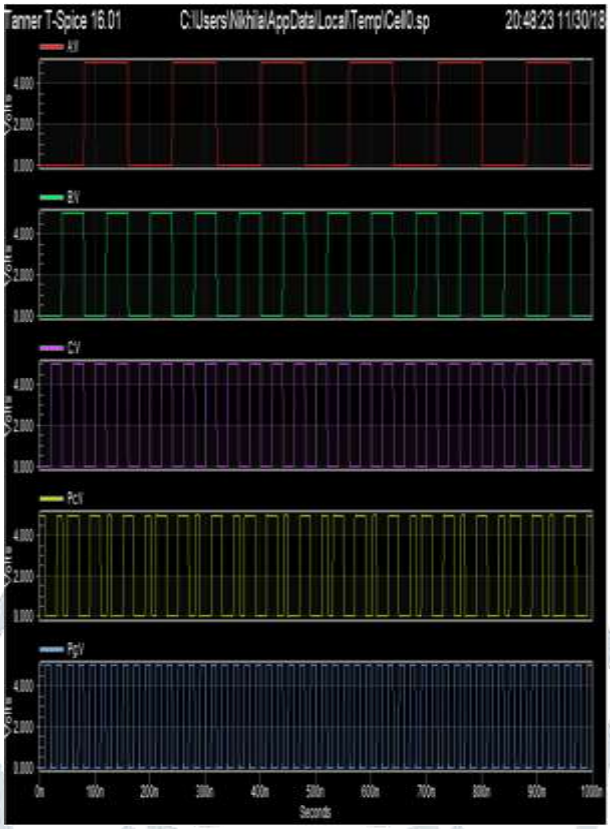

Figure.9: Odd parity checker circuit Simulation Result

The following are the result obtained for 4-bit even parity checker using Tanner EDA tool v16 operating at a voltage of 5v. In the results A, B, C, Pg are the inputs and Pc is the output. The results are obtained according to the truth table and the discussions of the circuit at different sub-threshold levels are compared in sub sections.

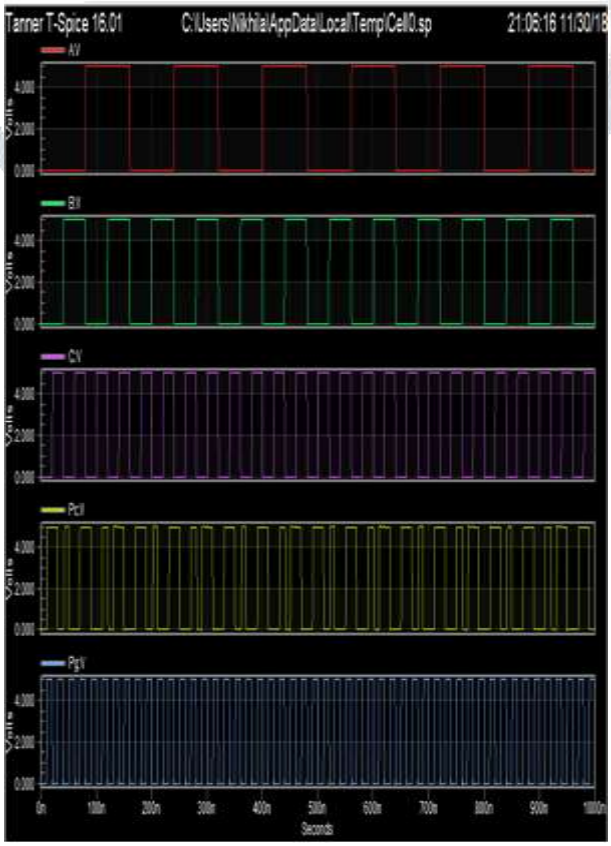

Figure.10: Even parity checker circuit Simulation Result

(a). Estimation of power related to odd, even parity generator and checker.

Parity/ Voltage	0V-0.5V	0V-1V	0V-1.5V	0V-2V
Odd parity generator	5.0 µw	2.5 µw	3.3 µw	2.2 µw
Odd parity checker	8.4 µw	5.3 µw	1.0 µw	6.2 µw
Even parity generator	6.1 µw	2.9 µw	2.9 µw	1.7 µw
Even parity checker	4.0 µw	2.2 µw	2.7 µw	4.6

Table.4: Voltage–Power variations for different Parities.

(b). In this section the comparison of parity circuits at different sub-threshold levels i.e.; VTH0=0.343, 0.323, 0.303 are discussed.

i) Comparison of circuits at VTH0=0.343.

S.No.	Parity	VTH0 = 0.343			
		Power (µw)	Rise time(µs)	Fall time(µs)	Delay (ns)
1	Odd Pg	2.1	1.2	1.1	0.12
2	Odd Pc	6.5	4.1	4.0	0.76
3	Even Pg	1.9	1.1	1.2	0.73
4	Even Pc	4.6	4.1	2.2	0.84

Table.5: Comparison of circuits at VTH0=0.343.

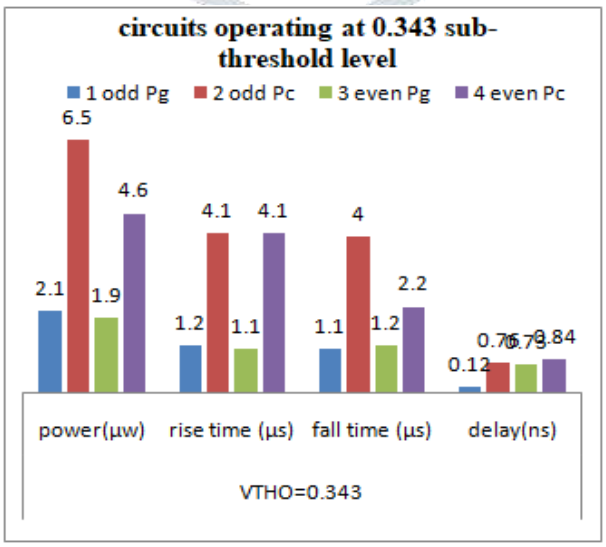

Figure.11: Plots of power, rise time, fall time and delay at VTH0=0.343.

ii) Comparison of circuits at VTH0=0.323.

S.No.	Parity	VTH0 = 0.323			
		Power (µw)	Rise time(µs)	Fall time(µs)	Delay (ns)
1	Odd Pg	2.2	1.4	1.1	0.11
2	Odd Pc	7.0	4.1	4.0	0.71
3	Even Pg	1.9	1.1	1.1	0.92
4	Even Pc	4.8	4.1	7.2	0.29

Table.6: Comparison of circuits at VTH0=0.323.

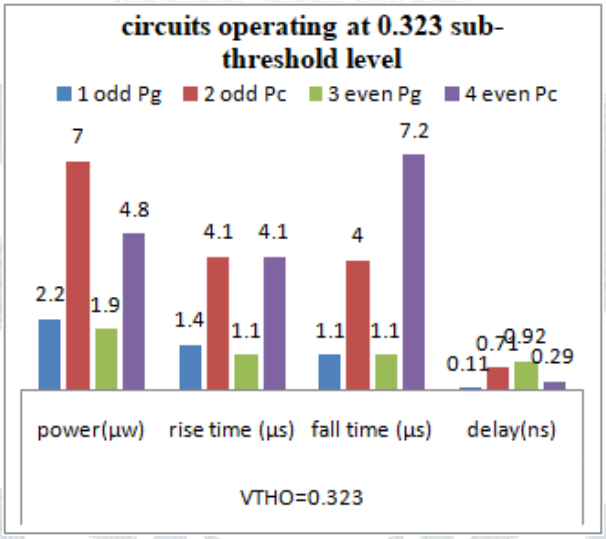

Figure.12: Plots of power, rise time, fall time and delay at VTH0=0.323.

iii) Comparison of circuits at VTH0=0.303

S.No.	Parity	VTH0 = 0.303			
		Power (µw)	Rise time(µs)	Fall time(µs)	Delay (ns)
1	Odd Pg	2.4	1.5	1.0	0.96
2	Odd Pc	7.5	4.1	4.0	0.66
3	Even Pg	2.0	1.0	1.8	0.27
4	Even Pc	4.6	4.1	7.7	0.28

Table.7: Comparison of circuits at VTH0=0.303.

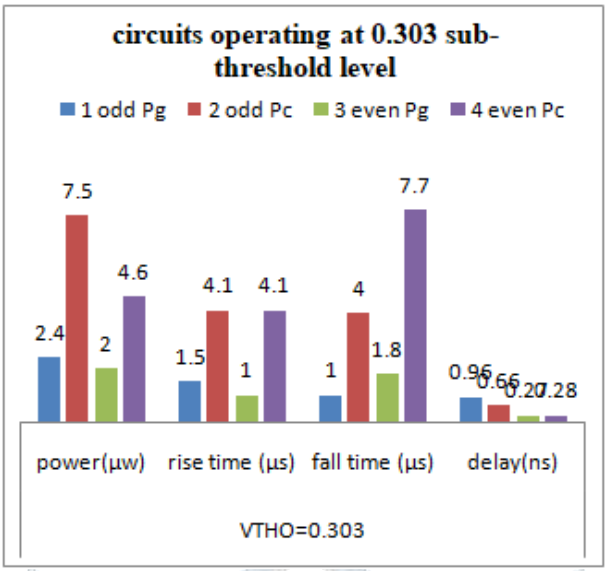

Figure.13: Plots of power, rise time, fall time and delay at VTH0=0.303.

VI. CONCLUSION

In this paper, a unique design of odd, even parity generator and checker circuit using GDI (Gate Diffusion Input) technique is designed to reduce the power, delay and also speed up the system design at sub-threshold level. The number of transistors used for designing the circuits is reduced and the power used by the designs is much less because of less complexity of the designs and power consumed by these circuits at voltages is 2.2µw, 6.2µw and 1.4µw and 0.2ns, 0.3ns, and 0.8ns worst condition of delay respectively, so this paper satisfies low power and high speed constraints. This paper also provides the schematic design and simulation waveforms of designs. In this paper the circuits are designed with less number of transistors and the predicted designs are simulated. The outputs of all the circuits are obtained successfully and verified using Tanner V16 designer tool.

VII. REFERENCES

[1] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low- power CMOS digital design," IEEE J. Solid-State Circuits, vol. 27, pp. 473–484, Apr. 1992.
[2] J. P. Uyemura, Circuit Design for CMOS VLSI. Norwell, MA: Kluwer Academic, 1992, pp. 88– 129.
[3] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low- power CMOS digital design," IEEE J. Solid-State Circuits, vol. 27, pp. 473– 484, Apr. 1992.
[4] Neeraj Kumar Misra, Subodh Wairya and Vinod Kumar Singh, "Approaches to Design Feasible Error Control Scheme Based on Reversible Series Gates" European Journal of Scientific Research, vol. 129, no. 3, pp. 224-240, 2015.
[5] IEEE Transactions on Very Large Scale Integration (VLSI) Systems, VOL. 10, NO.5, OCTOBER, 2002.
[6] International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.
[7] Arkadiy morgenshtein, Alexander fish & Israel Wagner, "Gate Diffusion input (GDI): A power efficient method for digital combinatorial circuits", IEEE Transaction on very large scale integration (VLSI) systems vol.10, no. 5 October 2002.
[8] Basic VLSI Design by Douglas A.Pucknell Kamran Eshraghian, 3rd edition, 2005 PrenticeHall India.
[9] Prateek Agrawal, S.R.P.Sinha, Neeraj Kumar Misra, Subodh Wairya, "Design of Quantum Dot Cellular Automata Based Parity Generator and Checker with Minimum Clocks and Latency," August 2016 in MECS.
[10] M. Mustafa, and M. R. Beigh, "Design and implementation of quantum cellular automata based novel parity generator and checker circuits with minimum complexity and cell count," Indian Journal of Pure and Applied Physics, 51, pp. 60-66, 2013.
[11] N. R. G, P. C. Srikanth, and P. Sharan, "A novel quantum dot cellular automata for parity bit generator and parity checker," International Journal of Emerging Technology in Computer Science & Electronics, 14, 2015.