EFFICIENT SCAN CHAIN MASKING AND RE-ORDERING FOR DIAGNOSIS OF MULTIPLE FAULTS IN VLSI CIRCUITS

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***Abstract*—** Time, power and test data volume are among some of the challenging issues for testing the VLSI systems and have not been fully resolved. The power and energy may increase significantly during testing, this extra power consumption may give rise sever hazards to the circuit reliability and effectively increases the test cost and time. Scan chain masking is a technique which makes the testing of the digital circuits easier by providing simple method to observe each and every flip-flops in the design. When Flip-Flops are connected in series forms a Scan chain and when two or more Scan chains in a single compactor forms complexity in diagnosis the integrated circuits. In this paper diagnosis of multiple failures in multiple Scan chains were proposed. The strategy mainly focused on test time reduction, power reduction during testing.

Index Terms —Automatic Test Equipment(ATE); masking ; Scan chain diagnosis; test response compaction; test data compression.

I. INTRODUCTION

For CMOS circuits, there are three main sources of power dissipation occurs: dynamic switching power due to the charging and discharging of circuit capacitances, short-circuit current power due to finite signal rise/ fall times, and leakage current power from reverse-biased diodes and sub threshold conduction. For existing CMOS technology, dynamic switching power is the dominant source of power consumption and is proportional to the amount of switching activity in the circuit. Switching activity in a circuit can be much greater during test than during normal operation. This is because successive functional input vectors applied to a given circuit during system mode have a significant correlation. In contrast, the correlation between consecutive test patterns generated by an Automatic Test Pattern Generator (ATPG) for external testing or by a Linear Feedback Shift Register (LFSR) for Built-In Self Test (BIST) can be low. The power consumed during test could be twice as high as the power consumed during normal operation. Excessive power consumption during test may result in several kinds of problems: instant circuit damage, increased product costs, decreased system reliability, reduced autonomy of portable systems and decrease of overall yield.

Once the circuit fails the flush test during testing of the integrated circuit, it can provide information on fault type and the faulty chain indices. There are many diagnosis technique were discussed in literature section to identity the faulty scan cells effectively.

W. D. Seng proposed a method of reducing power during scan testing in VLSI by arranging the scan cells which cause more internal circuit transitions to the positions with low transition weights of the scan cell .Two main functions such as scan cell transition count and impact functions of scan cell on internal circuit also calculated to achieve scan cell ordering and hence a power reduction of 17.35% were reported without considering an test vector reorder [2]. Nan-Cheng Lai presented a method of reducing power during a scan based BIST(built in self test).The technique combines a low power TPG(test pattern generator) with a Scan chain reordering technique. This work addressed a smoother with TPG to reduce the average power consumption but probability of fault coverage affected by the smoother. To overcome this fault coverage problem a cluster based scan chain reordering method was introduced. The results shown that by maintaining same test length the average test power was reduced by 58.66% with a 2 bit smoother and 85.55% with 3 bit smoother[3]. Yu-Ze Wu and Mango C-T Chao proposed a scan cell reordering approach ,which connects all scan cells with high response correlation to reduce transitions in the scan out during test mode while preserving all don't care bits in the test patterns for later optimization. The scheme combined with a pattern filling technique and utilizes both response correlation and pattern correlation simultaneously to minimize transitions in both scan-out and scan-in. The tradeoff between power driven scan cells reordering and routing driven scan cell were discussed , average of 45.7% reduction in power during scan shift transition were noticed [4]. Ayan Datta and Charudattan Nagarajan introduced an approach called as TSV(trough Silicon Vias) Scan chain ordering to reduce the 3D scan chain wire length optimization. The method employs multiplexing the TSVs between scan and functional path across two consecutive tires in a 3D IC. The results shown that the total scan wire length reduction was 31% when compared with the 2D scan chain optimization and total area reduced by 8-9% [5]. Usha Sandeep Mehtha proposed a hamming distance based distributed scan cell reordering technique where reordering was made separately for loading and unloading of scan in and scan out bits respectively. During loading of the in bit stream and unloading of last bit produce more transitions hence power consumption also more but time, area utilization was more [6]. Sungyoul Seo and Young Lee presented a approach for Scan chain reordering aware X filling and stitching for scan shift power reduction. For a complex circuit the scan cell count may high and excess power consumption produces a low shifting frequency during scan shift mode. Presented an scan shift power reduction with reduction in test

cost and speed up the shift frequency during shift mode [7]. Chandan Giri and Pradeep Kumar Choudary presented an scan power reduction through scan architecture modification and test vector reorder for reducing dynamic power consumption during testing by introducing XOR gates at selected places in the scan chain and converting D-flip-flop into T-Flip-flop temporarily during scan. Work mainly focused on scan vector reordering instead of Scan chain reordering and gained 34% reduction in switching activity within the circuit [8]. Chandanagiri and Naveen Kumar reported an scan flip-flop reordering to reduce the delay and time with reduction in power. It includes an genetic algorithm which considers the weighted sum of both delay and transition occurring during testing. Genetic algorithm is a class of stochastic search and global optimization technique used to identify globally optimal or near optimum solutions [9]. Mokhtar Hierech and James Bcausang presented a new approach to scan chain reordering using physical design constraints violations. The idea behind this work was to integrate the scan chain reorder functions into synthesis based design re-optimization takes place either in floor planning or place and root [10]. Wei Li and Seong moon Wang proposed an distance restricted scan chain reordering to enhance delay fault coverage .The work introduced an Scan chain reordering technique by maintaining a distance for the relocation of scan cell in the chain .It minimized routing overhead and fault coverage improved by 21.8%. An simulated annealing optimization algorithm was discussed and improved stuck open fault coverage [11]. Jonisha Stanis S and Maria Antony proposed an reordering and test pattern generation for reducing launch and capture power an VHDL based fault injection method was proposed to reorder the test vector [12]. Shalini Ghosh and Sugato Basu discussed an joint minimization of power and area in scan testing by scan cell reordering that used an novel dynamic minimum transition fill technique to fill the unspecified bits in the test vector to reduce the scan power during testing including reduction area overhead in comparable with random ordering of the scan cells. In this work for a given test vector set, found an optimal reordering of the scan cells that minimizes the score function, it is a linear combination of power and area [13]. Shrevin sharifi and Mohammad Hosseinabadi proposed a method of reducing test power in SoC testing using a Selective Trigger Architecture. The proposed scan cell will work in 3 modes namely :Shift mode, normal mode and Trigger mode .The architecture reduces the switching activities in the CUT. Scanning the data at higher frequency are possible because MUX s are not used in the scanning path [14]. T. C. Huang and K. J. Lee propose a token scan cell architecture for low power testing and achieved great power reduction [16]. Parthik Girard discussed a low power Testing of VLSI Circuits :Problems and Solutions. In the first phase discussed about the problems associated with testing of the VLSI systems externally and in BIST. In the second phase discussed about the techniques used to overcome the problems mentioned along with reduction in power during testing [17]. Y. Bonhomme and P. Girard propose a method of reducing the test power during the Testing of SOCs. In this approach including logic power and scan power, a method of reducing clock power by considering an concept called as gated clock scheme for the scan path and clock tree feeding the scan path was introduced. The Idea behind the technique is to reduce the clock rate on the scan cell during each shift operations without adding the test time. The architecture consists of a clock, its speed is half of the speed of the normal speed to activate one half of the scan cells in the path during one clock cycle of the scan operation and the second half of the scan cells in the scan path activated by another clock with speed is equal to half of the normal speed. The two clocks are synchronous with system clock and have same but shifted in time period during scan operation . The use of these modified clock operation reduces the transition density in the CUT[22].

Seongmoon Wang and Sandeep K Gupta proposed an ATPG (Automatic Test Pattern Generator) Technique to reduce the switching activity during full scan testing of sequential circuits. This method of testing exploits all don't cares during scan shifting, test application and response capture to minimize the switching activity in the CUT. Don't cares at primary inputs are used to block the gates which makes unnecessary transitions during scan shifting and Don't cares at state inputs are assigned with binary values to reduces the transition count. It shown that the length of the test sequence can be reduced by two ways [24]. Arranging the scan chains such a way that compatible state inputs are placed in neighboring positions. Using more sophisticated K-L Bi partitioning algorithm which assigns don't cares as state inputs. Mehrdad Nourani and Mohammad Tehranipoor presented a Low Transition Test pattern generator for BIST based Testing. A low transition test pattern generator also called as LT-LFSR (Low Transition Linear Feedback Shift Register) has been implemented which can be used in scan based combinational and sequential circuits which can be tested. The technique manages the reduction in the average and peak power during testing of circuits by reducing the transitions among the patterns in two dimensions . 1) The vertical dimension between consecutive test patterns (Hamming Distance) and 2) The horizontal dimension between the adjacent bits of a pattern sent to a scan chain. The conventional LFSR can be modified in such a way that it automatically inserts intermediate patterns between its original patterns [25]. Lung –Jen Lee and Wang-Dauh Tseng Adopted a method a Dual-LFSR reseeding technique for low power testing. The work mainly focused on BIST-based compression method for minimizing the test data volume and hence the reduction in test power. An Dual-LFSR are used as de-compressor to jointly generate the test pattern for a given test set [26]. Umesh Parashar worked by combining test-per-clock and test-per-scan test schemes, using two functional cycle lengths during scan and LT-RTPG(Low Transition Random Test Pattern Generator) as TPG (Test Pattern Generator) achieved an reduction in the switching activity as compared to conventional LFSR–BIST [23]. Lung-Jen Lee and Chia-Cheng He discussed about a deterministic ATPG for low capture power testing, in this work scan chain clustering method is used and whole architecture works in two modes of operation namely shift mode and capture mode. Scan chain clustering aims at disabling some non-critical scan cells during capture mode without affecting the fault coverage [19]. Abdallatif S. Abu-Issa and Iyad K.Tumar presented the use of SR-Counter (Switch-tail-Ring Counter) as low transition TPG in Test-per-clock and Test-per-scan BIST Applications. In SR-TPG for Test-per-clock BIST TPG was implemented by dividing a register into number of switch-tail ring counters during test mode. The first ring counter will be triggered directly by the system clock and the second one will be triggered using the system clock and control logic of the previous counter and so on for the remaining counters. In SR-TPG for Test-per-scan BIST TPG an output of a cell of the TPG will be used to scan-in the test vectors into the CUT inputs and memory elements [43]. A

Kavitha and G. Seetharaman designed an Low Power Test Pattern Generator (LP-TPG) to reduce the switching activity between the test patterns by combining a LP-TPG, an m-bit counter, gray code converter and NOR gate structure and XOR array [18].

By considering all above survey the Scan chain based VLSI testing still requires improvements in several aspects:

- External and BIST based testing for low power has requires area minimization.
- Multiple faults per chain are important for diagnosing chain failures caused by systematic defects.
- A reliable common solution for test-per-clock and Test-per-scan BIST testing is needed.
- A reliable solution for minimizing the switching activity between the scan cells in a scan chain and test vectors in a test pattern is required.
- A low power solution for diagnosing the multiple faults in a multiple chain failure is needed.

I. PRINCIPLE OF SCAN CHAIN DIAGNOSIS

Fig.1. shows an example of how to use the space compactors to produce improper compacted responses at an output channel when multiple chains observed through the same compactor fail. We can observe that when chain1 has fault at cell1 and chain 3 has fault at cell3, both the cells stuck at cell1 and cell3 respectively. After space compaction some of them will cancel each other messing up the compacted response. It makes confusion to decide which cell has the faulty with particular chains, its very difficult to identify the faults out of N channels from the compacted response. In other way by using some strategy, we can mask out chain 3,we possibly able to diagnose the failing cell of chain1 and vice versa.

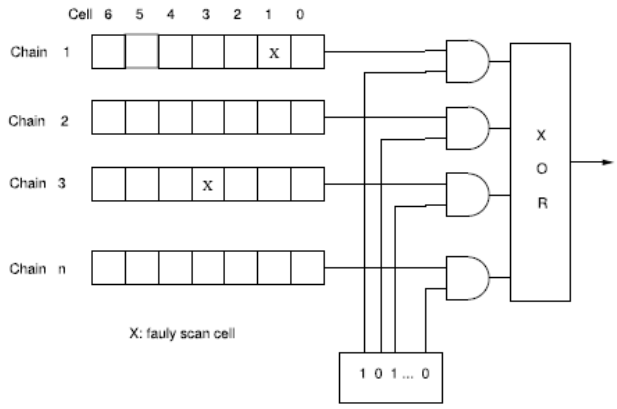

Fig. 1. Example of multiple chain failure

II. PROPOSED ARCHITECTURE OF TESTER

Fig. 2. shows the proposed architecture, the main strategy is to mask additional Scan chains to improve the diagnosis capabilities. The masking strategy is based on generating some essential patterns for any combination of failed scan chains. This will ensure that the compacted responses of the essential patterns will only be affected by one particular chain. Diagnosis of that chain will be extremely benefited by this. It may be noted that masking is done only at the compactor side, not at the de-compressor side. Therefore, the fault from any faulty chain can still cause loading errors and these errors can be propagated to good chains as well as faulty chains. However, if for a pattern only one failed chain is observed (all remaining faulty chains being masked), the failure at a compacted response may come from: 1) The loading errors on the masked faulty chains; 2) The loading errors at the non masked faulty chains; and 3) The unloading errors on the non masked faulty chains. The unloading errors on the non masked faulty chain will affect almost the entire compactor response bit stream, whereas the loading errors on the masked faulty chain can only affect a few of the bits. Therefore, a scan chain diagnosis algorithm based on the partial matching response can successfully identify the failing chains even in the presence of loading errors on the masked faulty chains. Hence, the problem of generating mask signals (normally mask signals are generated to block X's present in the responses) has been formulated for each pattern such that the compacted responses have enough information (essential patterns) for diagnosis of the failed Scan chains.

A simple heuristic has been proposed to solve the problem. The input to the algorithm is the pattern set and mask signals generated by the normal test generation flow. Initially make a list of all possible Scan chain combinations and keep track of their corresponding metrics. Without considering the cases where actual number of faulty scan chains is less than the maximum number of faulty chains considered by the tool.

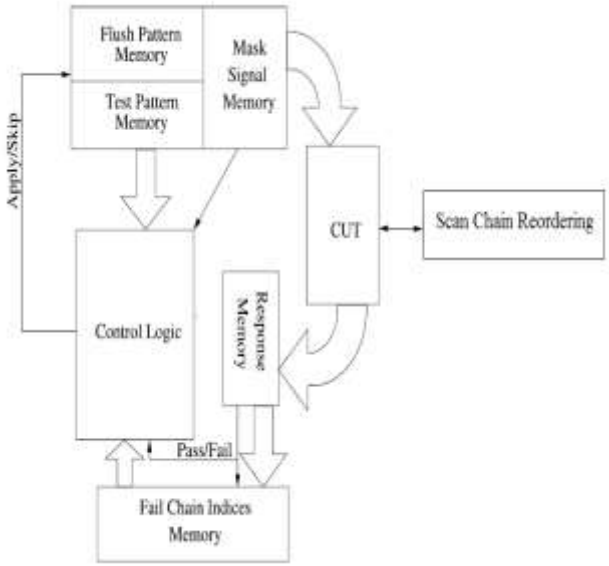

Fig. 2. Proposed tester architecture

II. WORKING PRINCIPLE

First the flush patterns are to be applied to the CUT. If the circuit fails the flush test, the failed chain indices are stored in failed chain index memory. Then the control logic will check the mask signal and the failed chain indices, and decide whether to apply or skip the current pattern. Fig. 2. shows the block diagram of the tester. Compared with the conventional external tester, the modified tester contains a control logic that decides whether to apply or skip a pattern. The rest of the tester architecture remains unaltered. For the proposed modified architecture, we have actually implemented two different approaches to select which of the patterns are going to be applied. In the first approach, the test patterns are selected on the fly. For a pattern next in the list, the tester generates a signal, apply/skip based on whether the pattern contains enough information for diagnosis. When the applied pattern count reaches a specified limit, the tester stops. The advantages of this approach are that the control logic for the tester is fairly simple and also the test time is less. The control logic of this approach can easily be generated by calculating the number of unmasked failed chains for a particular pattern. As given in [1], if more than 2 faulty chains are observed through the compactor, there is a very low chance to find any valuable information. Thus, if the number of observed failed chains is more than two, skip the pattern. Otherwise, apply it. In the second proposed method, the tester checks all the patterns and finds out the suitable patterns which may have the most valuable information for diagnosis. The control logic of the tester is a bit complex, but a better diagnosis result could be achieved. The control logic assigns weights to every test pattern based on [1] and also considering the number of times a particular chain(s) has (have) already been observed. Let us take an example, consider the failed chain indices to be 1 and 2. Suppose patterns 1 and 2 observe chain 1 only while pattern 3 observes only chain 2. Since all the patterns observe only one failed chain, they should have similar weight. However, as already taken a pattern which will help in diagnosis of chain 1, the weight of pattern 2 is less than that of pattern 3. Similarly, the chain combinations are also considered while generating the weight for a pattern. Once the patterns have been assigned weights, the best patterns are found out and applied.

III. SCAN CHAIN REORDERING

The proposed technique has been combined with a cell-ordering algorithm, which reduces the number of transitions in the Scan chain while scanning out the captured response. The problem of the capture power (peak power in the test cycle) will be solved by using a novel algorithm that will reorder some cells in the scan chain in such a way that minimizes the Hamming distance between the applied test vector and the captured response in the test cycle, hence reducing the test cycle peak power (capture power).

Algorithm for scan chain Reordering :

Step 1: Simulate the CUT for the test patterns generated by the LFSR.
Step 2: Identify the group of vectors and responses that violate the peak power.
Step 3: In these vectors, identify the cells that mostly change their values in the test cycle and cause the peak-power violation.
Step 4: For each cell found in step 3, identify the cells that play the key role in the value of this cell in the test cycle.
Step 5: If it is found that, when two cells have a similar value in the applied test vector, the concerned cell will most probably have no transition in the test cycle, then connect these cells together. If it is found that, when two cells have a different value, the cell under consideration will most probably have no transitions in the test cycle, then connect these cells together through an inverter.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed work has implemented on bench mark circuit of S27 and S5378, which has neatly simulated by using Modelsim 6.3 and Xilinx Isim simulator and the power and area utilization observed by using cadence tool. The simulation results are shown in fig. 3. To fig. 6.

- op and op_f are the 179 bit final scan chain outputs of original and faulty S5378 circuit respectively.
- scsel is the scan select to select input from its adjacent scan cell or circuit under test.
- v_out and v_out1 are the 35 bit primary inputs of original and faulty S5378 circuit respectively.
- z and z1 are the 49 bit primary outputs of original and faulty S5378 circuit respectively.
- scan_p1,scan_p2,scan_p3,scan_p4,scan_p5,scan_p6,scan_p7,scan_p8,scan_p9,scan_p10,scan_p11,scan_p12,scan_p13,scan_p14,scan_p15,scan_p16,scan_p17,scan_p18 are the input of the 18 scan chains in S5378.
- scan_op1,scan_op2,scan_op3,scan_op4,scan_op5,scan_op6,scan_op7,scan_op8,scan_op9,scan_op10,scan_op11,scan_op12,scan_op13,scan_op14,scan_op15,scan_op16,scan_op17,scan_op18 are the outputs of the 18 scan chains in S5378.

When scsel is '0' then test patterns are shifted into 18 scan cells. Once all are loaded then scsel is enabled('0') which stores the value of circuit under test into the Scan chain. scsel is then made '0' to shift out the response. The output is then masked and compared with expected one to identify fault.

TABLE I. Result of Gate counts, Area, Power and time analysis for S27, S5378 and S5378-reorder circuits

Circuits	No of Gates	Area(µm2)	Power(mW)	Time(ps)
S27	33	1373	47	10000
S5378	1396	16750	208	10000
S5378-reordered	1184	15416	98	10000

Circuits are later implemented to FPGA and the Analysis done by using Chipscope and Modelsim as follows

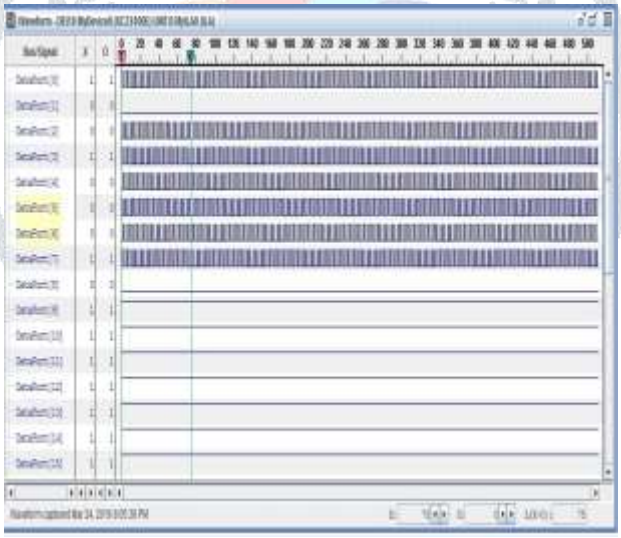

Fig. 3. Timing analysis S27 circuit using Chipscope

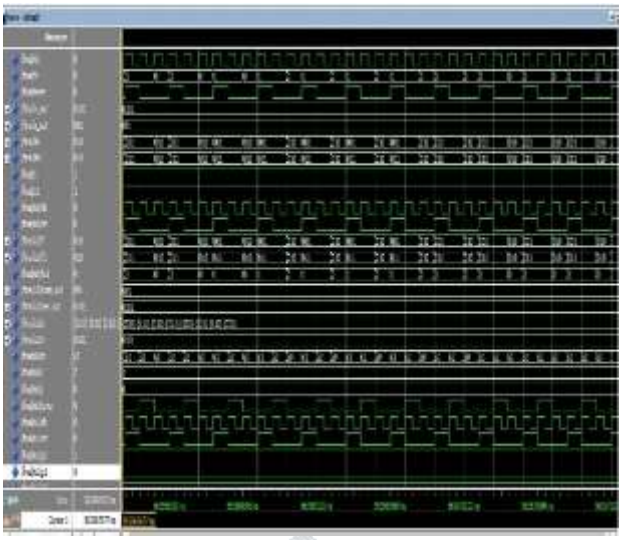

Fig. 4. Simulation results observation for S27 circuit

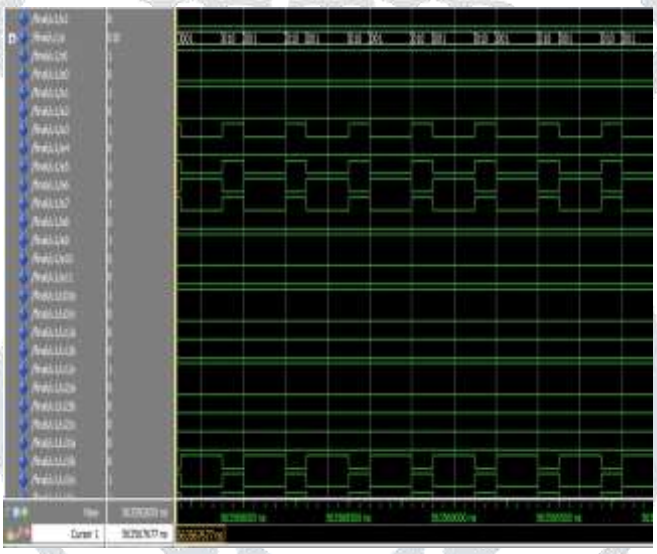

Fig. 5. Simulation results observation for S5378 circuit

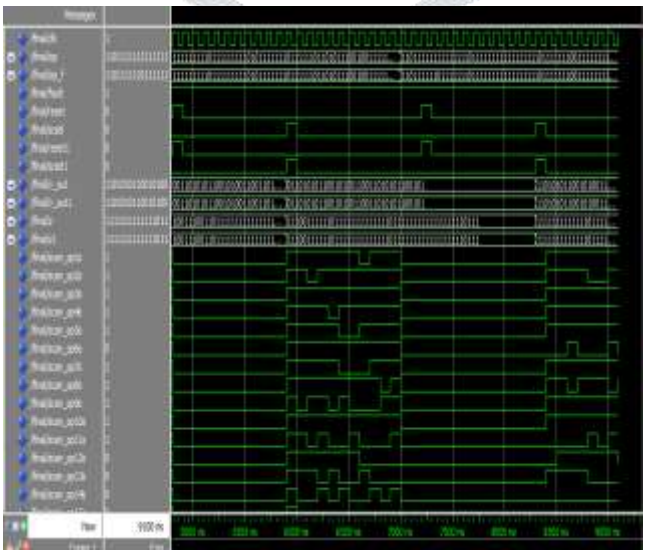

Fig. 6. Simulation results observation for S5378-reordering circuit

V. CONCLUSION

In this paper , we have proposed an tester architecture with re-ordering technique for diagnosing the multiple scan cell failures in multiple scan chains .The strategy uses less power during testing the integrated circuits and area and time consumption also less. The architecture implemented and tested for benchmark circuits S27 and S5378.The future work proceeding with applying selective scan cell triggering method.

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